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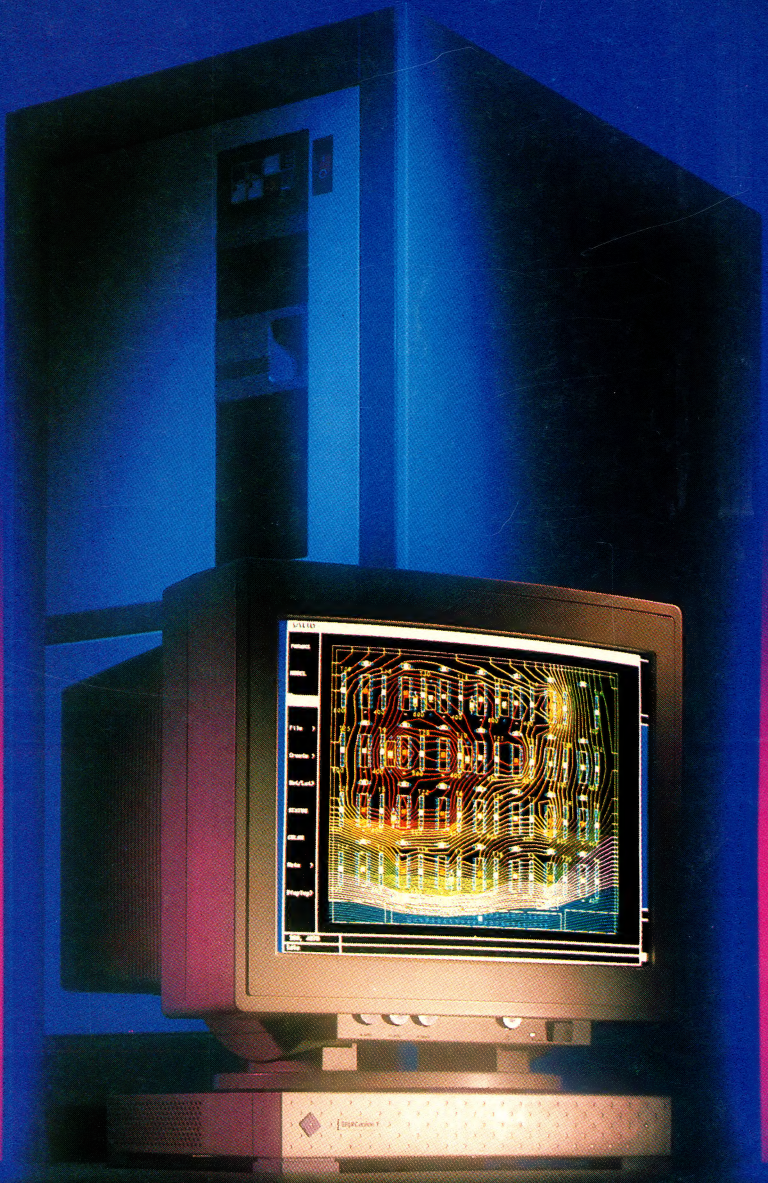

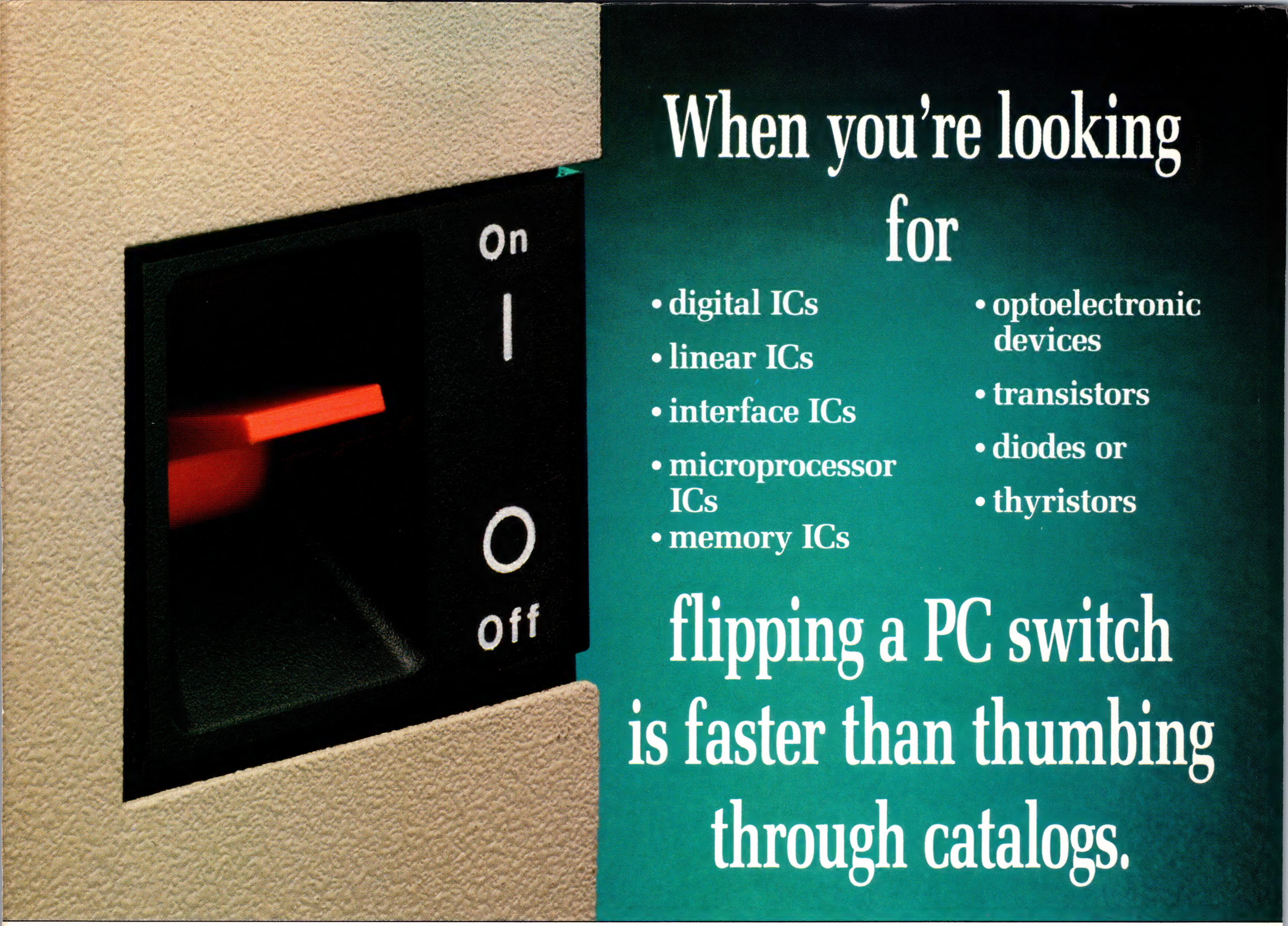

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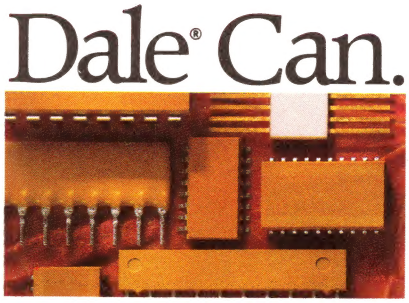

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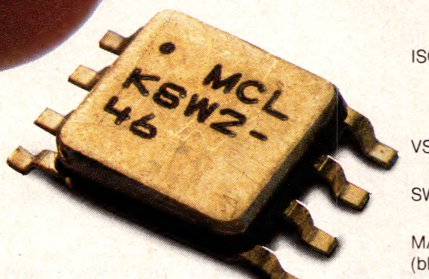
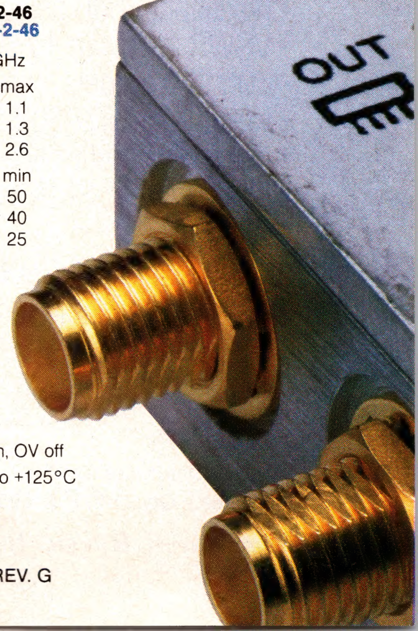


SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95** **$69.95**		**$48.95** **$79.95**	



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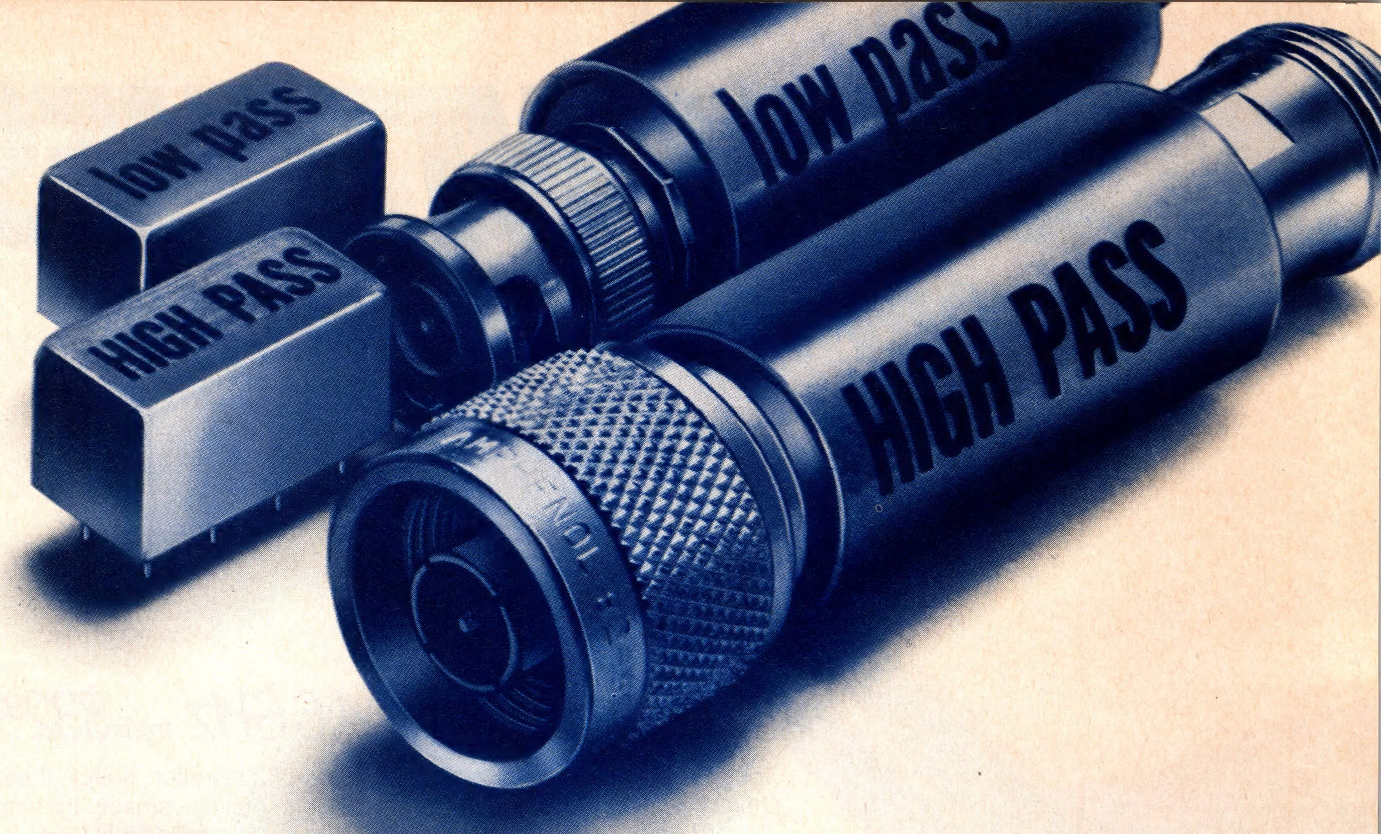

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LOW PASS Model *LP-	10.7	21.4	30	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to	10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max, 20dB Stop Frequency (MHz)	19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

Prices (ea.): Qty. (1-9) P $11.45, B $32.95, N $35.95, S $34.95

HIGH PASS Model	*HP-	50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.	41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	150	190	290	365	460	520	570	660	720

Prices (ea.): Qty. (1-9) P $14.95, B $36.95, N $39.95, S $38.95

*Prefix P for pins, B for BNC, N for Type N, S for SMA *example:* PLP-10.7

C105 REV. E

EDN® Magazine Edition

Volume 34, Number 23

November 9, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *It's not only processor performance that should influence your selection of a low-cost workstation; look, too, for third-party software support. Turn to pg 128 for our Special Report. (Cover photo features Sun Microsystems Inc's 12.5-MIPS SPARCstation 1 demonstrating Valid Logic Systems' Thermostats, a thermal-analysis pc-board-design package. Photo courtesy Sun Microsystems Inc)*

SPECIAL REPORT

Low-cost workstations 128

Even the world's fastest workstation will do you no good if it can't run the software you need. Before you select a workstation, make sure it can run your CAE software.—*Margery Conner, Regional Editor*

American engineers in Japan: Getting by with a little help from their friends 67

This article is the third in a series about engineering in Asia and the second of two articles about American engineers living and working in Japan.—*Gary Legg, Special Projects Editor*

DESIGN FEATURES

Wescon/89 147

Wescon/89 features a diverse program of courses and sessions on timely electronics issues.—*Tom Ormond, Senior Editor*

Wescon/89 Products 151

Designer's guide to resonant-mode power supplies—Part 1 201

Resonant-mode design techniques are becoming increasingly attractive to power-supply designers because they lead to fewer switching losses and allow you to use smaller components. Part 1 of this 2-part article reviews the classifications and circuits of the various resonant-mode topologies.—*Frederick E Sykes, Gennum Corp*

Limit noise in designs using advanced CMOS logic 215

Advanced CMOS devices made with tight line-width transistors provide greater speed, more drive, and use less power than their precursors. You must design more carefully, however, because the cost of these performance increases is a greater level of device-generated noise.—*William Hall, National Semiconductor and Charles Pace, Compaq Computer*

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EDN®(ISSN 0012-7515) is published 49 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Pubiishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Senior Vice President/General Manager, Boston Division; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. POSTMASTER: Send address corrections to EDN® at the Denver address. EDN® copyright 1989 by Reed Publishing USA; Ronald G Segel, Chairman and Chief Executive Officer; Robert L Krakoff, President and Chief Operating Officer; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $105/year; Canada/Mexico, $125/year; Europe air mail, $150/year; all other nations, $150/year for surface mail and $230/year for air mail. Single copies are available for $10. Please address all subscription mail to Eric Schmierer, 44 Cook Street, Denver, CO 80206-5800.

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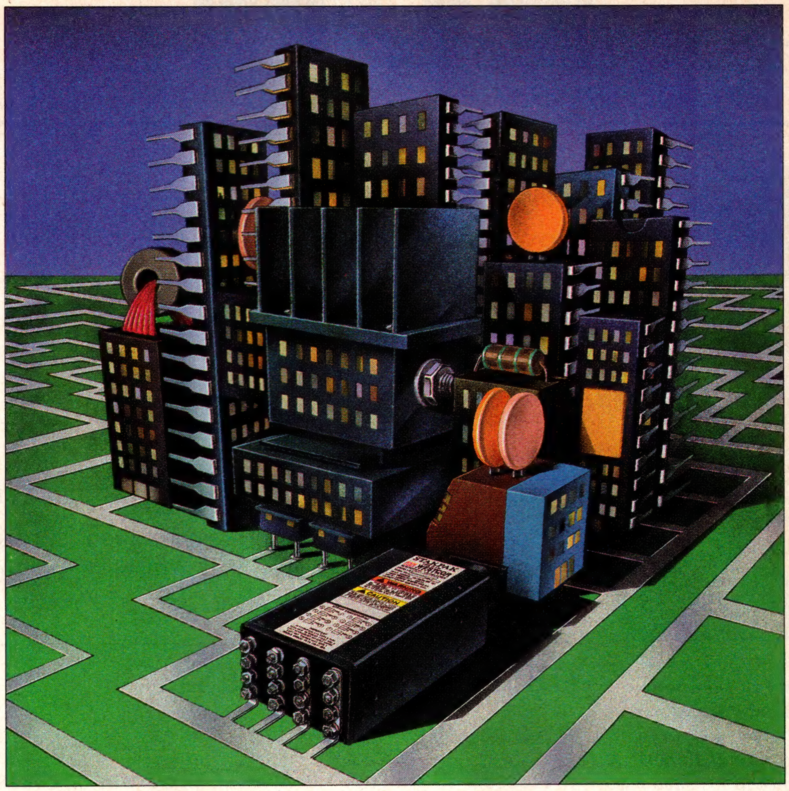

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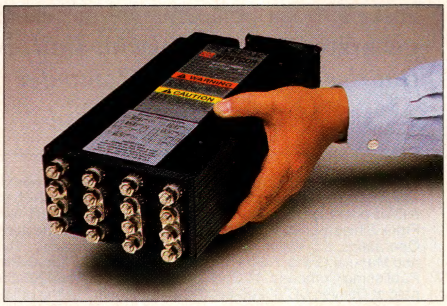

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SP1-1802	5 @ 240				
SP1-1803	12 @ 100				
SP1-1804	15 @ 80				
SP1-1805	24 @ 50				
SP1-1806	28 @ 42				
SP1-1807	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

Total output power may not exceed 1200 watts for any model, single or multiple output. Lower power StakPak models are available. Please contact the factory.

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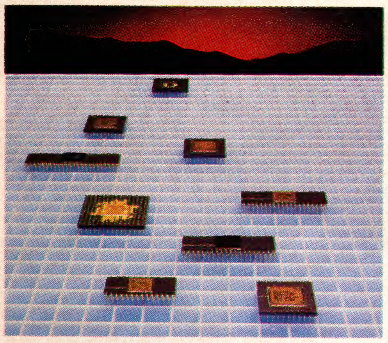

***A direct digital synthesizer** is a useful tool in spread-spectrum communications and arbitrary-waveform generation. Recent technology advances, however, have broadened the device's usual application territory (pg 95).*

Hands-on experience paves the way for future MCA designs 233

The advent of the IBM Micro Channel Architecture (MCA) represents performance and architectural improvements compared with the earlier PC/AT bus. But designing for the PS/2 is a tougher challenge than designing for the PC/AT.—*Tom Darbonne, Vinita Singhal, and Mike Webb, Altera Corp*

Message protocol unloads VMEbus processors 255

Integrating VMEbus boards made by different manufacturers can be a daunting task. To lighten the burden, manufacturers and systems engineers should adopt a simple, uniform way to exchange information between VMEbus boards. The MPP (message-passing protocol) is one such method.—*J H Brand and L de Graaf, Compcontrol BV*

TECHNOLOGY UPDATES

Surface-mount-technology update: Fine-pitch SMT needs shrewd pc-board design 77

Despite their frustrating package diversity, the need for increased circuit density and device pin count will probably force you to incorporate fine-pitch, surface-mount devices in your next design.—*Richard Quinnell, Regional Editor*

Object-oriented programming: Objects facilitate modular, reusable code 85

Object-oriented programming techniques are by no means new, but it's only in the last three or four years that compiled object-oriented languages have become available. Both are starting to change the way designers think about data structures for complex systems.—*Chris Terry, Associate Editor*

Direct digital synthesizers: Devices refine the art of frequency synthesis 95

Direct digital synthesizers (DDSs) offer many advantages over their PLL counterparts. If you need a frequency synthesizer that has switching speeds in the nanoseconds and can achieve a frequency resolution of a fraction of a hertz, a DDS is for you. —*John A Gallant, Associate Editor*

Continued on page 9

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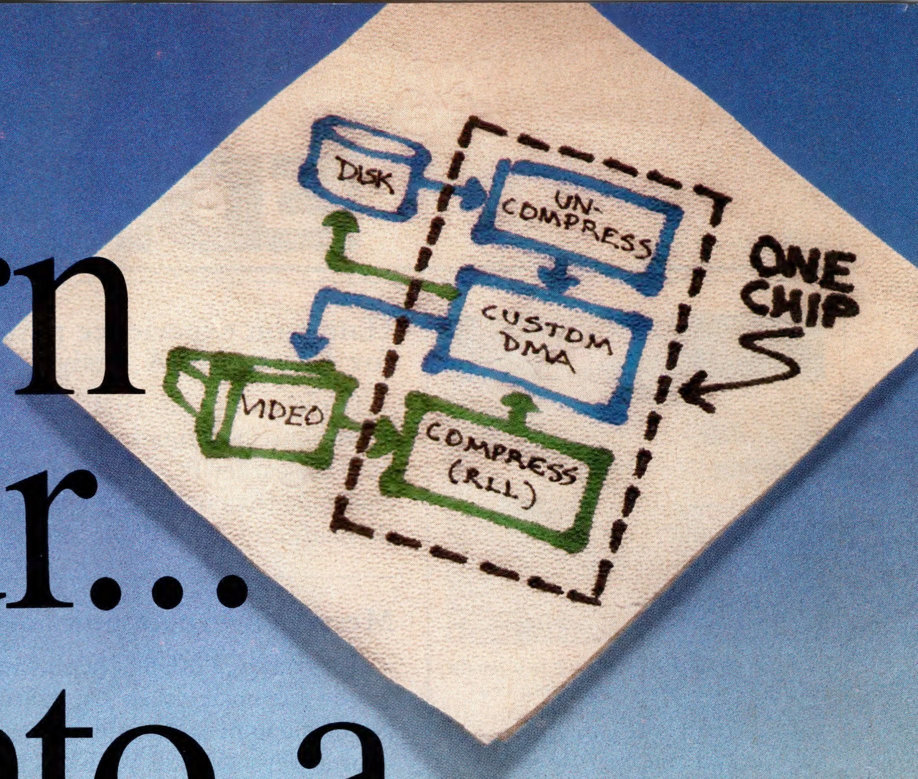

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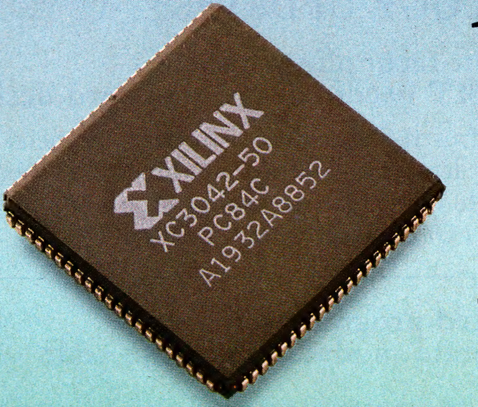

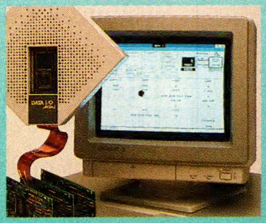

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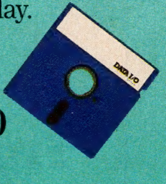

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November 9, 1989

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Engineers should be proud of the recent *Voyager 2* mission to the outer planets. As the spacecraft journeys out of the solar system, it remains a testament to engineering.

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Raymond Kurzweil and the second Industrial Revolution.
—*Jay Fraser, Associate Editor*

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Drill of the year.

When *Popular Science* reviewed new power tools, many were good. In fact, even great. But one of them stood out above all the others. The Porter-Cable Model 9850. A professional cordless driver/drill—driven to perfection by a rechargeable battery from Gates Energy Products.

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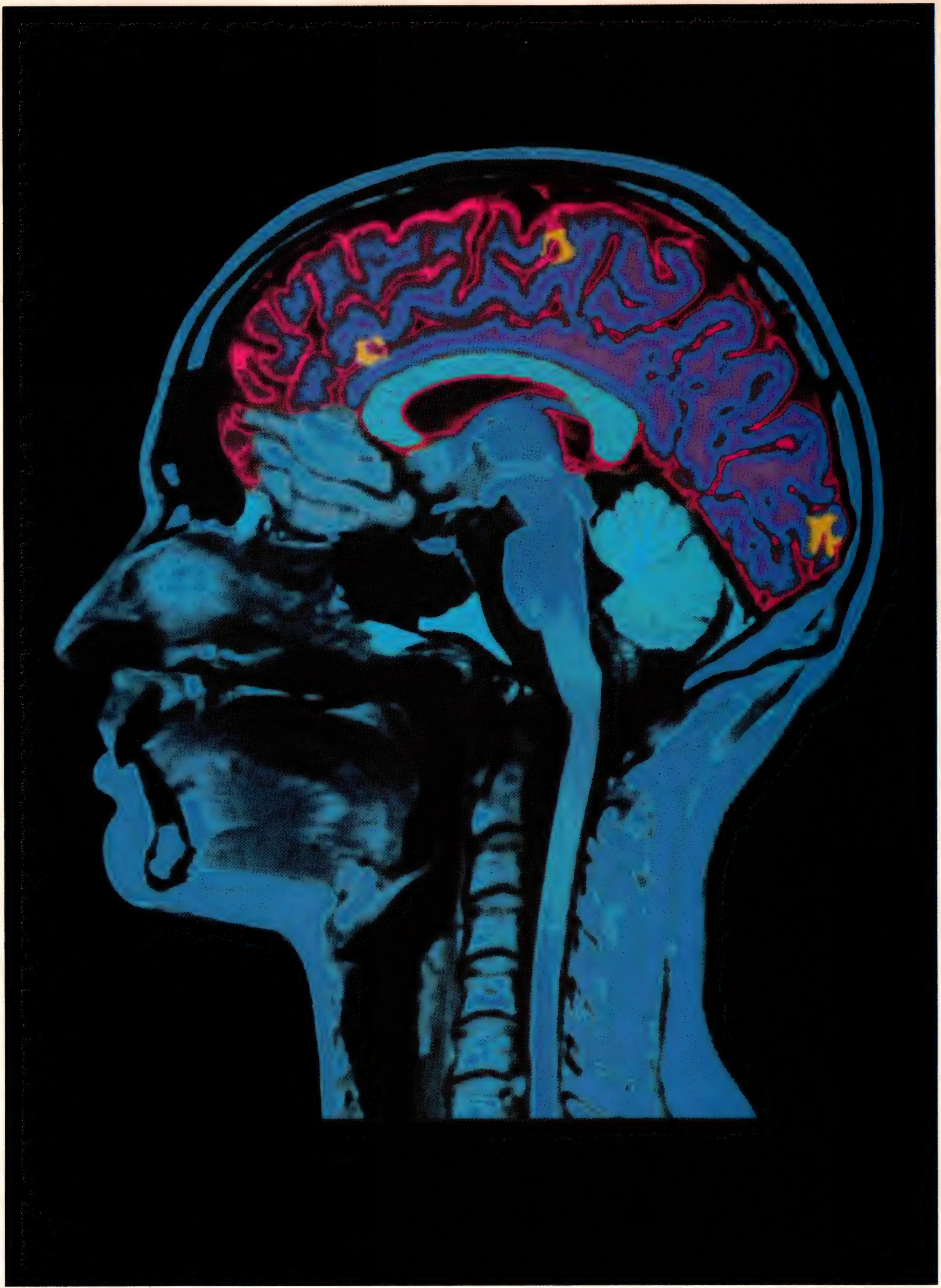

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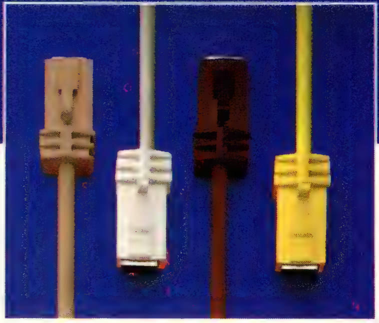

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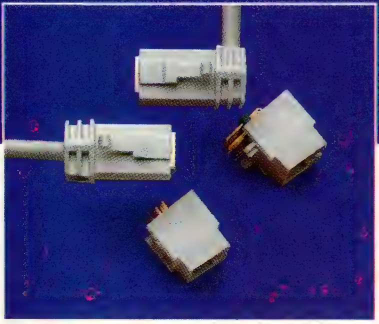

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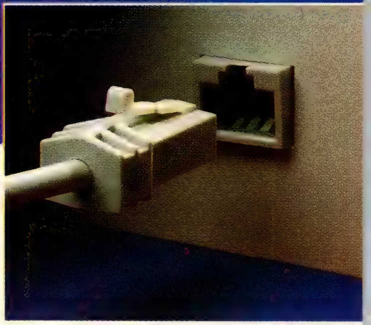

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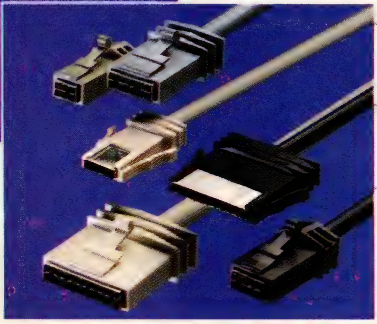

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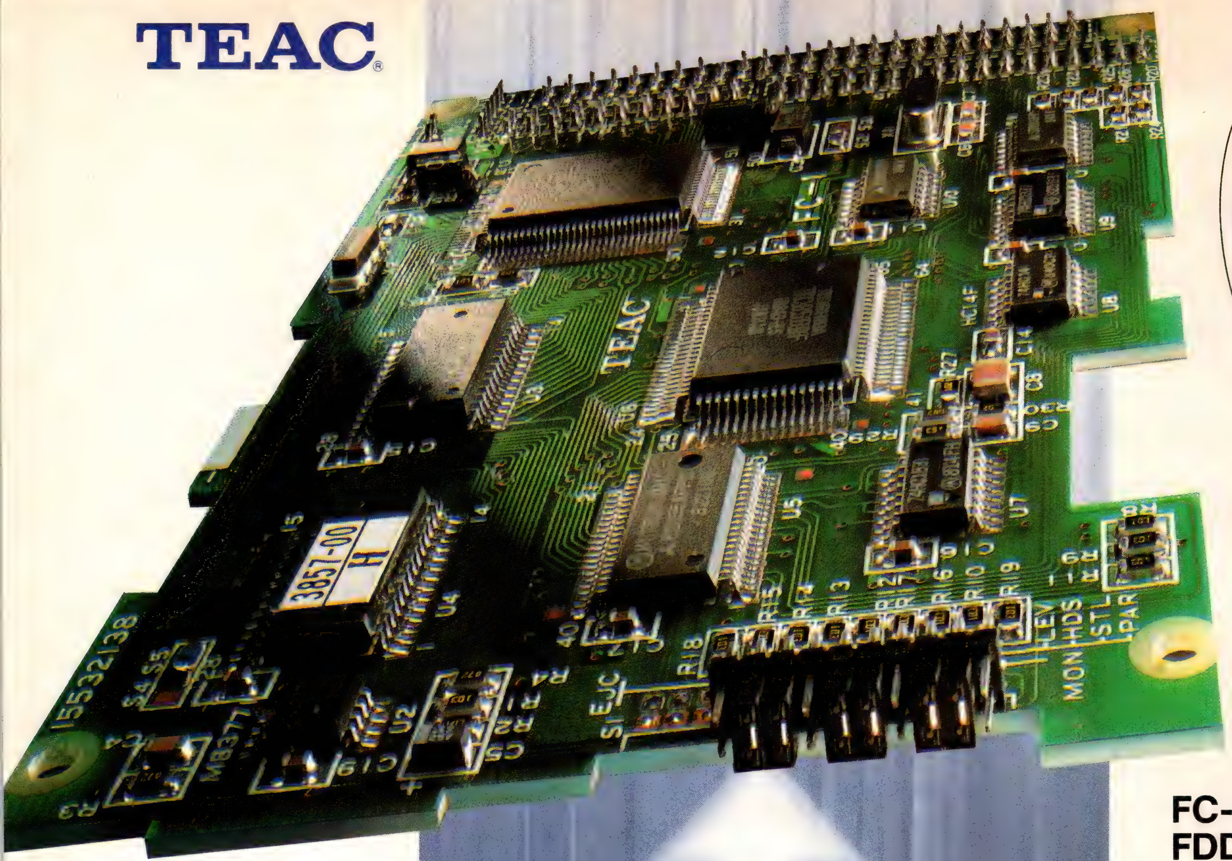

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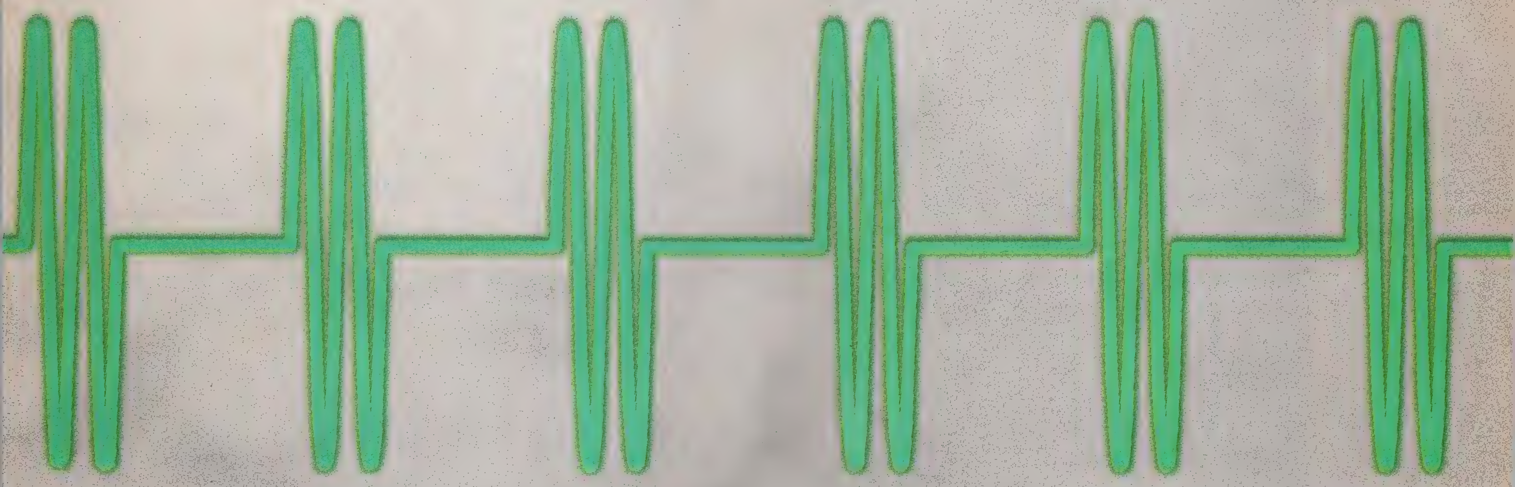

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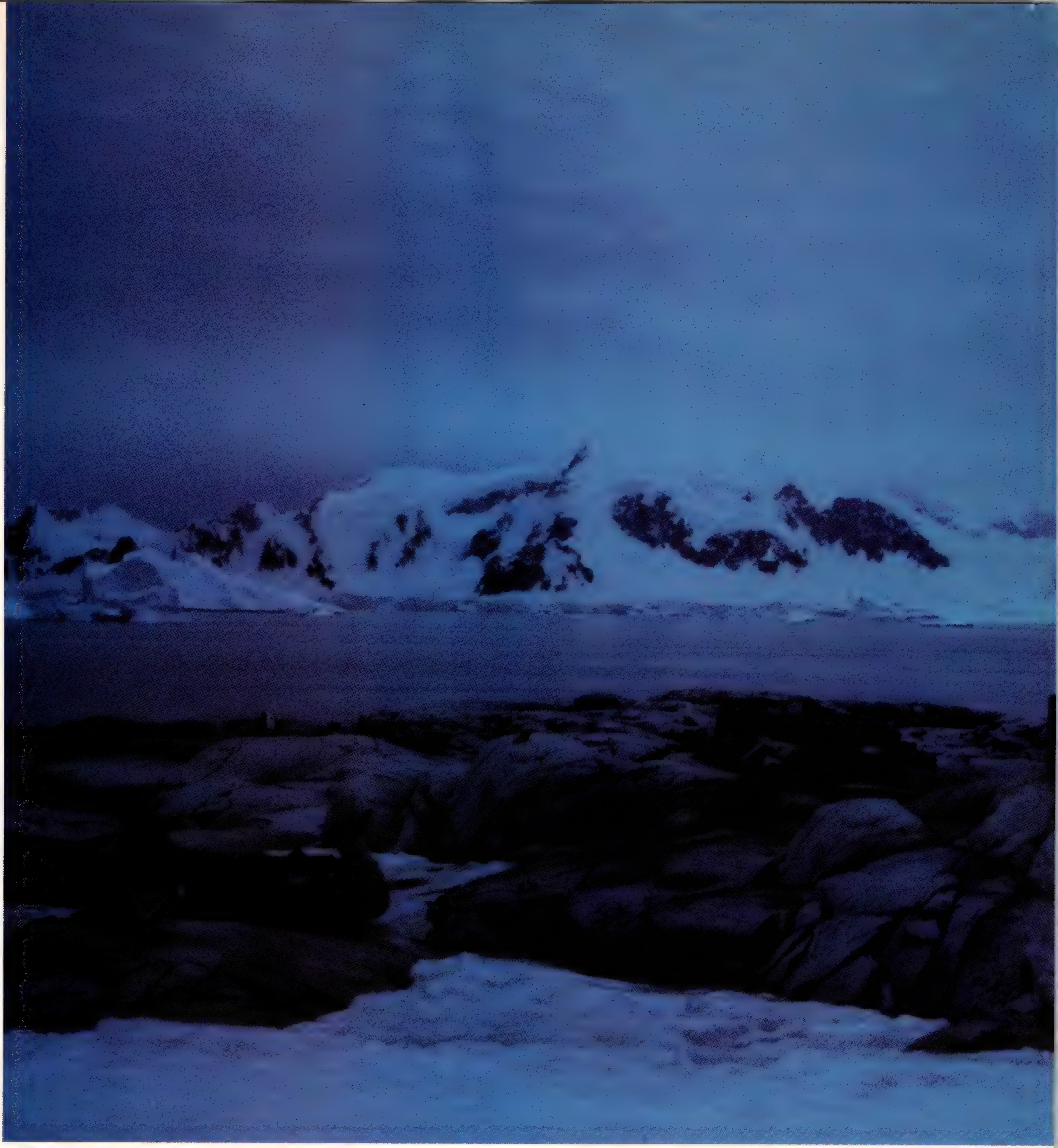

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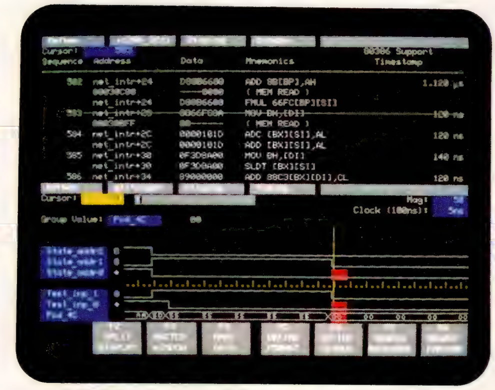

```
Cursor:                                          80386 Support
Sequence  Address        Data       Mnemonics                 Timestamp
   502    net_intr+24    D0006600   ADD 0B[BP],AH              1.120 µs
          00030C00       ----0000   ( MEM READ )
          net_intr+24    D0006600   FMUL 66FC[BP][SI]
   503    net_intr+28    0066F08A   MOV BH,[DI]                 120 ns
          000300FF       00------   ( MEM READ )
   504    net_intr+2C    0000101D   ADC [BX][SI],AL             120 ns
          net_intr+2C    0000101D   ADD [BX][SI],AL
   505    net_intr+30    0F3D0A00   MOV BH,[DI]                 140 ns
          net_intr+30    0F3D0A00   SLDT [BX][SI]
   506    net_intr+34    89000000   ADD 8BC3[BX][DI],CL         120 ns
Cursor:                                                Mag:
                                              Clock (100ns):
Group Value:               00
```

Split screen displays can show microprocessor activity time correlated with high-speed timing data (above) or disassembly of another microprocessor. The cursors can be locked to scroll in parallel, highlighting data nearest to the same point in time.

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NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

CMOS SINGLE-CHIP U TRANSCEIVER DISSIPATES 290 mW

Siemens (Santa Clara, CA, (408) 980-7912) has developed a single-chip echo-cancellation circuit for ISDN functions. The PEB 2091 features a 2-wire transceiver for full-duplex data transmission and reception at the U reference point in accordance with the layer 1 specification of the American Standard of Telecommunication. The device consists of three main blocks. The line-interface unit contains the crystal oscillator and all the analog functions. System-interface-unit features include activation and deactivation procedures and timing recovery. The receiver performs digital filtering. The device features a 144k-bps user bit rate, an 80k-baud transmission rate, adaptive echo cancellation and equalization, a wake-up unit for activation from the power-down state, a transmission range of 9.5 km with #26 AWG wire, and power dissipation of 290 mW. The device also supports the second revision of Siemens's standard bus architecture, the IOM (ISDN Oriented Modular) bus. The 44-pin plastic leaded-chip carrier will be available in production quantities in December for $60 (5000).—Anne Watson Swager

SYNTHESIS TOOLS GET ENHANCED TIMING ALGORITHMS

Using an improved algorithm, the Design Compiler Version 1.2 from Synopsys (Mountain View, CA, (415) 962-5000) generates circuits that the company claims are 8% faster and 8% smaller than those generated by previous versions of the software. Accompanying these improvements in speed and area is a 50% reduction in software runtime. The Design Compiler Version 1.2 also has a state-machine optimization capability. The software that performs state-machine optimization also analyzes your state table—in either Verilog or VHDL or extracted from a netlist—and automatically chooses an optimized state assignment. The Design Compiler costs $35,000 and runs on Apollo, DEC, and Sun workstations.—Michael C Markowitz

READ/WRITE CACHE BUFFER REPLACES 17 ICs

The LR3220 read-write buffer from LSI Logic Corp (Milpitas, CA, (408) 433-8000) provides buffered read/write operations between a 32-bit µP and memory. Although intended primarily for use in systems based on the MIPS R3000 µP, the buffer chip can also operate in a Harvard mode. In the R3000 mode, the buffer chip matches the µP's address- and control-line timing by latching half of the address on one clock edge and the other half on the next edge. In Harvard mode, the buffer chip latches the entire address on the clock's rising edge. These modes affect only memory-write operations. The chip also supports fast-page-mode write operations to 1M-bit dynamic RAMs. The LR3220 replaces four of the company's LR3020 write-buffer chips plus some glue logic and increases the write-buffer depth of such a design from four to six words. The 25-MHz version costs $161.50 in a 180-pin ceramic pin grid array and $139 (100) in a 184-lead plastic quad flatpack.—Steven H Leibson

SINGLE-CHIP AT CONTROLLER REDUCES MOTHER-BOARD SIZE

Chips and Technologies (San Jose, CA, (408) 434-0600) has announced a single-chip IBM PC/AT and compatibles system controller, the 82C235, with which you can build a mother board using 14 additional components plus memory. A typical 82C235-based system contains a single 80286 µP, one 82C235 VLSI logic chip, one keyboard controller, one EPROM, 10 inexpensive TTL components, and memory. The 82C235 supports

8-, 10-, and 12.5-MHz clock rates at zero wait states, and a 16-MHz clock rate with one wait state. The chip includes bus control logic, a built-in math coprocessor, and an 80287 interface, and provides memory control for as many as 16M bytes. The chip also supports shadow RAM and an 8- or 16-bit BIOS. The 82C235 is compatible with the company's VGA controller, I/O controller, and floppy-disk-drive controller, so you can also use it in a fully featured 80286 system. Samples of the 160-pin chip in a plastic flatpack are available now; production quantities will be available in the first quarter of 1990 for $46 (1000).—Anne Watson Swager

COMDEX PUSHES COMPUTER AND PERIPHERAL STATE OF THE ART

Although vendors of 5¼-in. quarter-inch-cartridge tape drives have started shipping 300M-byte drives and talk about a 1G-byte drive, vendors of data cassette and digital-audio tape drives offer higher capacity products in the 3½-in. form factor now. Teac America (Montebello, CA, (213) 726-0303) offers the MT2ST/F data cassette drive that stores 600M bytes with no data compression. The drive stores data on 21 tracks across the 0.15-in. tape at 38,400 bpi. The drive transfers data at 242k bytes/sec and includes a choice of SCSI or QIC-02 interfaces. The company will ship the $550 (1000) drive in the first quarter of 1990.

Archive Corp (Costa Mesa, CA, (714) 966-4772), meanwhile, announced its Python family of digital-audio tape drives based on a 3½-in. mechanism. The mechanism was designed from the ground up for data storage and is not a reworked entertainment-grade product, as many early digital-audio tape drives were. The drives offer an MTBF of 20,000 power-on hours at a 20% duty cycle. The Python drives comply with the Manufacturers Group digital-data-storage standard for digital-audio tape drives and store 1.3G bytes. The drives include a basic nonintelligent interface; the company offers a SCSI controller, which also fits on the drive in a 5¼-in. arrangement, for off-drive mounting. The company will ship the drives in the first quarter of 1990 at a price of less than $1500 (100) for the basic interface.

Winchester disk drives ranging in size from 2½ to 8 in. were also announced at Comdex. The MD-2050 2½-in. disk drive from Areal Technology (San Jose, CA, (408) 954-0360 offers a formatted capacity of 50M bytes. Targeting battery-powered applications such as notebook computers, the 4.8-oz drive consumes only 950 mW during operation and only requires a 5V power source. The drive features an average access time of less than 29 msec. The company plans to ship the drive in the first quarter of 1990 at a cost of $595 (OEM quantities).

Western Digital (Irvine, CA, (714) 474-2033) introduced an 80M-byte, 3½-in. disk drive with an embedded-AT interface. The AC280 costs about $500 (100,000) and will be shipped in December or January. The drive offers an average seek time of 19 msec and transfers data at a minimum rate of 800k bytes/sec.

Hewlett-Packard, Imprimis, Maxtor, and Micropolis all introduced 5¼-in. drives that store more than 1G byte prior to Comdex, but Imprimis (Minnetonka, MN, (612) 936-6267) also showed that there is life left in larger form factors by introducing a new 8-in. drive. The Imprimis Sabre 2500 offers a capacity of more than 2G bytes and an average seek time of 13 msec. You can choose from SMD-E, (Storage Module Device) IPI-2 (Intelligent Peripheral Interface), and SCSI interfaces for the product;

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all interfaces support a transfer rate of 3M bytes/sec. The drive has a 100,000-hour MTBF spec, uses thin-film heads and media, and costs $6595 (OEM quantities).

Micro Channel Architecture (MCA) and IBM PC/AT-compatible token-ring LAN-adapter boards from Western Digital (Irvine, CA, (714) 474-2033) can act as bus masters. The WD8000 family of boards support types 1, 2, and 3 token-ring cables and cost between $600 and $1000. The IBM PC/AT bus does not fully support arbitrated bus mastering but does let these boards perform first-party DMA transfers. The MCA token-ring board will be among the first to support the much discussed bus-master capability of the MCA bus and should fit nicely in a system with bus-master SCSI adapters from Western Digital or Adaptec (Milpitas, CA, (408) 946-8600).

. Lastly, the FPF8060HRUK plasma display from Fujitsu Component (Santa Clara, CA, (408) 562-1000) supports three text and six graphic gray-scale modes of the IBM VGA standard. A Paradise Systems standard VGA card can drive the display via its Feature Connector. The display features a 640×480-pixel resolution and a 10½-in.-diagonal screen, and costs $1099. Fujitsu also offers monochrome and color LCD flat-panel displays, some of which incorporate touch screens.—Maury Wright

μPs AVAILABLE TO 883C CLASS B

The 80C286/883 and the RTX-2000GM-8/883 microprocessors from Harris Semiconductor Military and Aerospace Div (Melbourne, FL, (407) 724-3800) both meet the quality conformance requirements of MIL-STD-883, method 5005, which includes electrical, mechanical, life, and packaging tests. The 80C286/883 costs $603.90 for a 10-MHz version and $713.90 for a 12-MHz version; delivery is 16 weeks ARO. The RTX-2000GM-8/883 costs $995; delivery is 17 weeks ARO.—Michael C Markowitz

5-PORT REGISTER IC PROVIDES 8-nSEC ACCESS TIMES

Organized as 64 18-bit registers, the B2210A, B3210A, and B5210 register-array ICs from Bipolar Integrated Technology Inc (Beaverton, OR, (503) 629-5490) provide 5-port access in as little as 8 nsec, and each of the five ports is independently addressable. The B3210A has TTL-compatible I/O ports and a 12.5-nsec access-time rating. The B2210A and B5210 have ECL-10KH-compatible I/O ports and feature the faster 8-nsec access-time rating. The company specifically designed the B5210 as a companion part to its ECL SPARC μP. All three devices cost $190 (1000).
—Steven H Leibson

WORKSTATIONS READ DATA FROM CD-ROMs

Adding its name to the growing list of CD-ROM supporters, Sun Microsystems Inc (Mountain View, CA, (415) 960-1300) has added the SunCD Pack to its catalog of options for the SPARCstation 1. The SunCD Pack is an external, 5¼-in., half-height package that connects to the workstation via a SCSI cable. SunCD can store 644M bytes of data on a single-sided disk. The SunCD software is contained within SunCD Pack and lets any user on a network share databases and application software via Sun Microsystems' Network File System. The software supports the International Standards Organization's 9660 file-system format for CD-ROMs. The SunCD Pack costs $1500; delivery is 30 days ARO. On a related note, Meridian Data Inc (Scotts Valley, CA, (408) 438-3100) is designing a CD-ROM developer's system for the SPARCstation 1.—Michael C Markowitz

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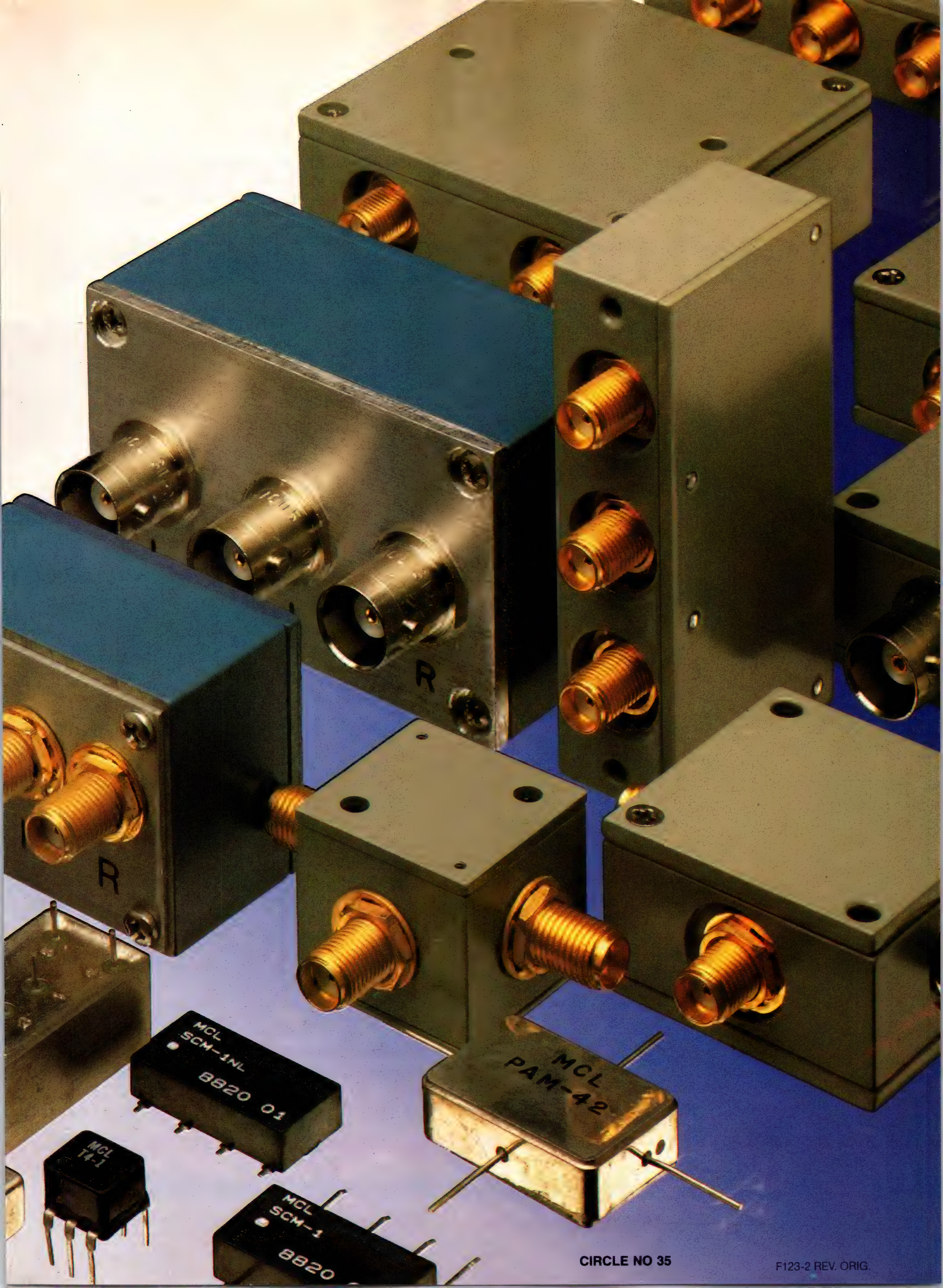

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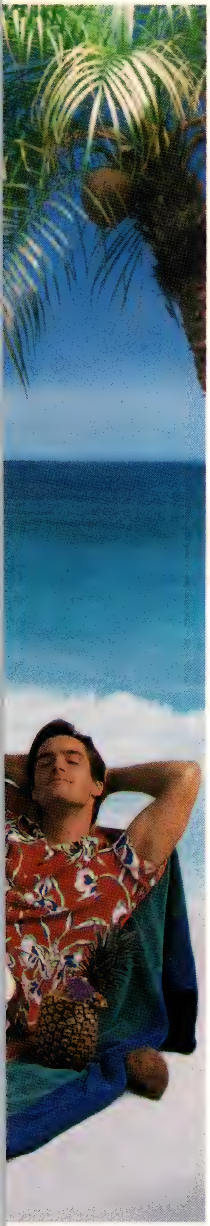

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Experienced ASIC team at your service

Whether you're an ASIC design pro or tackling your first project, Oki's team of experienced design engineers is ready to assist you. We understand the pressures you're under. And we'll help you shorten development time, improve testability and manufacturability, and achieve first-time design success. We'll work with you to optimize your circuits or develop special cells. From start to finish, we'll do whatever it takes to help you succeed.

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Oki has a full set of powerful mainframe design tools which ensure that your design will work, be efficient to manufacture, and perform reliably: logic, timing and fault simulations, automatic layout, detailed checking of design rules, and automatic test program generation. We support many popular workstations. Our large cell library includes many highly complex macrofunctions.

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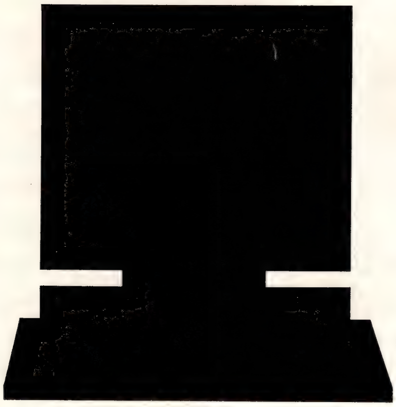


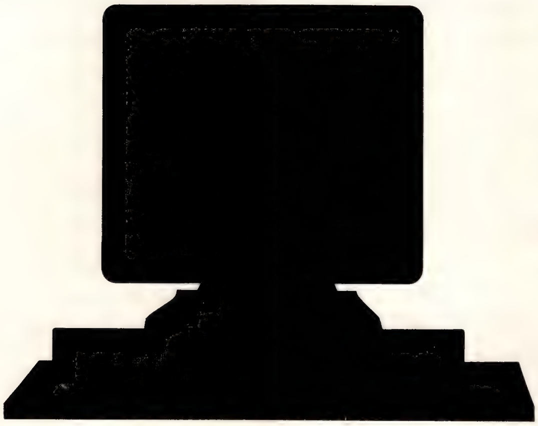
SUN

No POSIX compliance

No symmetric multiprocessing

No commercial-grade file system

No system under $700/MIPS



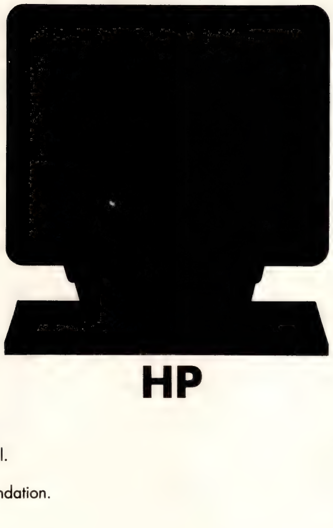
DEC

No symmetric multiprocessing currently available

No system under $700/MIPS

No multi-vendor binary compatibility

No open I/O bus across product line



HP

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No POSIX compliance

No desktop RISC system

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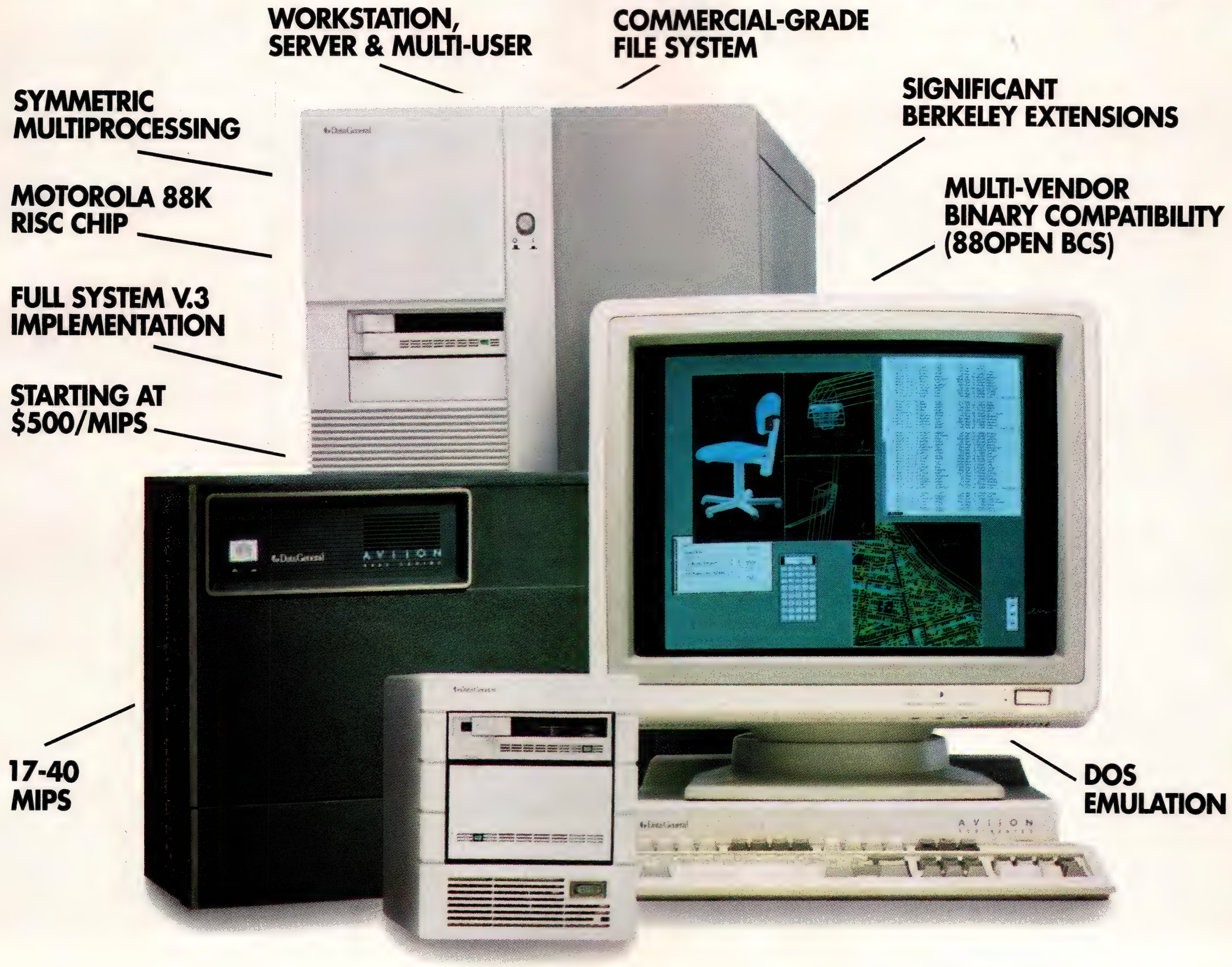
VS. UNIX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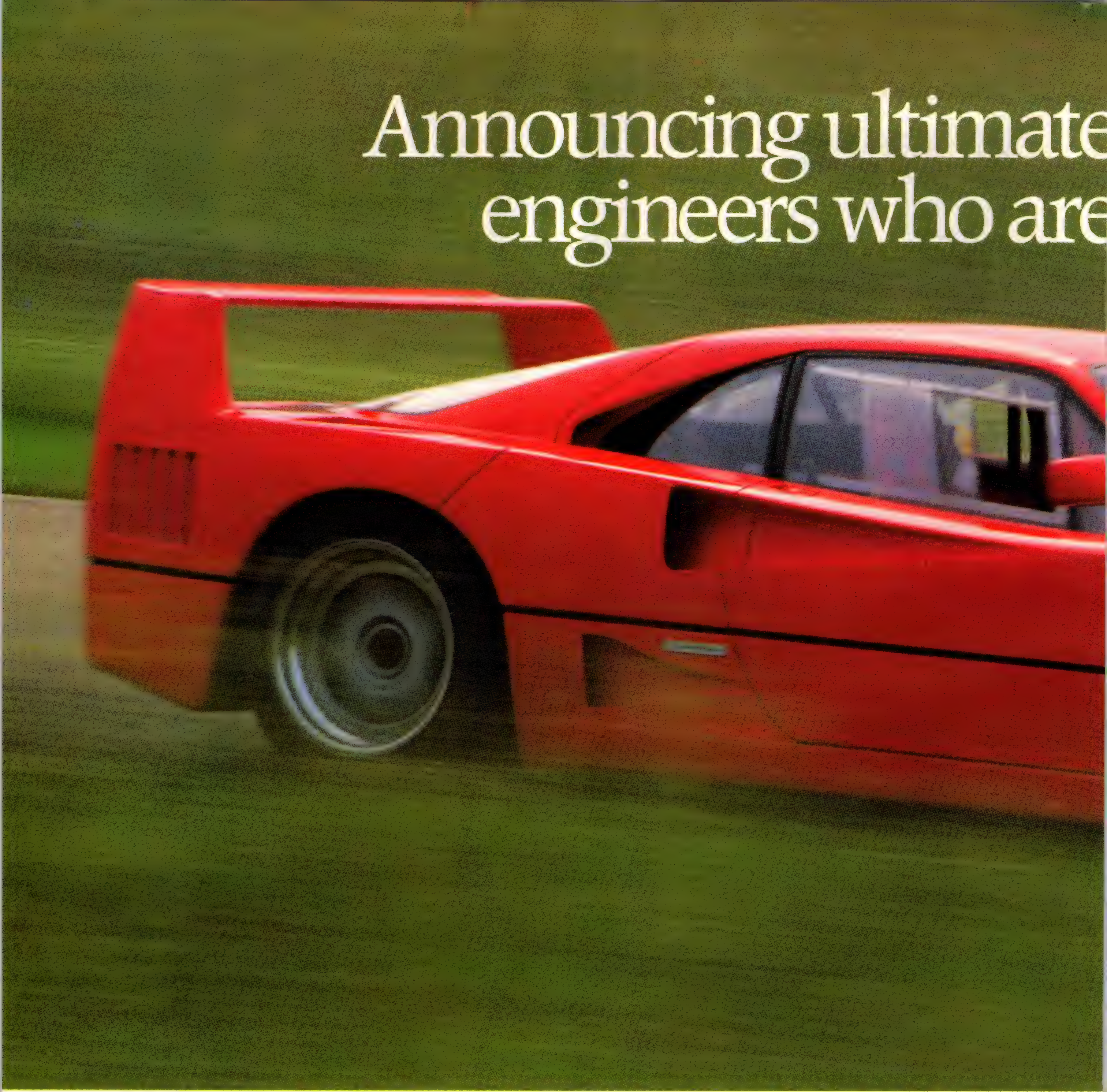

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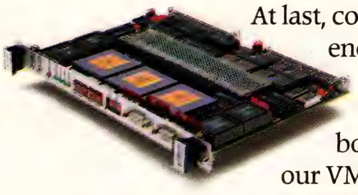

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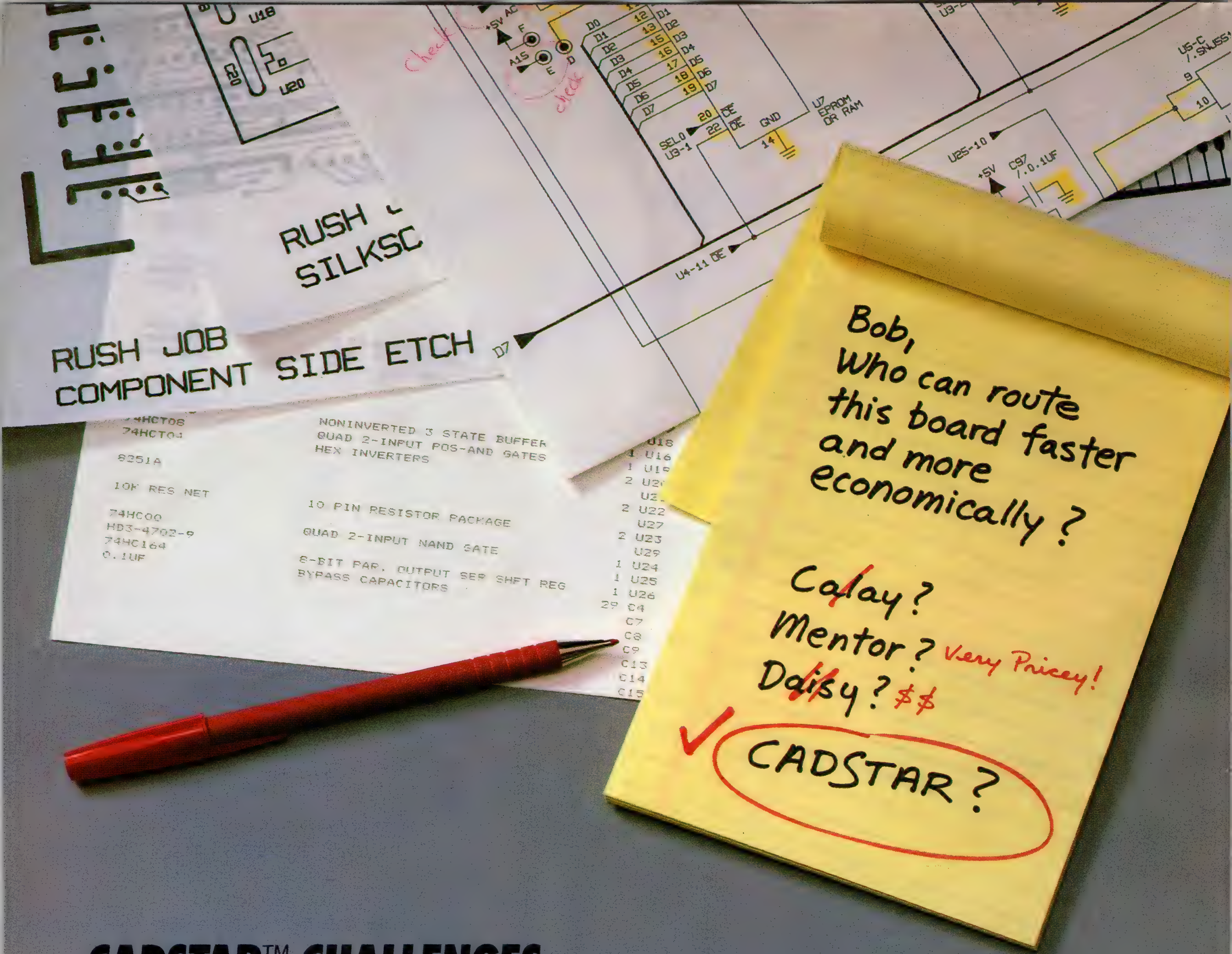

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TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Beyond VGA

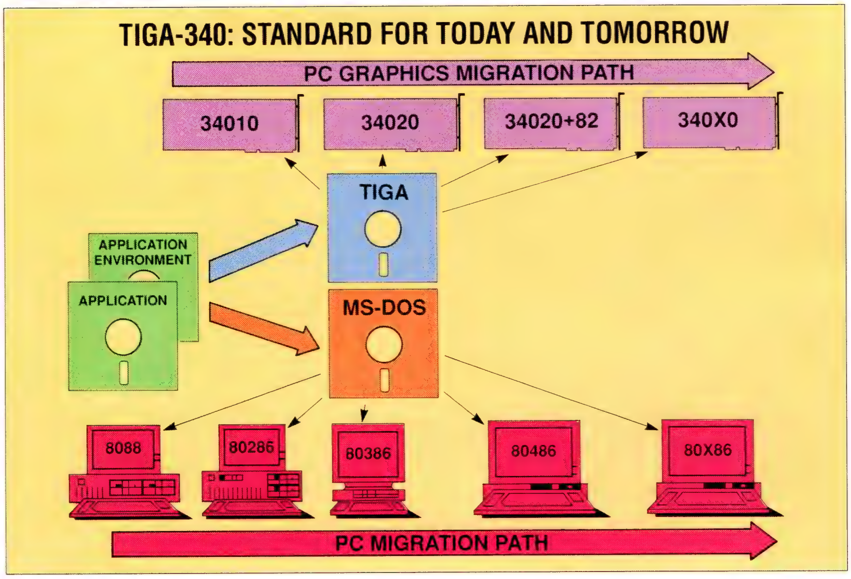
IN THE ERA OF

MegaChip□
TECHNOLOGIES

TIGA-340 from Texas

The open graphics interface standar a clear path for your future.

A ground swell of support is rallying behind TIGA-340™, the Texas Instruments Graphics Architecture. It and TI's TMS340 family are poised to become the next standard beyond VGA as PC users demand higher performance and resolution.



Just as MS-DOS® allows applications to run on any MS-DOS PC using 80X86 processors, TIGA allows graphics applications to run on any TIGA display system using a 340X0 processor.

The PC graphics standard anyone can use

TIGA™ is a high-performance software interface that optimizes communications between industry-standard 340 family processors and the PC host processor.

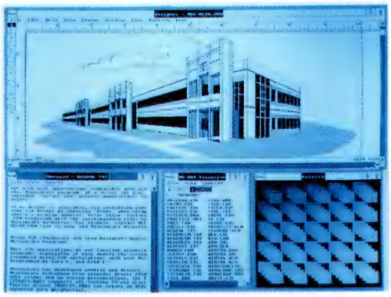
With TIGA, hardware and software specifications for a PC graphics standard are open and available from inception — one of the reasons why more than 100 companies have already made plans to evaluate TIGA-compatible hardware and software products.

Lowest cost, highest performance

TIGA's move into the mainstream is being fueled by the price of TMS34010-based boards falling to well below $1,000. In fact, TI's 34010 processor is the most economical way to implement high-performance 1024 x 768 resolution PC graphics boards. The faster speed and greater throughput of the second-generation 34020 result in even higher performance boards.

Clear migration path

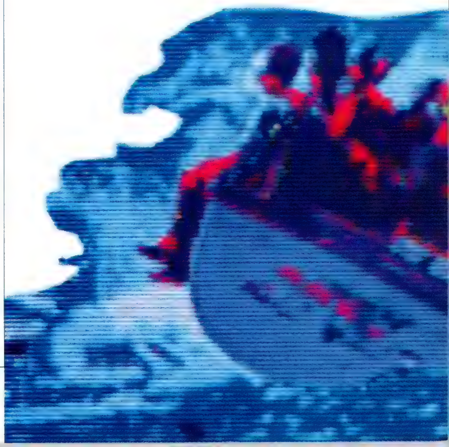
TIGA provides a common platform upon which graphics applications can take advantage of the processing power of the TMS340 family.



Software developers no longer have to rewrite code in order to migrate to higher performance hardware. Software applications that run through TIGA on the 34010 processor run on the upward-compatible 34020 as well as on future 340 family members.

Hardware developers benefit from wide software support, reduced system development time and costs, and easy differentiation of products.

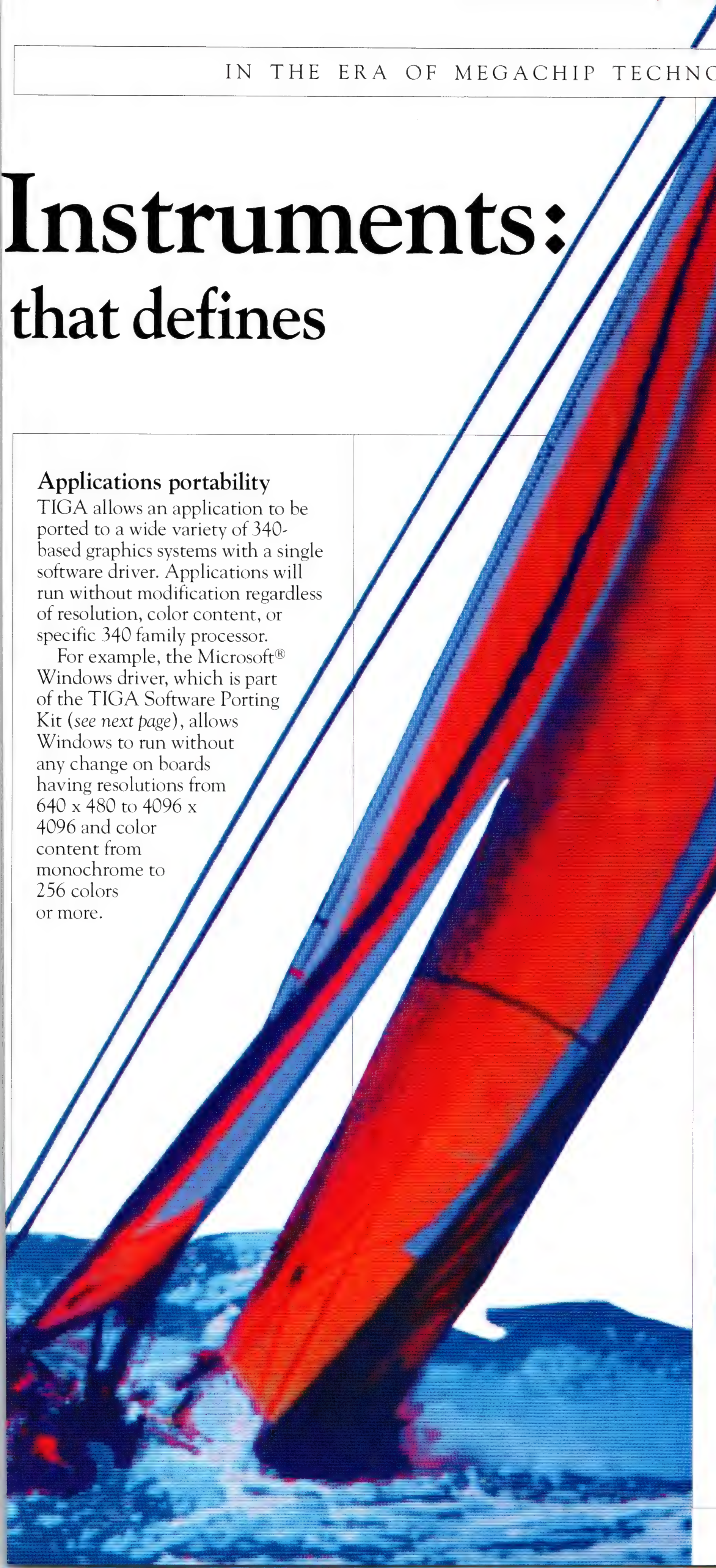
At present, TIGA supports DOS-based PCs, with UNIX™ and OS/2 forthcoming.



IN THE ERA OF MEGACHIP TECHNOLOGIES

Instruments:

that defines



Applications portability

TIGA allows an application to be ported to a wide variety of 340-based graphics systems with a single software driver. Applications will run without modification regardless of resolution, color content, or specific 340 family processor.

For example, the Microsoft® Windows driver, which is part of the TIGA Software Porting Kit (*see next page*), allows Windows to run without any change on boards having resolutions from 640 x 480 to 4096 x 4096 and color content from monochrome to 256 colors or more.

Speeds time to market

Now hundreds of popular applications can be made available for your new graphics product almost instantly using TIGA and Microsoft Windows. Porting TIGA to a 340-based board typically takes less than one man-week of effort.

More than 150 OEMs have made the TMS340 graphics family their own. That wide acceptance, coupled with open architecture and a defined migration path, makes the future for TIGA-340 and the TMS340 family rich and promising.

A PERSPECTIVE ON GRAPHICS INTERFACE STANDARDS

TI's leadership TMS340 graphics family

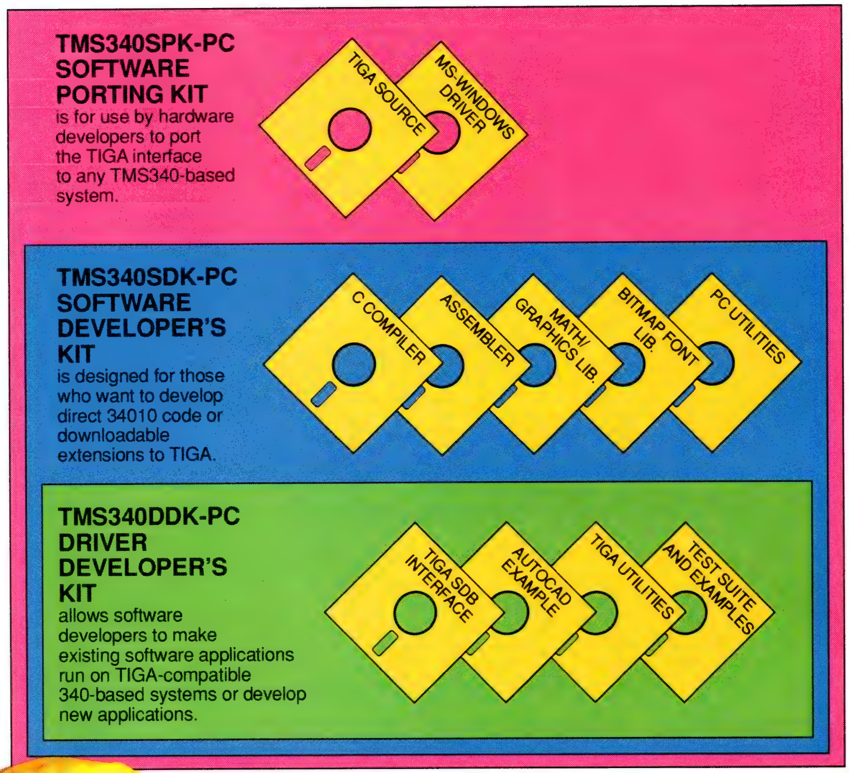
No other supplier comes close to TI in the range of cost/performance options for the development of integrated graphics solutions. The widely used TMS34010 processor and other family members are now being joined by a group of new-generation products that will bring the higher levels of workstation performance to PCs.

Chief among these is the TMS34020, a programmable, 32-bit processor up to 20 times faster than the 34010.

For use with the 34020, the TMS34082 will perform floating-point operations up to 100 times faster than current PC coprocessors. It is the industry's first graphics floating-point coprocessor.

The family's video RAMs, invented by TI, have been augmented by the TMS44C251 1-megabit VRAM. It was designed in conjunction with the 34020 for the high system bandwidths demanded by today's mid- and high-resolution graphics systems.

TIGA-340 DEVELOPMENT KITS



TMS340SPK-PC SOFTWARE PORTING KIT is for use by hardware developers to port the TIGA interface to any TMS340-based system.

TMS340SDK-PC SOFTWARE DEVELOPER'S KIT is designed for those who want to develop direct 34010 code or downloadable extensions to TIGA.

TMS340DDK-PC DRIVER DEVELOPER'S KIT allows software developers to make existing software applications run on TIGA-compatible 340-based systems or develop new applications.

Free user's guide

For more information about the TIGA-340 standard, get your free copy of the *TIGA-340 Interface User's Guide* and the *TIGA-340 Interface Brochure*.

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TEXAS INSTRUMENTS

SIGNALS & NOISE

Reader offers help and asks for help

May I add my thanks to Bob Pease for his excellent series of articles on troubleshooting analog circuits? In return, may I offer him a little help on how to connect LEDs the right way (see EDN, Aug 3, 1989, pg 132).

An LED is a diode and so has its cathode end marked. How do [manufacturers] mark a diode without printing on it? Either by cutting the cathode lead short or by [molding] a flat [spot] on the case next to [the cathode]. The point is that [designers don't] have to especially remember which lead is which. [The diode polarity] is marked in [much the same way as you would do it using] paint or a marker pen. Once I realized this method was logical I found it was easy [to remember], and it has worked for me for the past several years.

Bob mentioned the effects of the turn-on time of clamping diodes. I have a problem with clamping diodes with which some of your readers may be able to help. I need to clamp current pulses of around 200A lasting a few hundred nanoseconds, with a repetition rate of 7 kHz. Although the mean current is less than 100 mA, the "killer" is the turn-on di/dt of 2 to 3A/nsec. Conventional fast rectifier diodes are unable to cope with this [rate of current rise]. Bob was worried by the odd ½V. That's nothing—I've seen forward voltage drops of 20 to 40V per diode on a string of diodes during turn-on. It would seem that carriers just cannot be generated fast enough to carry such a rapid rise of current.

The other trifling complication I have is the operating PIV of 15 to 20 kV. When you have to put 35 diodes in series to [withstand] the voltage, you find the scrap bin filling up remarkably fast when you [don't observe the proper precautions. In this unusual application,] "fast" diodes did not appear to [turn on faster] than general-purpose ones—but they did cost more. Turn-on di/dt is something that does not seem to be specified in the average data sheet.

Offering my thanks for all the good articles you have published. Long may they continue.

P Gascoyne
West Hanney, Wantage,
Oxon, UK

(Ed Note: Putting a string of diodes in series to obtain a PIV higher than that of any one member of the string is a tricky business. All the diodes must have the same capacitance and leakage. If they don't, you will overstress the "best" units (those with the lowest capacitance or leakage) and cause them to fail. For this reason, construction of high-PIV diode strings is best left to a vendor who has the requisite test equipment and know-how. The entire string should be encapsulated in a single package to prevent inadvertent separation of the set.)

Little-known fact about coax deterioration

In Part 5 of Robert Pease's troubleshooting analog circuits series (EDN, March 2, 1989, pg 159), he states: "It is a little-known fact that some coaxial cable can degrade just sitting on the shelf. Types whose codes end in "U," such as RG-58U, have an "uncontaminating" outside shield. In contrast, RG-58 might have an outside shield with superior physical characteristics, but it could, over time, degrade the electrical properties of the cable—specifically its UHF attenuation. So, even in something as simple as wire, there may be more problems than meet the eye."

Here is how I would have written that paragraph: "It is a little-known fact that some coaxial cable can de-

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T.C.: 100 PPM/°C.,
10 ohms to 1 Meg.

RNC/RNR —
"S" level in
50, 55, 60, 65
(Char. "H", "J").
Tol.: .1, .5, 1%,
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grade just sitting on the shelf. In the early days the outer jackets of many types of coaxial cable were made from ordinary PVC, containing plasticizer compounds which, experience eventually proved, were causing serious problems. Over time the plasticizer migrated from the jacket and interacted with the shield braid, forming compounds that contaminated the cable and degraded its high-frequency characteristics. The DoD eventually recognized this undesirable situation and revised its specifications for many RG-cable types to call for a "noncontaminating PVC jacket." Using RG/U varieties as examples, RG-58/U and RG-58A/U (both per JAN-C-17A) need not have a noncontaminating PVC jacket, but RG-58C/U and M17/28-RG058 (both per MIL-C-17F) are required to have noncontaminating PVC jackets. (Presence or absence of the /U suffix has no relation to the contaminating or noncontaminating nature of the PVC jacket.) A description such as RG-58 type or RG-58/U type does not imply clear compliance with any DoD requirement. A cable with a contaminating PVC jacket may start out with excellent characteristics and then degrade over the years whether installed or on the shelf. So, even in something as simple as coaxial cable, there may be more problems than meet the eye."

During the late 40s, I remember reels of war-surplus military coaxial cable made before noncontaminating jackets were required. Stripping the jacket revealed shield braid that was greenish from corrosion and greasy from the plasticizer products that migrated to the braid. Our applications weren't critical—we used "good" old UHF connectors—but since we couldn't solder the braid, we had no choice but to throw out the stuff.

The problem was real, and Bob's caveat is historically justified. Without much more than intuition to back up my opinion, I would hazard a guess that [these days] any competent manufacturer would probably have little reason to clutter up its extrusion machinery with contaminating, vinyl-jacket material, and so would be likely to supply noncontaminating material even when there is no specification requirement for it. The danger may still exist, however, in surplus or "no-name" coaxial cable.

Larry Johnson
Los Altos Hills, CA

Keep the candle burning

Your magazine should be commended for the excellent job of keeping the analog candle lighted in the fast-moving digital era. The fading interest in analog circuits will certainly backfire if there is no expertise left to interface the marvels of computer products to the (still) analog world.

I'd like to comment on the article by Steven Hageman (EDN, Sept 1, 1989, pg 117), which brought to focus the important problem of output impedances of power supplies. Simple analysis shows that the analytical expression for the output impedance (Z_{0f}) of a negative feedback system such as a power supply is

$$Z_{0f}=\frac{Z_C \| Z_0}{\left(1+\beta A\,\dfrac{Z_C}{Z_0+Z_C}\right)},$$

where
Z_0=original output impedance,
Z_C=added capacitor impedance,
A=amplifier's gain,
β=feedback ratio.

When

$$\beta A \gg 1,$$
$$Z_{0f}=\frac{Z_0}{\beta A}$$

Considering the above analysis, end users have little chance to change the output impedance of commercial power supplies significantly for the following reasons.

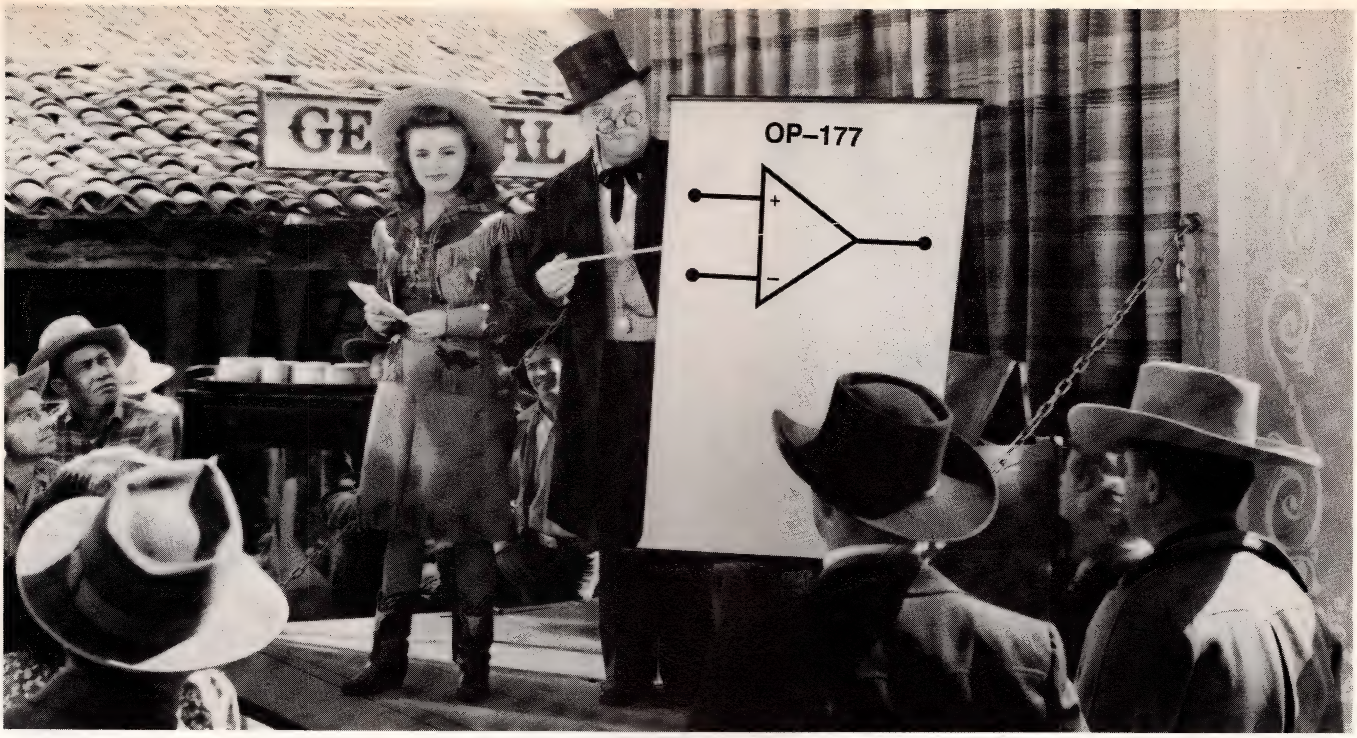
- Within the effective bandwidth of the loop gain (βA), the impedance can be reduced only by increasing the loop gain
- Most if not all commercial power supplies (and certainly switch-mode supplies) will already include output capacitors, so the addition of an extra capacitor to reduce the impedance beyond the effective bandwidth of the loop gain will be like a drop in the bucket. The addition of a very large output capacitor might drastically change the loop performance and cause instabilities as pointed out in Hageman's article.

The only effective remedy I can suggest would be to add an LC section. But this [solution] has its own problems as it might also cause instability of the feedback loop. It appears then that the only safe way to go would be to select (or design) the right power supply for each given application.

Sam Ben-Yaakov
Ben-Gurion University of the Negev
Beer-Sheva, Israel

A misunderstanding

We've received numerous letters from readers complaining that we were using Design Ideas to sell products or help our authors make money. We apologize for any misunderstanding caused by the term "nominal fee" in Thom Van Nguyen's Design Idea "Program generates pseudonoise" (EDN, September 28, 1989, pg 166). For us, nominal fee means "no profit, materials and shipping fees only." His program was simply too long for us to publish, so he agreed to send copies for the cost of the disk. For programs longer than one page, we'll provide address information so you can contact authors directly. Address requests for Thom Van Nyugen's program to his home: 7804 Norcanyon Way, San Diego, CA 92126. Include a floppy disk and a self-addressed stamped envelope.



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CIRCLE NO 58

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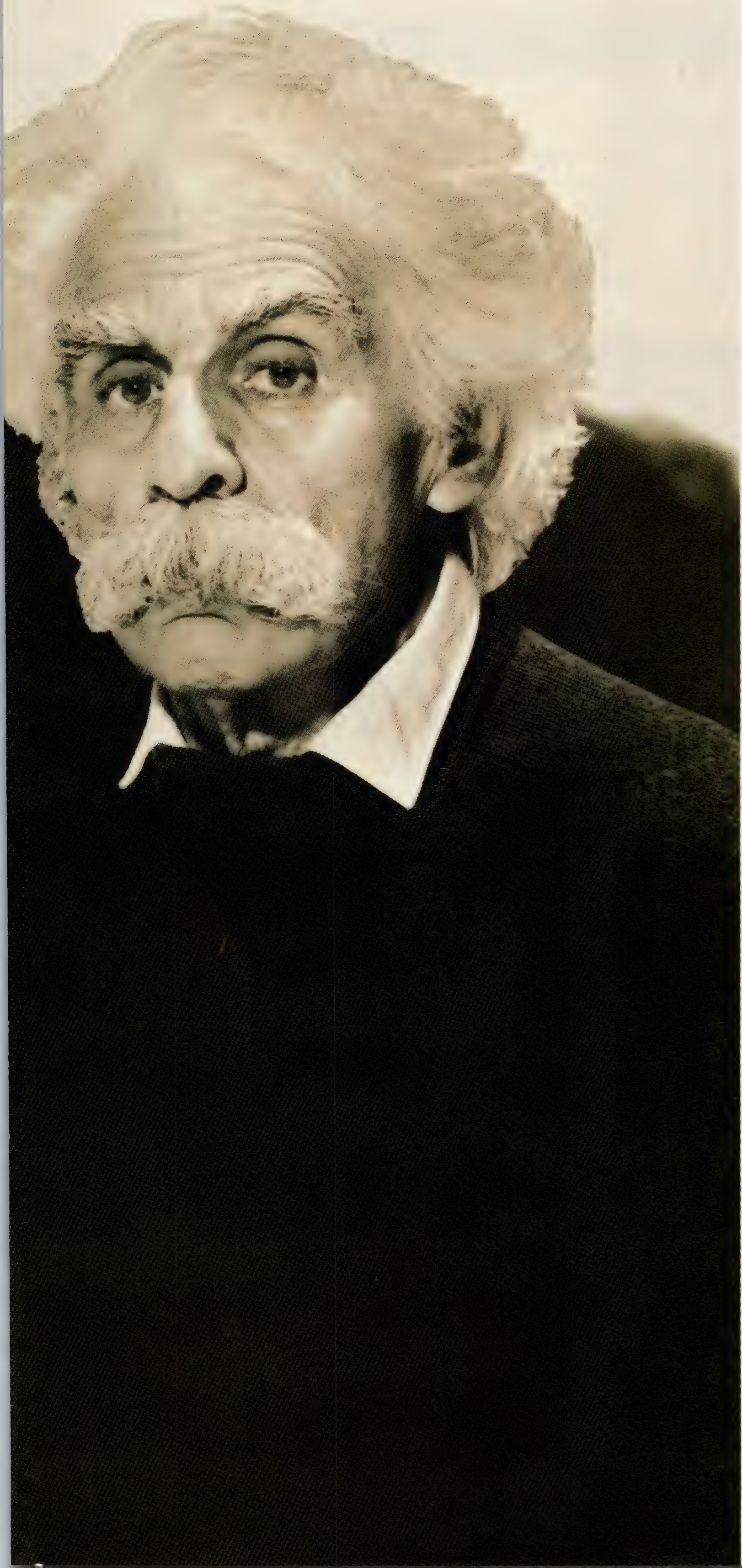

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256×64 pixel graphics mode; 40×8 text mode (with a moveable window on 80×25 character display)

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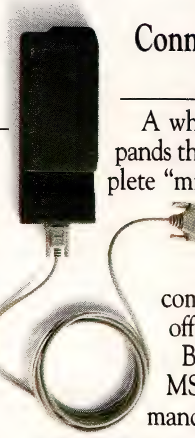

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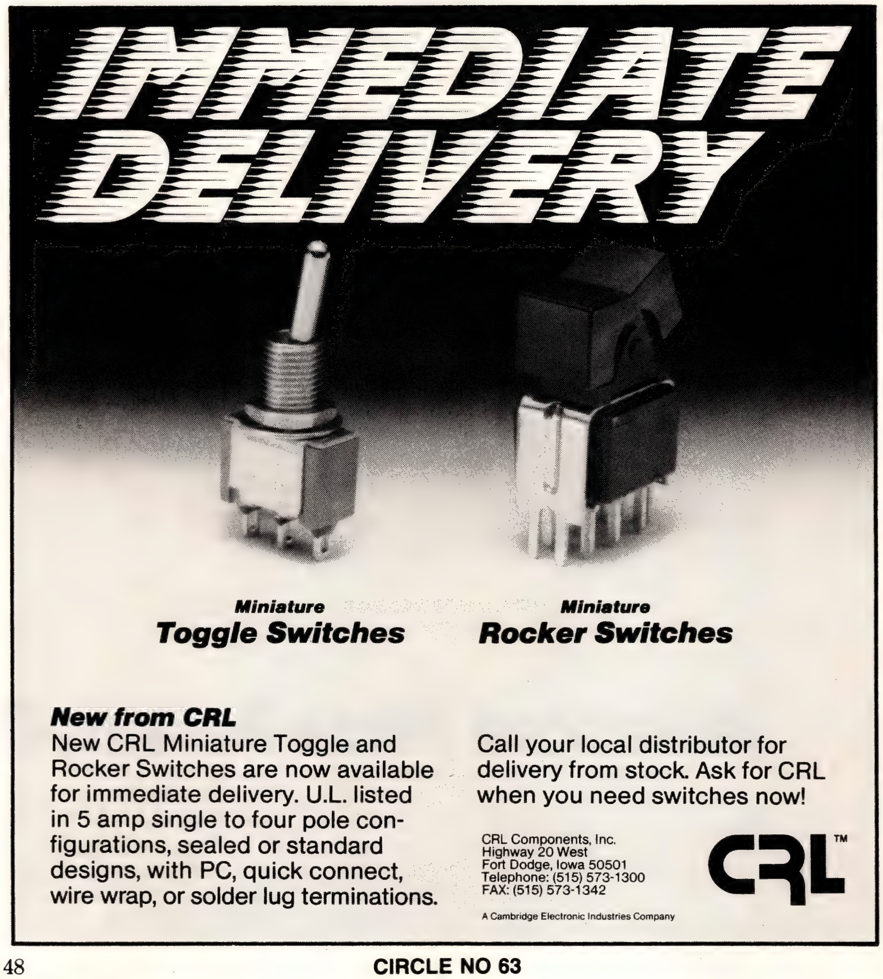

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1989 Linear Applications Seminar, Bellevue, WA. Various locations and dates. National Semiconductor, Box 58090, Santa Clara, CA 95052. (800) 548-4529. Through December 1.

Training Workshop for Visual Inspection of ICs and Hybrids, Boston, MA. Integrated Circuit Engineering Corp, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. FAX 602-948-1925. November 9 to 10.

Comdex Fall, Las Vegas, NV. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6602. FAX 617-449-2674. November 13 to 17.

Supercomputing '89, Reno, NV. Lyz Dunham, NASA Ames Research Center, Moffett Field, CA 94035. (415) 694-4370. November 13 to 17.

Wescon/89, San Francisco, CA. Wescon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. FAX 213-641-5117. November 14 to 16.

VMEbus in Industry, Paris, France. VMEbus International Trade Association, Box 192, NL-5300 AD Zaltbommel, The Netherlands. 31-4180-14661. FAX 31-4180-15115. November 21 to 22.

Spectrum 20/20 '89 Symposium, Montreal, Quebec, Canada. Marg Coll, Conference Coll Inc, 1138 Sherman Dr, Ottawa, Ontario, K2C 2M4, Canada. (613) 224-1741. FAX 613-224-9685. November 28 to 29.

Surface Mount Design for Manufacturability (short course), Bethlehem, PA. John Gilda, National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethle-

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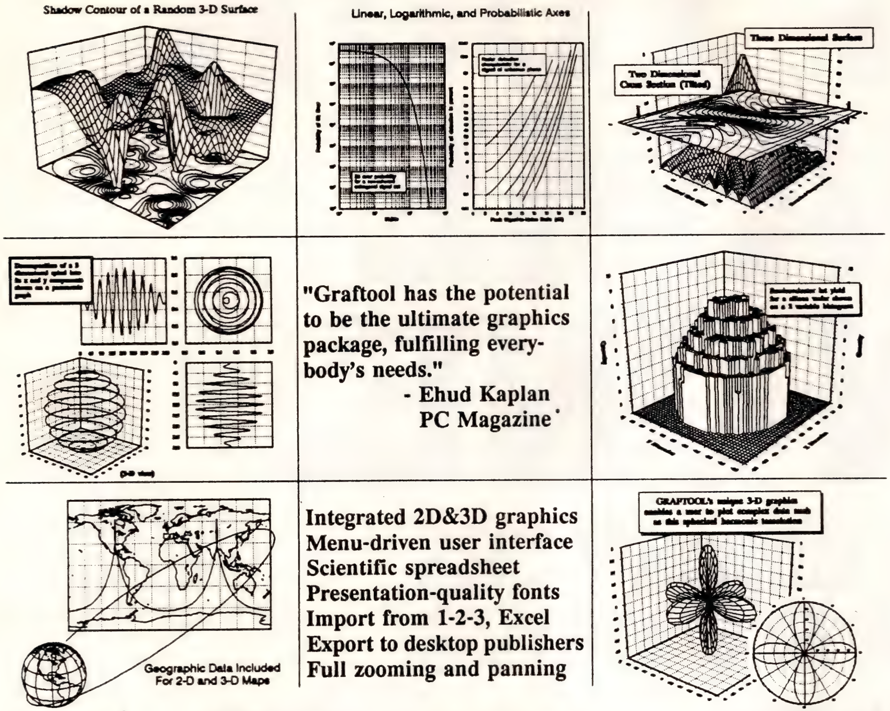

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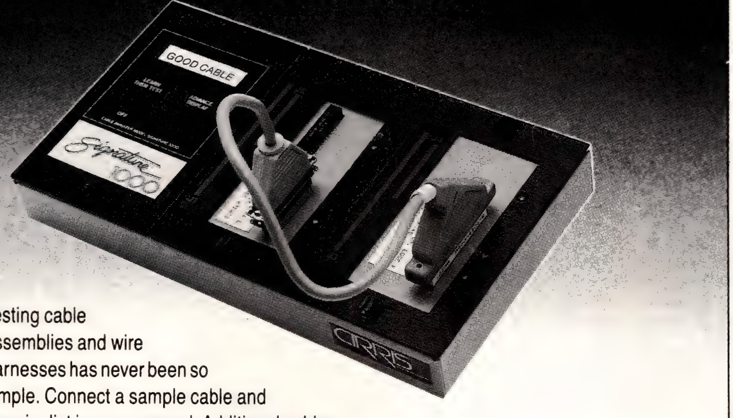

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hem, PA 18017. (215) 861-5450. FAX 215-861-5373. November 28 to 29.

Lasers in Electronics Manufacturing (seminar), Palo Alto, CA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. FAX 313-271-2861. November 29 to 30.

Computer Connectivity Invitational Computer Conference, Fort Lauderdale, FL. Suzanne Hubner, Invitaional Computer Conferences, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. FAX 714-957-0903. November 30.

SemiCon/Korea, Seoul, Korea. Semi, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 940-6901. December 6 to 8.

The International Conference on CAD/CAM and AMT in Israel, Jerusalem, Israel. Dr Lawrence R Odess, Dept 9621, Israel Aircraft Industries, 70100 Ben Gurion Airport, Israel. (972-3) 971-3991. December 11 to 14.

1989 289th IEEE Conference on Decision & Control, Tampa, FL. Leonard Shaw, Dept of Electrical Engineering and Computer Science, Polytechnic University, 333 Jay St, Brooklyn, NY 11201. (718) 260-3802. December 13 to 15.

OE/LASE '90—Optics, Electro-Optics, & Laser Applications in Science and Engineering/Exhibit, Los Angeles, CA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. January 14 to 19.

SaudiComputer '90, Saudi Arabia. Gerald G Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. January 28 to February 1.

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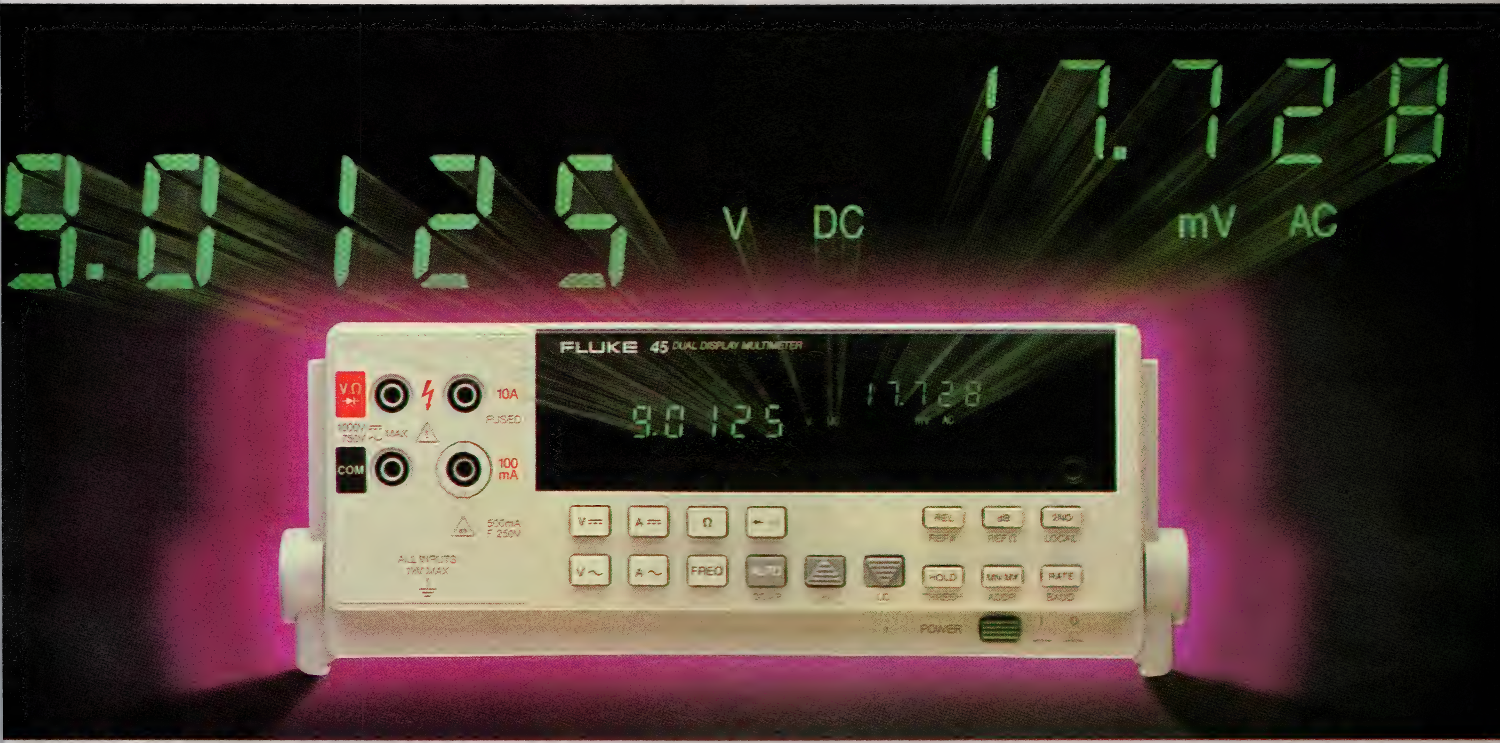

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4Mb DRAM SPECIFICATIONS

	4M x 1	1M x 4
Access Times	80ns, 100ns	80 ns, 100ns
Operating Power	550mW, 468mW	578mW, 495mW
Packaging	ZIP & SOJ	
Modes	Fast Page Nibble Static Column	Fast Page Static Column Write Per Bit

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CIRCLE NO 68

BEFORE LIGHT TRAVELS FROM HERE TO THERE WE'VE ALREADY SAMPLED IT TWICE.

Tek introduces the 2 GS/s DSA 600 Series. Phenomenal acquisition and waveform analysis at your fingertips.

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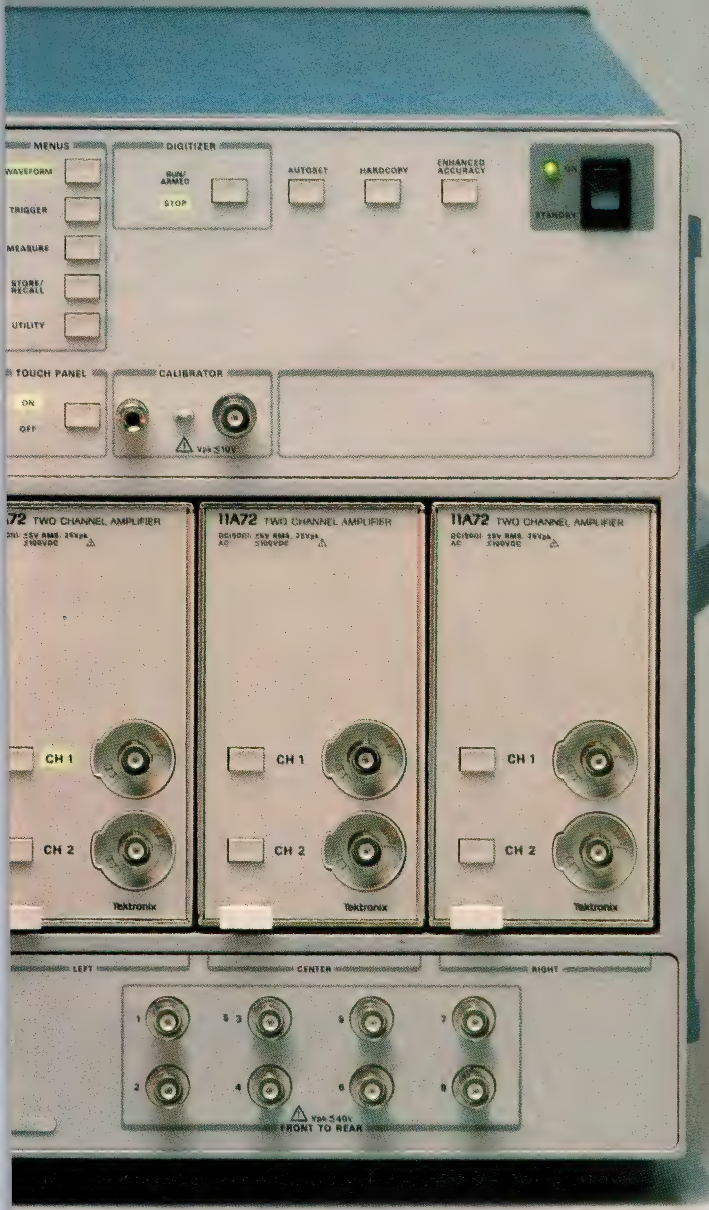
Just as logic and spectrum analyzers evolved from Tek scopes, now so does the Digitizing Signal Analyzer: thanks to Tek's proprietary digital signal processing chip, it is the first instrument to make real-time measurement and analysis practical at the highest acquisition speeds.



First of a new class of high-performance analysis tools, the DSA 600 Series combines the fastest acquisition speeds—1 GHz bandwidth, 2 GS/s sampling—with superb resolution and accuracy and an unprecedented set of waveform math and analysis capabilities.

These include real-time FFTs. Calculated gain and phase. Complex transformations. Averaging and smoothing. Processing capabilities you've never seen "live," if at all, on an oscilloscope before—all made possible by Tek's own TriStar™ Processor integrated between the instrument's digitizing and display processors.

Experience the DSA's phenomenal speed for yourself. In front-end acquisition. In waveform processing and analysis. In streamlined operation that lets you capture, measure, analyze, label, and output waveforms like they're standing still.

Call 1-800-426-2200 for a closer view of Tek's visible edge. *Or contact your local Tek sales engineer.*

	DSA 601		**DSA 602**		
Sample Rate	**500 MS/s**	**1 GS/s**	**500 MS/s**	**1 GS/s**	**2 GS/s**
Number of Channels	**2**	**1**	**4**	**2**	**1**
Record Length per Channel (Points)	**512-10K**	**512-20K**	**512-10K**	**512-20K**	**512-32K**
Nyquist Bandwidth	**250 MHz**	**500 MHz**	**250 MHz**	**500 MHz**	**1 GHz**
Repetitive Bandwidth	**1 GHz**		**1 GHz**		
Vertical Resolution	**8 Bits**		**8 Bits**		

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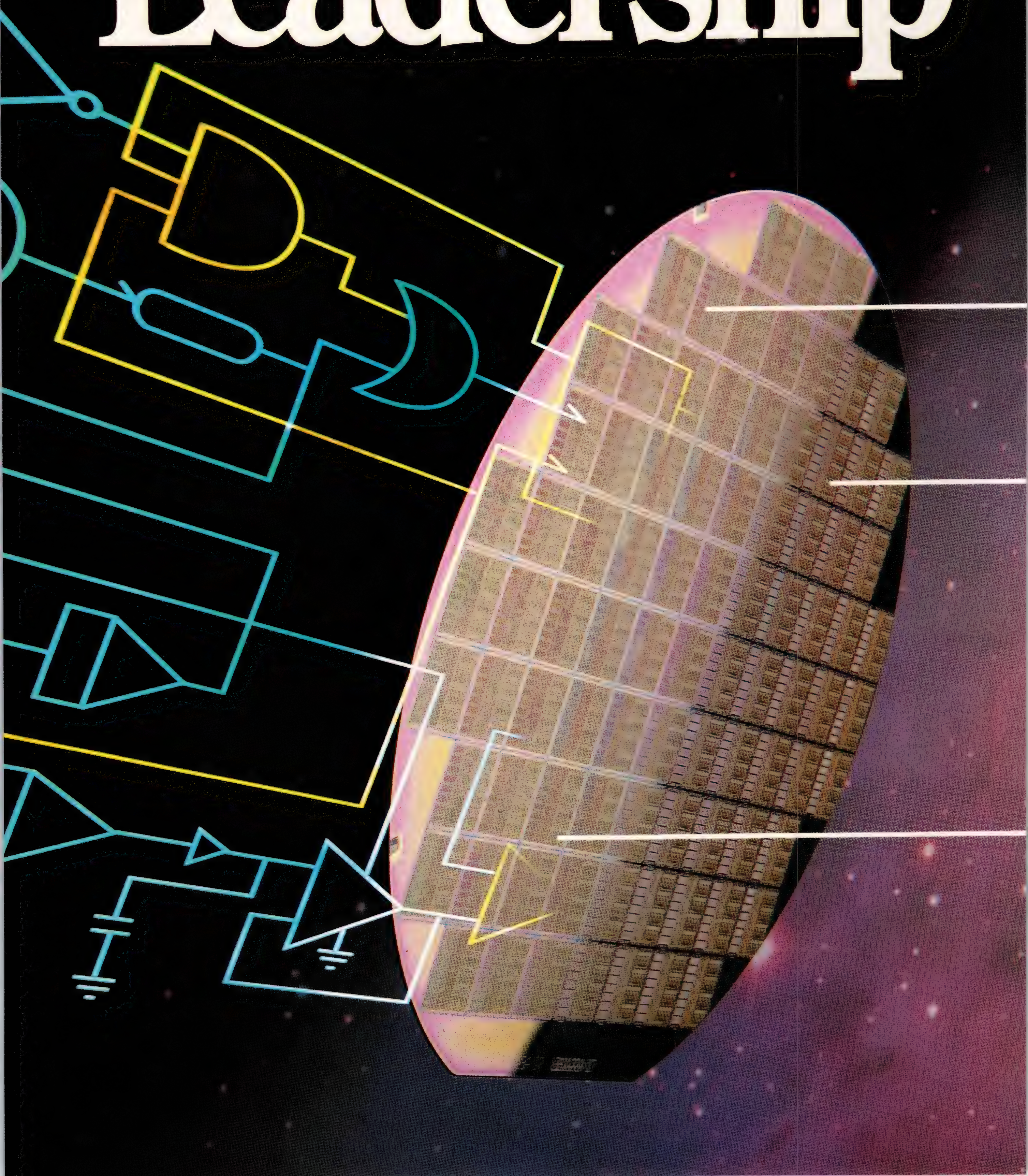
CIRCLE NO 69

Leadership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Innovation: At Plessey, new ideas, new designs, new applications and new technologies are what we do best and what we do first.

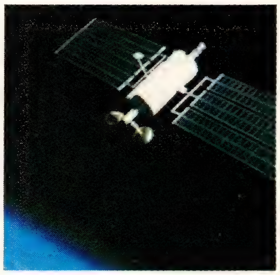
And while newness counts, so does practicality. The price/performance factor is integral to everything we do. Unlike some, we're not interested in creating flashy technology that no one can afford to use - or in solutions for which there is no problem!

Leadership means both breadth and depth
Plessey's broad product line is key to our leadership role. We offer an incredible choice of arrays that include our advanced "Read Channel" disk drive technology that we offer in highly flexible forms. Custom. Semi-custom. Standard. Semi-standard...The choice is yours.

As an ASIC company we supply the world with all manner of ASICs - analog, digital and mixed analog/digital in a variety of advanced state-of-the-art processes. In fine geometry, high density CMOS, bipolar and ECL technologies we provide the highest levels of performance and system integration available today.

As an ASSP (Application Specific Standard Product) company our standard product range offers the highest performance products available in the world today. Capabilities ranging from CMOS devices operating with only 10µA of current to the world's most advanced 1.3 GHz monolithic amplifier.

Leadership also means being colorful
Plessey's family of advanced DSP products offer you technology leadership in a variety of advanced image processing applications. For example our DSP 2D Convolver can easily handle 40 million pixels per second and it can be tailored to many specific applications like Medical, Military, or even the motion picture industry. It comes with its own cell libraries - written for DSP- not the typical all-too-general cell libraries others offer. Plessey also leads the way with compression techniques. And it's vital technology because as resolution improves with for example, HDTV, color copiers, color FAX machines or ultra-sonic imaging; disk space can be quickly gobbled up, unless you know how to put the squeeze on your images. Plessey shows you how.



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Search no more, start at the top with Plessey. Whether you're looking for a low-cost entry in stand-alone linear array design, JTAG Built In Test capability, machine vision, digital cellular phones, satellite or Global Positioning Systems, look to Plessey. We understand systems, components, packages and systems-on-a-chip. Plessey has them all. And you can have them all.

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CIRCLE NO 70

THE NO HASSLE FLASH

Face it, flash really was a great idea. They billed it as an easy-to-use, in-system programmable memory. And, it would be priced right.

Great idea, but they came up short. Real short.

Announcing the no-hassle, single-voltage flash that gives you the stuff they promised and more.

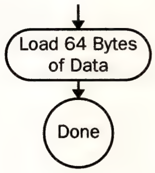
We call our flash a programmable read-only memory (PEROM). It's easier to use because there is no pre-write erase cycle. Erase is automatic; all you do is write. Atmel's PEROM (AT29C256) executes a complete, full-chip erase/write cycle in 10 seconds and only uses less than 40 bytes of code. Theirs takes two minutes because it uses a trial and error algorithm that needs over 200 bytes of code (want to guess who has to write and debug the code?). Just look at the number of steps to run each write routine—remember theirs also requires a trial and error full erase routine.

NOW FOR THE GOOD NEWS! The Atmel PEROM fits snugly into your 5-volt system. No extras. Theirs requires a 12-volt power source. Not only is a second power source a pain, it requires up to $8 more in circuitry per system, which in itself increases the potential for system failure.

So if you want in-system programmable memory without the hassle remember that the *real flash* is called PEROM.

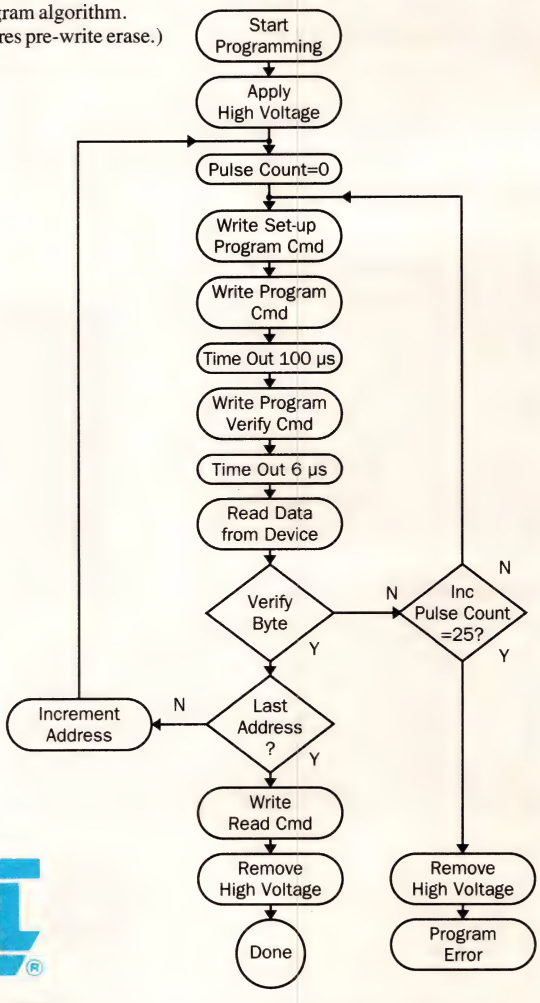
OURS

Reprogram algorithm.
(No erase required.)



THEIRS

Reprogram algorithm.
(Requires pre-write erase.)



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CIRCLE NO 71

EDITORIAL

Engineering goes on and on

As I glanced through a recent issue of *National Geographic* magazine, I realized that much of what one civilization passes on to another is its engineering artifacts. Thus, today we have the great pyramids of Egypt, the castles of northern Europe, the Great Wall of China, and the lost cities of the Americas. Other examples abound.

Certainly some literature and art are left behind, but even those remaining links with old civilizations often depend on science and engineering techniques, such as ceramics and metallurgy. Although many of those techniques and technologies were crude, they teach us a lot about the people who used them. The point is that without good engineering skills, such remains would be long gone.

Engineers today have reason to be proud because another one of their creations will last for a long, long time. The *Voyager 2* spacecraft, which has just completed its mission to Neptune, embodies electrical, electronic, mechanical, and chemical engineering technology that may well live to the end of the universe. In all likelihood, this artifact of 1970s engineering will be continuing on its silent voyage as the sun turns into a red-giant star and incinerates our solar system. To date, the only permanent records of man's existence in the solar system are several small spacecraft—*Pioneer 10* and *11* and *Voyager 1* and *2*.

Although it is doubtful that any other civilization will come across these mechanical space travelers, we can wonder about the reaction at such an encounter. Just in case such a meeting occurs, the *Pioneer* spacecraft incorporate an engraved plaque that describes where this work of ancient engineering originated. *Voyager 2* carries a recording of sounds ranging from whale songs to music by Chuck Berry.

We offer our congratulations to all the engineers, scientists, and technicians who worked on these spacecraft.

Visit us at Wescon

An enjoyable part of working on EDN is visiting and talking with readers. If you'd like to meet an EDN editor to talk about new technologies, products, standards, software, careers, your company, or anything else that involves engineering, stop by Booth 806. Editors will be available between 1:30 and 4:30 pm on Tuesday and Wednesday.

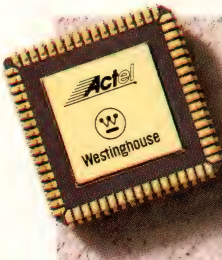
Jon Titus

Jon Titus
Editor

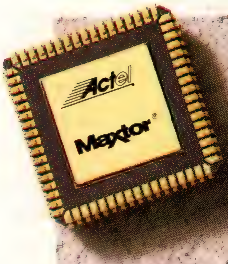
Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

Logic Int
For The



Westinghouse military systems engineers replaced four 22V10 PALs and six MSI devices with a single ACT 1010 part, handling the entire error correction, registration, and interface logic for their high speed, high dynamic range A/D converters. Schematics were captured on a Mentor system, and implemented with the Action Logic System (ALS). The design utilized 224 out of 295 logic modules.



Maxtor engineers use Actel's ACT 1010 chips and the Action Logic System software to quickly create and modify new disk drive electronics. They've produced nine different designs, with 85% to 95% gate utilization. During seven months of intensive work the ALS software has never crashed or lost data, and the system has produced every part as designed.

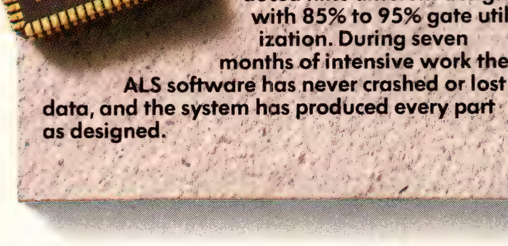
Actel Field Programmable Gate Arrays.

Let's face it. When it comes to programmable ASICs, greed is just good engineering. The best engineers are always hungry for more. More logic. And more different kinds of logic. All on one chip.

More is exactly what you get with Actel's ACT™ 1 field programmable gate arrays.

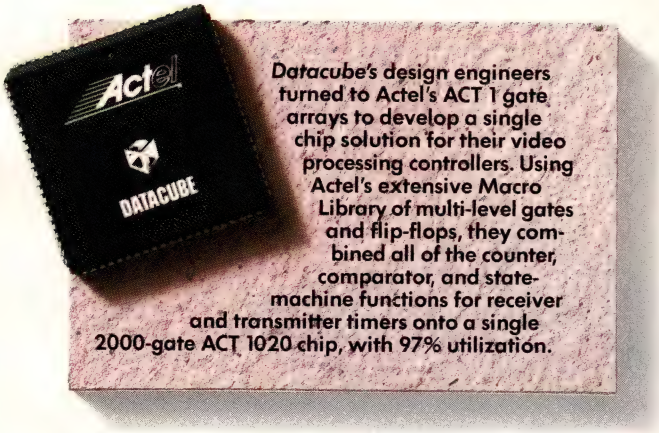
They're a whole new technology designed specifically for logic integration. Not just another brand of EPLD, PAL®, or LCA™ chip. They combine a true channeled gate array architecture with Actel's revolutionary PLICE™ antifuse programming element—resulting in 85% gate utilization. Guaranteed.

But you not only get more with Actel, you als get less. Less work, thanks to 100% automatic place and route. Less

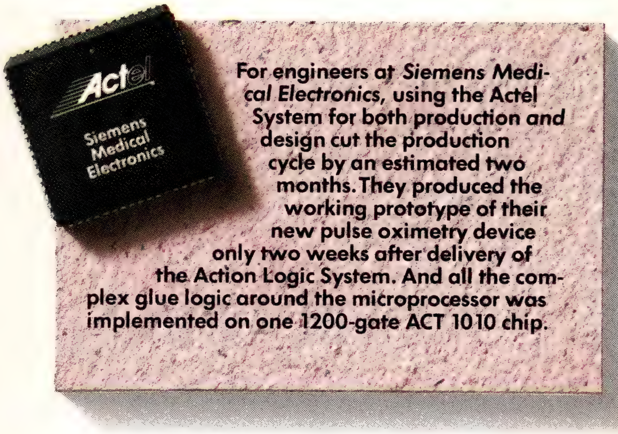


Actel's complete logic solution includes the Action Logic System (ALS) software, a programming module, and 1200- or 2000-gate ACT 1 programmable gate arrays.

egration Greedy.



Datacube's design engineers turned to Actel's ACT 1 gate arrays to develop a single chip solution for their video processing controllers. Using Actel's extensive Macro Library of multi-level gates and flip-flops, they combined all of the counter, comparator, and state-machine functions for receiver and transmitter timers onto a single 2000-gate ACT 1020 chip, with 97% utilization.



For engineers at *Siemens Medical Electronics,* using the Actel System for both production *and* design cut the production cycle by an estimated two months. They produced the working prototype of their new pulse oximetry device only two weeks after delivery of the Action Logic System. And all the complex glue logic around the microprocessor was implemented on one 1200-gate ACT 1010 chip.

design entry, with over 150 standard logic functions in the ACT 1 Macro Library. Less design time, with 100% observability of internal logic signals. And less time to market, with finished parts in hours, not weeks or months.

Not to mention much less cost, with no NRE. As in zero.

And the Actel design system is flexible. It works with popular workstations like SUN,™ Apollo,™ and 386 PCs; and popular design software like Viewlogic,™ OrCAD,™ Mentor,™ and Valid.™ Our 1,200-gate array holds the equivalent of 3,000 PLD/LCA gates, and our 2,000-gate array the equivalent of 6,000 PLD/LCA gates. And even higher densities are on the way.

So the next time you feel the need for greed, turn to Actel.

Call **1-800-227-1817, ext. 60** today for more information and a free demo disk.

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Risk-Free Logic Integration

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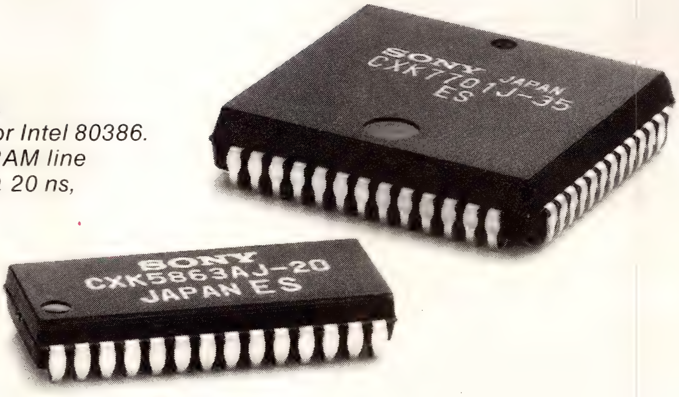
CIRCLE NO 72

SONY TAK
COMMITMENT TO



FAST CACHE.
Cache memory for Intel 80386. Also standard SRAM line down to 8K x 8 @ 20 ns, 16K x 4 @ 15 ns.

What you see here is a demonstration of Sony's intense commitment to your each and every SRAM need.

A commitment made even more impressive by the fact Sony's only been engineering and producing SRAMs for just over five years.

And when you consider we're pouring all our resources into SRAM technology—including a new production facility in Nagasaki, Japan—this demonstration merely hints at the Sony SRAM technology yet to come.

Ultra-high speed cache.

Via a unique 0.8-micron process, Sony covers your fast processor cache-memory needs two distinct ways.

First, there's our Model CXK7701J, designed specifically for the Intel 80386.

This application-specific memory (ASM) combines address latch, memory and transceiver within one IC. Ready for user configuration as either an 8k x 16-bit memory or as two 4k x 16-bit memories.

ULTRA-HIGH SPEED CACHE SRAMS

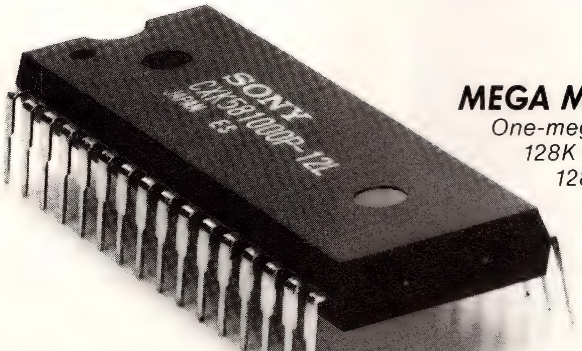
MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK7701J*	8K x 16	30/35/45/55	PLCC
CXK5863AP	8K x 8	20/25/35	DIP 300 mil
CXK5863AJ	8K x 8	20/25/35	SOJ 300 mil
CXK5466P	16K x 4	15/20	DIP 300 mil
CXK5466J	16K x 4	15/20	SOJ 300 mil
CXK5467P**	16K x 4	15/20	DIP 300 mil
CXK5467J**	16K x 4	15/20	SOJ 300 mil

*For Intel 80386. **O/E

Second, consider our new ultra-high speed SRAM capabilities.

As you scan the chart above, keep in mind even higher speeds will be available soon.

S ITS SRAM
THE EXTREMES.



MEGA MEMORY.
One-meg SRAM line includes
128K x 8 @ 100/120/150 ns,
128K x 8 @ 70/85 ns,
128K x 8 @ 35/45/55 ns.

Ultra-high density.

Sony solves your board-space problems with three new 1-Mbit SRAMs.

Each is based on our 0.8-micron CMOS technology. Configured as 128K x 8 bits. And available in 32-pin DIP and surface-mount plastic packages.

And not only do Sony 1-Mbit SRAMs maximize board space, but process speeds as well.

HIGH-DENSITY SRAMS			
MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK581000P CXK581000M	128K x 8 128K x 8	100/120/150 100/120/150	DIP 600 mil SOP 525 mil
CXK581001P CXK581001M	128K x 8 128K x 8	70/85 70/85	DIP 600 mil SOP 525 mil
CXK581020SP CXK581020J	128K x 8 128K x 8	35/45/55 35/45/55	DIP 400 mil SOJ 400 mil

Nowhere else will you find a greater choice: 100/120/150-ns, 70/85-ns and 35/45/55-ns speed figures.

Sony SRAMS cover the performance spectrum.

Sony offers well over one hundred SRAM solutions, covering the entire performance spectrum.

All competitively priced, all shipping now.

So call Sony with your most demanding SRAM spec.

We'll go to the extremes to deliver.

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It's a small wonder. The new BT&D™ DLX2000. The first completely integrated data link transceiver with a one-piece design that takes up less than two square inches of precious board space.

What's also wonderful is the way our DLX2000 performs. Performance that's the result of a high speed ELED light source and a planar PIN diode that has been created by our unique high-volume MOVPE process. With unequaled reliability stemming from the DLX2000's totally integrated, one-piece design.

The DLX2000 is extremely sensitive, offering a loss budget of -18.5dB with a 62.5μ fiber to virtually guarantee that your signal goes through. Go with a 50μ fiber and your loss budget is the same. Because the DLX2000 uses an ELED, not an SLED.

And it's been designed for full FDDI, point-to-point and LAN compliance. In a 28-pin package.

Only a company like BT&D could make a component as smart as the DLX2000. Combining the experience of an optoelectronic pioneer like British Telecom with the world-famous materials and manufacturing innovation of Du Pont.

Put the DLX2000 to your own test. It's available on an engineering evaluation board for a special, introductory price.

To order or for more information on the transceiver that will transform the way you think about space, call **1-800-545-4306.**

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CIRCLE NO 74

inside ASIA

American engineers in Japan:

Getting by with a little help from their friends

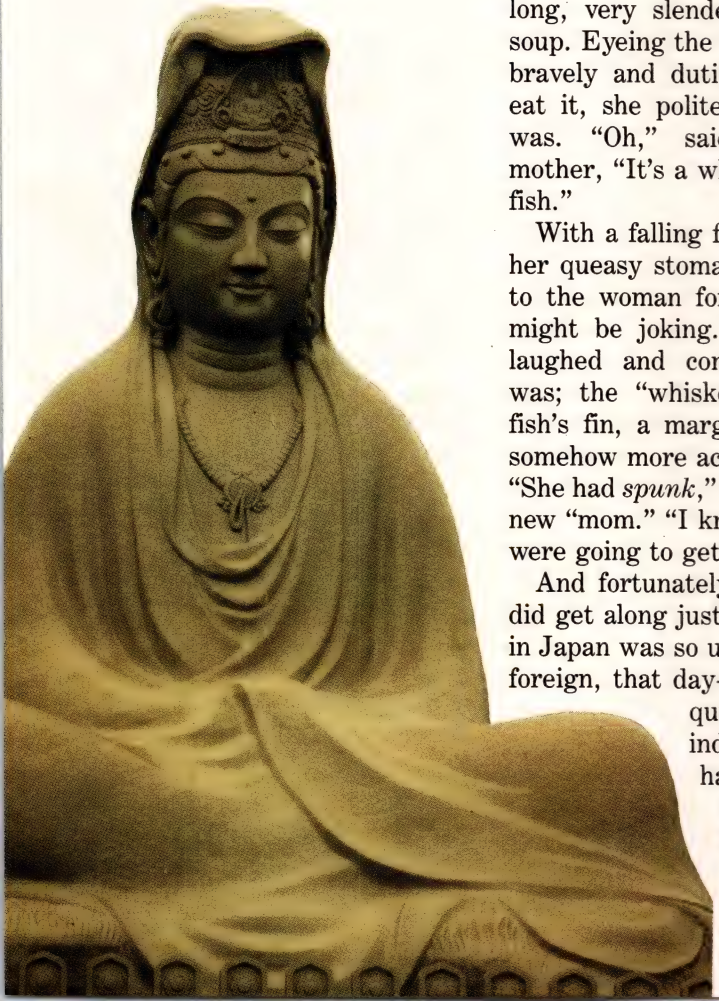
Gary Legg, *Special Projects Editor*

日本

American engineer Sue Galatz expected some surprises last year, when she spent six months working in Japan and living with a Japanese family. And right away, at one of her first dinners with her hosts, she found something strange—"a clear, long, very slender thing"—in her soup. Eyeing the object warily, but bravely and dutifully prepared to eat it, she politely asked what it was. "Oh," said the Japanese mother, "It's a whisker from a catfish."

With a falling face that betrayed her queasy stomach, Galatz looked to the woman for a sign that she might be joking. Hitomi Shimase laughed and confirmed that she was; the "whisker" was really a fish's fin, a marginally better but somehow more acceptable delicacy. "She had *spunk*," Galatz says of her new "mom." "I knew right then we were going to get along just fine."

And fortunately the two women did get along just fine, because life in Japan was so unfamiliar, so very foreign, that day-to-day coping required resources an individual might have difficulty mustering. With the help of her Japanese hosts, however, Galatz managed nicely; when she returned to America four months later, leaving the warmth of her new "family," she says, was one of the hardest things she had ever done.



Others from Galatz's home base, a Tektronix pc-board manufacturing facility in Forest Grove, Oregon, report similar experiences. Since 1985, Tektronix has sent ten engineers to Japan in an exchange program with NEC Toyama, a subsidiary of the Japanese NEC Corporation. (See EDN, October 26, 1989, page 59.) Assignments begin with two months of intensive Japanese language study and end with four months of engineering work.

Japanese work conditions are harsh, the Tektronix engineers discovered, and Japanese customs can be bewildering, but the Japanese people are friendly and animated once you get past a typical quiet reserve. The "home-stay" aspect of the exchange program (Americans live with Japanese families in Japan, and Japanese engineers live with American families in Oregon) offers not only assistance in adapting to a different culture, but also

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This article is the third in a series about engineering in Asia. It's the second of two articles about American engineers living and working in Japan.

Sue Galatz relaxes with her Japanese host "sisters," Akemi and Mari Shimase.

opportunities for intimate glimpses of that culture.

Galatz, for example, was amazed to learn that her host couple had become engaged on their second date but didn't kiss until six months later. She was further surprised that even after 13 years of marriage the couple still would not display affection in front of others. Only after Galatz had become very close to them, and only after a great deal of teasing and coercion, did she finally persuade them to hug for a snapshot. They agreed only on the condition that she never show anyone the picture.

For Japanese engineers living in Oregon, the situation was reversed. Every time Hidebumi Ohnuki's American host couple hugged or kissed in his presence, he was embarrassed. "I was very uncomfortable," he says. "We don't have that [in Japan]." Ohnuki will hug or kiss his own wife only in private.

Thirty seven at the time of his exchange assignment in 1986, Ohnuki lived with American "parents" who were only a few years older than he was. In general, NEC exchange engineers are considerably older than their Tektronix counterparts and are much more likely to be married. All the exchange-program participants complete their six-month assignments apart from their families, but of the ten American engineers sent to Japan by Tektronix, only one was married at the time. Most of the Americans have been in their early to mid-twenties.

The Japanese reluctance to display affection, the Americans discovered, is actually part of a more general trait: a conditioned aversion to showing *honne*, or true feelings. When Galatz was shown the Shimase family photo album soon after her arrival, she was startled to see unsmiling faces in all her hosts' wedding pictures. "Weren't you happy?" she asked. "Of course," came the reply. "Then why aren't you smiling?" Hitomi responded with a pause and a puzzled "Oh," as if she had to carefully consider the ramifications of such odd behavior.

Hitomi's reaction to her mother's death further bewildered Galatz, who only a few months earlier had lost her own mother and still felt an acute sense of loss. Hitomi, however, displayed no emotion whatever over the loss of her own mother. She came home from her mother's deathbed, Galatz recalls, and there were "no tears, nothing—nothing at all. She sat down, ate watermelon, and went to bed."

For Mary Mollison, a Tektronix engineer who participated in the exchange program in 1987, the absence of displayed affection was most unsettling at the time of *Obon*, a festival in which Japanese visit the graves of their ancestors. On this particular occasion, the extended family of Mollison's homestay "dad"—three siblings, their spouses, and their children—had come from all over Japan to gather in Mollison's hosts' home. "They don't see each other very often," Mollison says, and yet, when the family members met, they merely "got down on the *tatami* (mat) and gave a huge, big bow—no hugging, no kissing. I'm from a family that's very open, very demonstrative," Mollison continues. "I was very upset."

Surprises at foreign customs and attitudes weren't limited to the Americans, however. Some common American situations were difficult for the Japanese hosts to grasp. The American melting pot, for example, when considered by members of a society that is virtually

Japanese homes contain plenty of electronic items, the Americans discovered, but few modern appliances.

homogeneous, is a strange and sometimes amazing concept. "To tell them that my father is from Romania and my mother is from Italy," says Galatz, "just blows them out of the water."

Galatz also had difficulty explaining that she was adopted, because adoption is virtually unheard of in Japan. First, she says, "I got out my huge dictionary, because the little one I carried around with me didn't have 'adopt' in it." When that didn't work, she resorted to drawing pictures—first a pregnant woman, then a baby, and finally a set of parents. "They didn't get it for a while," she says.

Taken individually, things such as language difficulties and unfamiliar customs weren't particularly bothersome to the Americans. Their engineering work was familiar to them, and their host families kept them from feeling isolated in the foreign culture. In combination, however, language, customs, and social pressures—to hide feelings, for example, and to suppress individuality—created some stress.

Sue Galatz prepares to eat kaiseki ryori, the traditional food of the Kyoto area. With her is her host "mom," Hitomi Shimase.

Pressure to conform is strong in Japan; it's expressed by the oft-quoted saying: The nail that sticks up gets hammered down. And nowhere is this more true, the American engineers found, than in the workplace. You work as a team, not as individuals; you know your place, and you stay in it.

For Mollison, an important coping mechanism was to keep her quintessentially American traits—assertiveness and confidence—and to freely express her feelings. If this behavior seemed unusual to the Japanese, it was at least acceptable. According to Ross McLaughlin, another Tektronix exchange engineer, "They expect it. If you try to become too Japanese, they resent that. They realize you're different."

Similarly, the Americans learned to accept some Japanese attitudes that they couldn't subscribe to themselves. Mollison, for example, now married but single while in Japan, found some attitudes toward marriage simply baffling. Arranged marriages, for example, although no longer the norm, still occur in Japan; marriages of convenience, to a "suitable" breadwinner or homemaker, are common. When Japanese friends suggested that Mollison's inability to understand such customs is because she's American, her response was, "You got *that* right!"

"My heart doesn't allow me to understand it," Mollison says. Nor does she understand the common practice of Japanese families living apart, sometimes for several years, when the husband, who is almost always the main breadwinner, gets a job transfer. Although she has good memories of her time in Japan, she would "never do it again" now that she's married. "I'd have to have my family over there," she adds.

One source of stress for the Americans was simply being different from everyone else. As far as they know, the Americans who work at NEC Toyama—two at a time—are the only non-Japanese in Nyuzen, the city of 30,000 people where they live. They stand out so distinctly that children would point and cry out, "*gaijin*!,"as Galatz rode her bike to work.

Being so obviously a *gaijin* (foreigner) created more tangible problems, too. Mollison and a male friend were refused admittance to ten different restaurants in Kyoto, a fact she attributes to racial preju-

dice. McLaughlin's host family had difficulty finding vacation hotel accommodations whenever they mentioned a *gaijin* would be with them.

Just dealing with things that were different required extra mental energy, and one thing the Americans found very different was the Japanese food. Although they loved most of it, there were a few things they didn't: *natto* (fermented soybeans connected by "a kind of goo"), fish heads (sour, with staring eyes), and a typical breakfast (rice, raw egg, and fish). "If you don't like fish," Mollison says, "do *not* go to Japan." You can escape eating raw fish, though, according to McLaughlin, and for a break—in the large cities, at least—you can even find American fast food. After a prolonged diet of Japanese cuisine, McLaughlin says, "a Big Mac never tasted so good."

But Japanese tastes are expanding, the Americans found. Spaghetti, for example, is popular, perhaps because noodles are a traditional Japanese staple. Japanese pasta sauces tend to be sweet, however; when Mollison made a sauce from her favorite recipe, using tomatoes, olive oil, and basil, her home-stay family didn't like it. Galatz, on the other hand, cheerfully concocted a sauce from ingredients at hand—ketchup, mostly—and her family loved it.

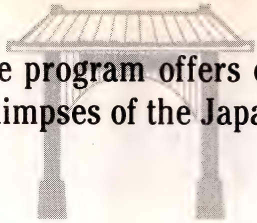
McLaughlin introduced his family to breakfast cereal, a food they continue to enjoy. In general, however, the Japanese host families didn't distinguish breakfast from other meals; anything left over from dinner the night before—noodles, steak, even pizza—was likely to find its way to the breakfast table.

Food, especially Western food, is expensive in Japan. Beef costs as much as $70 to $90 a pound, according to Galatz, and cantaloupes sell for $60, or $10 a slice. Cantaloupes are so rare, in fact, they're sometimes given as gifts or as game-show prizes.

Even beer is expensive—about $3 to $6 a bottle in bars. Surprisingly—to Americans, at least—you can buy beer in vending machines. Not surprisingly, considering their Japanese sources, the machines are state-of-the-art marvels, complete with digital displays for the amount of money you've deposited and timers that prohibit sales after 11:00 PM.

Housing is expensive in Japan, too, largely because of a space shortage. The country is smaller than California in area, but its population is roughly half that of the entire US. For a four-bedroom, 2500-square-foot apartment in Tokyo, a friend of McLaughlin paid a monthly rent of $12,000. Such large quarters are unusual, however; by

Ross McLaughlin models traditional Japanese garb—a yukata (a somewhat informal kimono), geta (sandals), and sensu (fan) with his host "dad" (more like a big brother), Haruo Shimizu. The attire is typically worn in public for special occasions, although some people wear it daily.



The exchange program offers opportunities for intimate glimpses of the Japanese culture.

American standards, says McLaughlin, most apartments in Tokyo are "rabbit hutches." Even so, they're expensive enough that most city workers face long commutes from more reasonably priced areas.

Nyuzen, where all the Americans' host families lived, is a small city in an uncrowded area, so housing is roomier and more affordable. It's still far from cheap, though; McLaughlin cites as an example a 2200-square-foot house valued at $360,000.

Japanese homes contain plenty of electronic items, the Americans discovered, but few modern appliances. Stereos, VCRs, and large, feature-laden TVs are common; dishwashers, garbage disposals, and clothes dryers are not. Practically every home has an automatic rice cooker, but few have microwave ovens. Most homes contain lots of "stuff"—much of it trinkets and souvenirs given as presents by friends.

The Americans' home-stay families were close, and the fathers played a more active role than many Japanese fathers do. Galatz's "dad," 40-year-old Akiyoshi Shimase, was usually home from work by 7:30; on his arrival, the female household contingent—his wife, his 6- and 10-year-old daughters, and Galatz—would gang up on him in playful banter. For McLaughlin, the first order of business after work was a *sumo* wrestling match with his eight-year-old "brother," Kendai.

Since the engineering exchange program's inception in 1985, its participants have empirically determined what kinds of families are best suited as hosts. The Japanese families now involved seem to be somewhat American in outlook, with actively involved fathers, for example, and mothers who may hold jobs outside the home. Neither Galatz's nor McLaughlin's home-stay mother fits the stereotypical mold of a homebound Japanese wife. Galatz's likes to drink whiskey and water and play pachinko, and McLaughlin describes his, a former nurse, as "a wild one, really crazy, really off the wall, really excitable." Galatz recalls McLaughlin coming to work soon after their arrival in Nyuzen and saying, "I can't believe her! She talks two inches from my face!"

Yet along with the high spirits come stability and calm. The families' greatest benefits to their foreign guests, the Americans agree, were their constancy and their receptive ears. "I wanted to be in an environment where things were common to me," says Galatz, "where if someone asked me something, I knew there wasn't a hidden agenda. When you're at work," she adds, "you have to mind your P's and Q's constantly. If you say something wrong to somebody. . . "

"On the days when you come home," Galatz continues, "and you're tired and ready to tell everybody off at work, and there are the kids greeting you at the door and a home-stay mom [to talk to] . . . it's just like having your own family again."

"You grow very close to them," says Mollison. "They're the one thing you can rely on to get you through things." Leaving her home-stay family at the end of her assignment, she says, brought "the most sickening feeling I've ever had. I sobbed for hours."

Leaving was equally difficult for Galatz and McLaughlin. "The last day," says Galatz, "I came downstairs, and the 10 year old had made me a huge banner, and there were balloons all over the kitchen. We all sat at the breakfast table and cried."

"You just can't thank them," continues Galatz. "You don't know the correct Japanese to express how you really feel. You can just say thank you so many times, and you feel you still haven't done it enough." **EDN**

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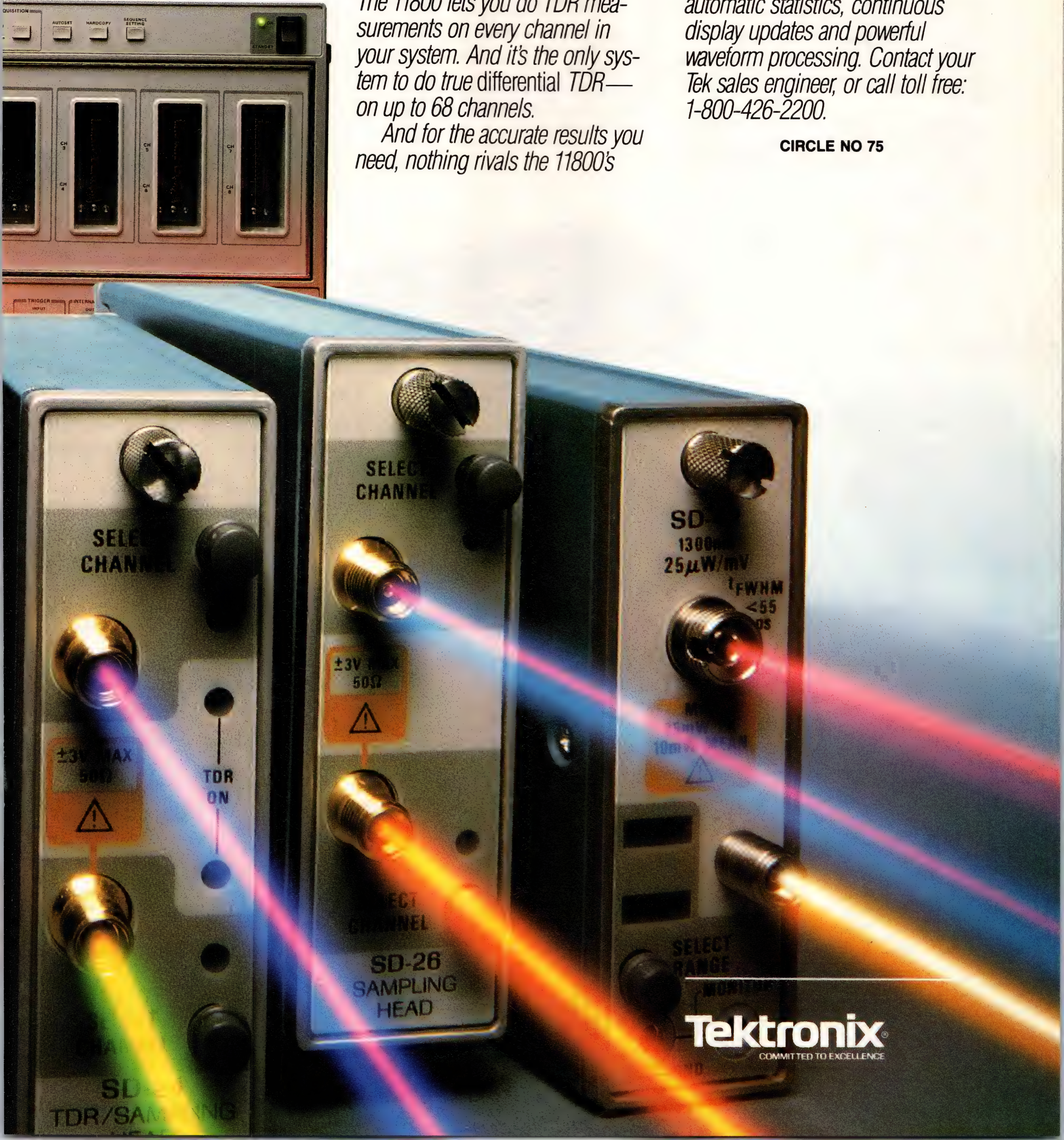

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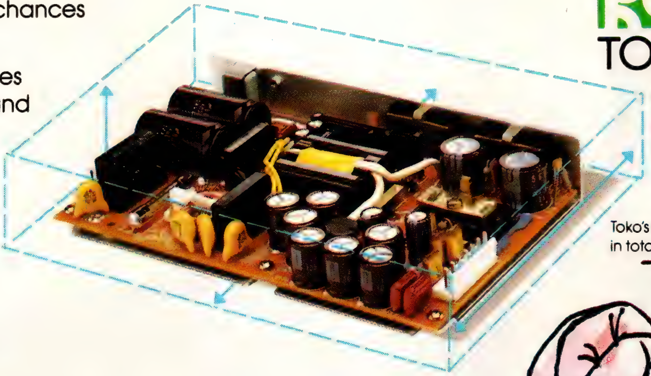

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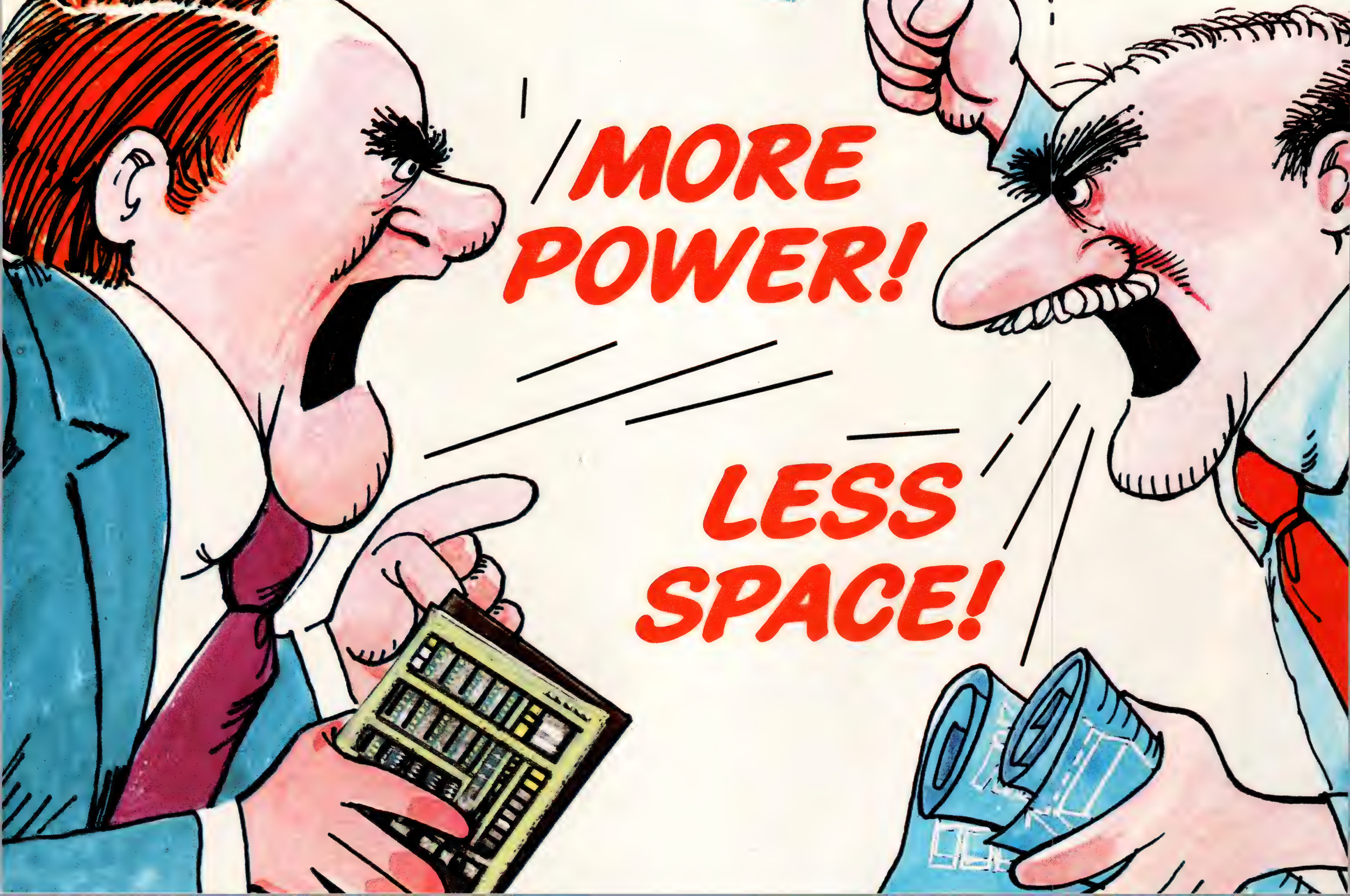
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SURFACE-MOUNT-TECHNOLOGY UPDATE

Fine-pitch SMT needs shrewd pc-board design

Despite their frustrating package diversity, the need for increased circuit density and device pin count will probably force you to incorporate fine-pitch, surface-mount devices in your next design.

Richard A Quinnell, _Regional Editor_

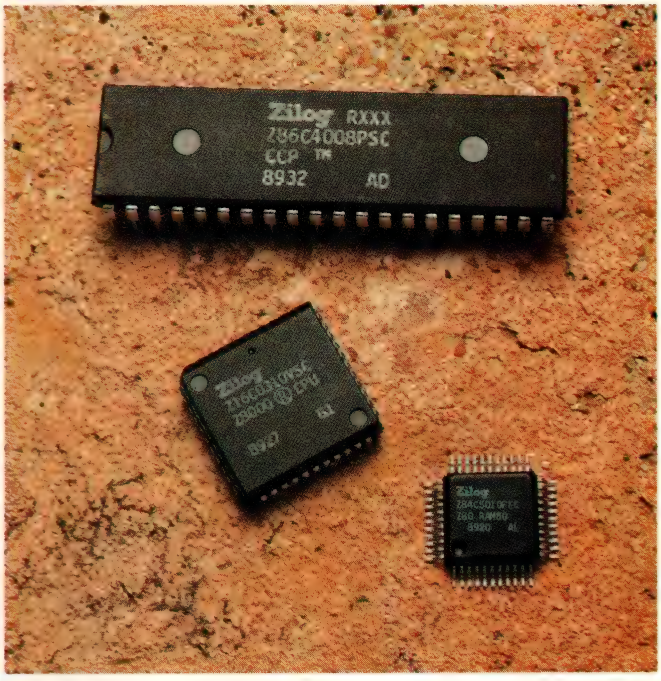
Whether or not you have experience using surface-mount plastic leaded-chip carriers (PLCCs), your design work is going to become more complicated. To attain the circuit densities new designs will need, your circuit boards will most likely include fine-pitch devices, and using those devices will require a good deal of extra work.

Fine-pitch packages are packages with lead pitch (center-to-center spacing) of ≤25 mils. Manufacturers developed fine-pitch package styles to overcome the pinout limitations of the older surface-mount-technology (SMT) packages, such as PLCCs and small-outline IC (SOIC) packages. PLCCs and SOIC packages feature lead-pitch settings of 50 mils. Because of practical restrictions on package size, lead pitch determines the device's maximum possible lead count. PLCCs, for example, can have no more than 84 leads. SOICs are even more limited; their use is confined to MSI (medium scale integration) functions such as those found in 14- or 16-pin DIPs.

Fine-pitch packages get around these lead-count limitations by reducing lead pitch. The lead pitch can be 25, 20, 15, 12, or 10 mils, resulting in packages that sport as many as 524 leads. Package styles that fall into the fine-pitch category include the quad flatpack, the plastic quad flatpack, and ICs designed for tape automated bonding.

Fine-pitch standards are broad

Unlike the more established package styles, fine-pitch packages lack a consistent set of design rules for creating circuit boards. Fine-pitch standards do exist, but many industry experts and board manufacturers claim that those standards are too broad. The result of these broad standards is a plethora of similar-looking packages whose variations seem minor but are actually very significant.



As PLCCs replace DIPs, *they're replaced in turn by fine-pitch devices. Companies such as Zilog, with its Z80 family, are providing a full range of package styles for their ICs.*

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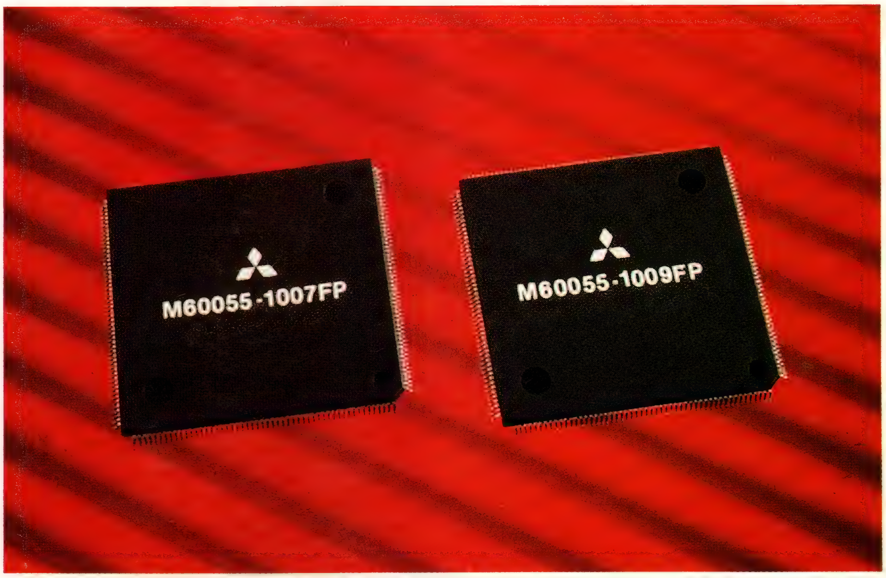
A good example is the flatpack. The two versions of this package style are the quad flatpack (offered by Japanese companies) and the plastic quad flatpack (offered by US companies). The Japanese version, under the EIAJ (Electronic Industries Association of Japan) standard, offers a mix-and-match set of package sizes and lead pitches. Packages may have an edge length of 14, 20, 28, or 40 mm with lead pitch of 1, 0.8, 0.65, or 0.5 mm. The US version, under the JEDEC standard, has a fixed lead pitch of 25 mils; package size varies with pin count.

Even with packages of the same size and lead pitch, variations may exist. Some devices have leads that drop straight from the package to the board; others have leads that extend from the package at an angle. The resulting difference in footprint position is comparable to the size of a fine-pitch solder pad.

The result of all this variation becomes apparent when you begin board layout. Surface-mount devices, especially fine-pitch devices, require precise board design. The size, shape, and placement of solder pads on the board have a great impact on the yield and reliability of SMT circuit boards. Pads that are too small result in unreliable connections; pads that are too large encourage formation of solder bridges. A .005-in. misorientation during part placement may cause the leads of a high-pin-count device to fall between rather than on the pads.

All isn't lost, however. You can



***Fine-pitch devices go beyond the limits of older SMT packages** by providing more I/O capability. This gate-array package from Mitsubishi, for example, has 208 leads—an I/O capability that was once the exclusive territory of pin-grid arrays.*

Can your CAD system handle SMT?

Before you begin your SMT design, make sure that your CAD system can deal effectively with SMT packages. Jim Blankenhorn, president of SMT Plus, suggests that you check the following features of your CAD:

- ***Grid size***—Because of the wide variety of lead pitches in use, in both metric and standard measurements, your minimum grid size should be ≤1 mil. You should also be able to handle multiple-grid routing to accommodate a combination of package styles.
- ***Vias***—You should be able to create blind and buried vias in addition to conventional ones. Make sure your system doesn't automatically place a through via for each lead—you won't necessarily need them.
- ***Component placement***—You should be able to stack components as well as mount them on both sides of the board. This capability lets you place passive components underneath ICs.
- ***Component size***—You should be able to handle devices that have as many as 1000 leads.
- ***Pattern shapes***—You should be able to create odd-shaped patterns for solder pads and reference markers.
- ***Test points***—You should be able to create and verify test pads—a bare solder pad with no associated component.
- ***Pad patterns***—Make certain that the solder-pad patterns in your library correspond to the part you'll be using and not to a generic standard.

Other helpful CAD capabilities include layout-impedance simulation and the ability to measure trace lengths.

take steps during the design phase to increase the odds of successful manufacturing. The first step is to become familiar with your board-manufacturing capability.

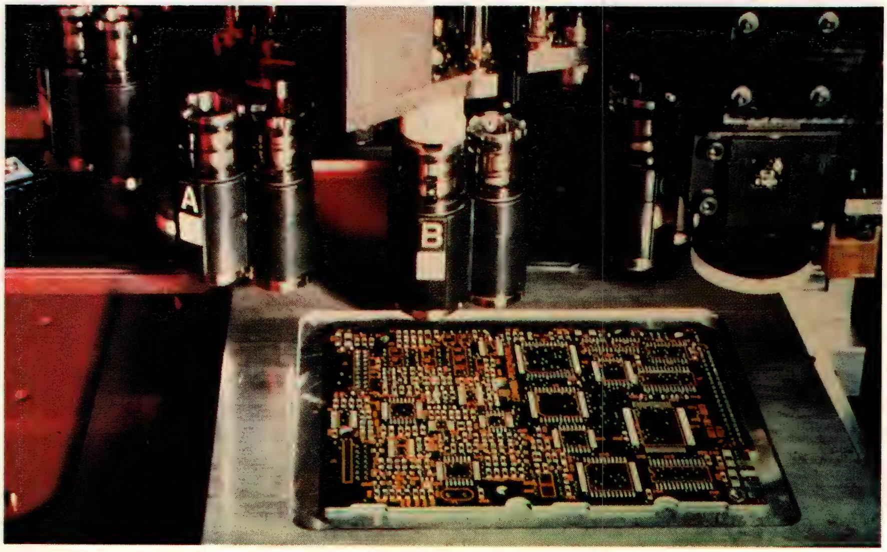
Manufacturing variables such as solder-paste chemistry, part-placement accuracy, and even the direction the wiper blade moves when applying solder paste can dictate board-layout details. As a result, board manufacturers have developed design guidelines based on their processes and equipment. These guidelines cover topics such as pad dimensions and geometry, preferred component orientation, and spacing between vias and solder pads.

Knowing your manufacturing capability also enables you to leave enough space between components for inspection and rework access. You may also find that you need to put reference markers on the board so that vision-based placement systems can accurately position parts on it.

Another step you can take is to make sure that your pad-layout patterns match the lead spacing the devices you'll be using. If you use the empirical approach and measure a representative device that you've purchased, make sure your manufacturing department uses the same source of supply. Devices from different manufacturers may be in specification and still require different pad patterns. Instead of measuring each device, you could simply buy layout patterns. For example, SMT Plus, an SMT training company, offers a handbook ($99.95) with pad-layout geometries for more than 100 SMT devices.

Board layout affects reliability

Parts layout can also affect your board's manufacture. From a signal-performance standpoint, it's desirable to arrange intercommunicating parts as close together as possible, but an uneven placement of parts can cause poor manufacturing yields. Such placement results in uneven heating of the board during soldering, causing thermal stress, overheating of smaller components, and insufficient heating of large components. Tombstoning and unreliable solder joints can often result. To ensure proper soldering, design your board so that its thermal mass is evenly distributed.



***An even distribution of thermal mass** is one of the keys to successful SMT board design. The even distribution allows more uniform heating of the pc board during soldering. (Photo courtesy Solectron)*

Finally, consult your test department to determine their need for test pads. The leads on fine-pitch devices are easily damaged, so the test department may not be able to probe the package leads to pick up their test signals. Because SMT devices don't require a via for each lead, the signals may not appear on the back of the board, either. Circuit traces may be buried on an inner layer or may be too small to probe. Therefore, to make your design testable, you'll need to place test pads on your critical signal lines.

If your company is just starting to use surface-mount technology, you may wish to try contract board assembly. Experienced contract assemblers—such as Flextronics, Jabil Circuit Co, SCI Manufacturing, and Solectron in the US—have well-characterized processes and are familiar with their sources of supply. Each company has design guidelines optimized for its production capability.

If you are setting up your own SMT production line, plenty of help is still available from professional organizations that offer information and guidance. The Surface Mount Technology Association (SMTA) is a nonprofit society that provides education on SMT. The Association works through local chapters that hold monthly meetings, sponsors an annual technical symposium, and publishes a quarterly journal. You can obtain general design guidelines and information on standards from the Institute for Interconnecting and Packaging Electronic Circuits (IPC).

For more immediate help, try a phone-in service. The Surface Mount Network (New Britain, PA, (215) 348-7033) serves as an infor-

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mation broker, connecting users of SMT devices and manufacturing equipment with suppliers. Jones Futurex (Rancho Cordova, CA) sponsors a free SMT electronic bulletin board. You can call the bulletin board with a 1.2k- or 2.4k-baud modem ((916) 635-8665) to exchange notes with other users.

As designers and manufacturers gain experience with fine-pitch devices, useful industry-wide design guidelines are bound to emerge. Until then, you'll have to do the footwork to find out what works for your particular manufacturing environment, but if you devise your own guidelines and carefully adhere to them, you can produce reliable fine-pitch SMT boards. **EDN**

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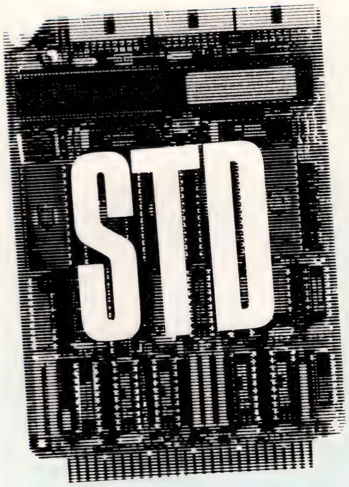

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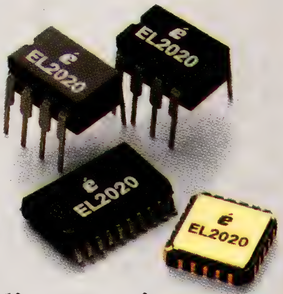

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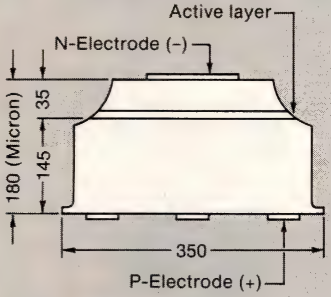

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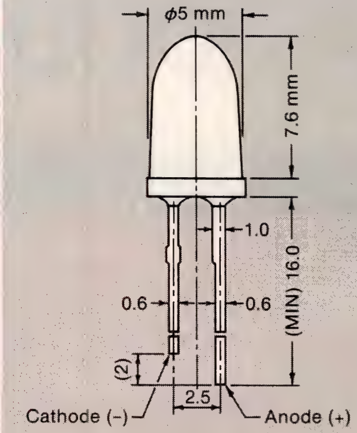

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CIRCLE NO 81

OBJECT-ORIENTED PROGRAMMING

Objects facilitate modular, reusable code

Object-oriented languages and techniques are starting to change the way designers think about data structures for complex systems.

Chris Terry,
Associate Editor

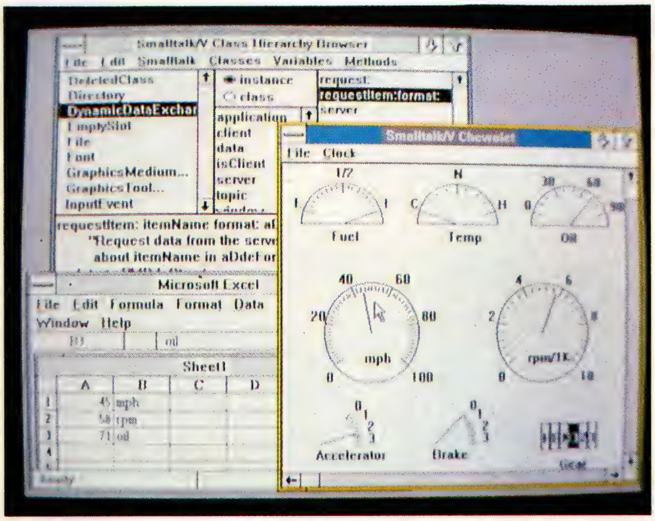
OOP (object-oriented programming) techniques are by no means new—some of them have been around for nearly twenty years. However, it's only in the last three or four years that compiled, rather than interpreted, OOLs (object-oriented languages) have become available. Previously, because of the multiple levels of indirection inherent in object-oriented programs, you traded the convenience of an interpreted object-oriented program for a considerable degradation in execution speed. But today, because of desktop computers' dramatic increase in graphics and computing power, execution speeds of compiled object-oriented programs compare favorably with those of compiled programs written in procedural languages such as C and Pascal.

The basic concepts of OOP are relatively simple, although it's not so simple to apply them in practice. The first, and probably most important, concept is that you can no longer separate your data from the procedures that manipulate the data.

Procedural languages, by definition, emphasize procedures, with the result that although a data structure is defined in one place only, the program may contain many different procedures to manipulate that structure. And if you change the data structure in the course of debugging or balancing the system, you will probably have to change all of the procedures in some way. You may minimize the number of such procedures by using encapsulation, but each procedure has to know the details of the data structure in order to be able to manipulate the structure.

In an object-oriented program, on the other hand, an *object* is a block of code that contains a data structure together with all of the procedures that are required to create, modify, delete, import, or export data elements. In some OOLs, these procedures are called *methods*. Other objects do not have to know how the data is represented, or how to manipulate data elements; if object B needs a piece of data contained in object A, B merely sends a message to A requesting the data element by name.

This basic idea is not new—the Modula-2 language can create such blocks of code and can specifically define the data that a block may import or



```
requestItem: itemName format: a
    "Request data from the serv
    about itemName in aDdeFor
```

	A	B	C	D
1	45	mph		
2	58	rpm		
3	71	oil		
4				

The Smalltalk/V graphic interface helps you to build *the messages that an object (such as this meter panel) will accept and act on.*

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export. However, a Modula-2 block cannot *inherit* characteristics from other blocks in the way that an object or class can.

What's different about an OOP language is that an object can be an instance of a *class* of objects that share common properties. And again, a class can inherit the attributes and properties of a more general class. For example, the general class VEHICLE might have the properties of being able to travel from place to place, having a propulsion system, and being able to carry one or more passengers. Subclasses AUTOMOBILE and AIRPLANE would automatically inherit these properties, and in addition would have their own attributes. The specific properties of the automobile subclass might include having four wheels, a steering wheel, and two or four doors.

A system function might send a message to the AUTOMOBILE object, ordering it to take *n* passengers from Boston to New York. Checking the validity of the order (message) would be the responsibility of the procedures (methods) that are part of the AUTOMOBILE object, not those of the sending object.

The class concept is central to OOP. A class is a template for creating individual objects that behave in a similar manner; and because a class is a mechanism for abstraction, an object-oriented system will have many classes arranged hierarchically. Toward the top of the tree you'll find classes with very general characteristics that apply to many other, more specialized, classes; at the bottom of the tree will be the classes that inherit some of their characteristics from other classes, but also have very specific characteristics of their own.

Normally, a class inherits characteristics only from the class immediately above it in the hierarchy. However, some OOLs support the idea of *multiple inheritance*; that is, a class can inherit characteristics from several other superior classes that don't necessarily have to be on the same branch of the tree. Thus, if you create a new object, you don't have to describe *all* of its characteristics—you just have to define the ways in which it is different from classes you've already defined.

To make effective use of OOP techniques requires quite a drastic shift in the way we view programming. Mark Mullin (**Ref 1**) gives a good description of the shift: "...you must stop viewing programs as large blocks of instructions that drive the computer around. Instead you are dealing with a world where packets of data drive pieces of the program around. No longer do programs control things; now we deal with objects who [*sic*] do things. Control has been distributed to objects that send out messages to have things done."

There are several good reasons why you should start experimenting with OOP, even though it may take you several months to break free of the viewpoints that are inherent in simple procedural languages. One reason is that object-oriented techniques reduce the number of names (of variables, structures, and functions) that you have to remember in order to keep a clear vision of what's going on in the system. P J Plauger, a chief engineer at Intermetrics Inc, estimates that the proliferation of names begins to impair your control over a C program when program size reaches 10,000 to 50,000 lines of code. But if you're writing in C++, he says, and making full use of OOP techniques, the program can easily reach 100,000 lines before the number of names starts to overwhelm you.

Another good reason for making the switch to object-oriented techniques is that your systems become more easily extensible and modifiable as your customers' needs

Explore the bookstores

For anyone who is pondering any serious work in OOP, Mark Mullins's *Object-Oriented Program Design With Examples in C++* (**Ref 1**), is lucid and readable. In addition to being an excellent starting point for C programmers, the book is also very practical—the examples are all set in the context of designing a corporate database to track inventory, suppliers, customers, and employees. Topics range from design issues, such as how to design classes and objects (strategy), to implementation issues, such as how to derive specialized classes from general classes, and how to implement constructor and destructor functions (tactics).

Among the recent magazine articles, you'll probably find John Dlugosz's article (**Ref 2**) useful if you want an introduction to OOP without learning a whole new language. In fact, almost the whole of the August, 1989 issue of *Computer Language* is devoted to OOP topics and contains much that will be helpful, even if you're only mildly interested and don't intend to get involved yet.

change. You can add new objects to a class, or derive new classes that inherit most of their characteristics from classes that you've already defined. Larry Rice, a product manager of integration products with Valid Logic Systems, says that this characteristic of object-oriented systems is particularly valuable because it allows both designers and customers to extend the features of Valid Logic's ASIC-design tools to meet new needs and to extend the applicability of a tool to new devices.

Also, if you're involved with parallel or multiprocessor computers, you may find OOP techniques a great help in mapping concurrent processes onto multiple processors.

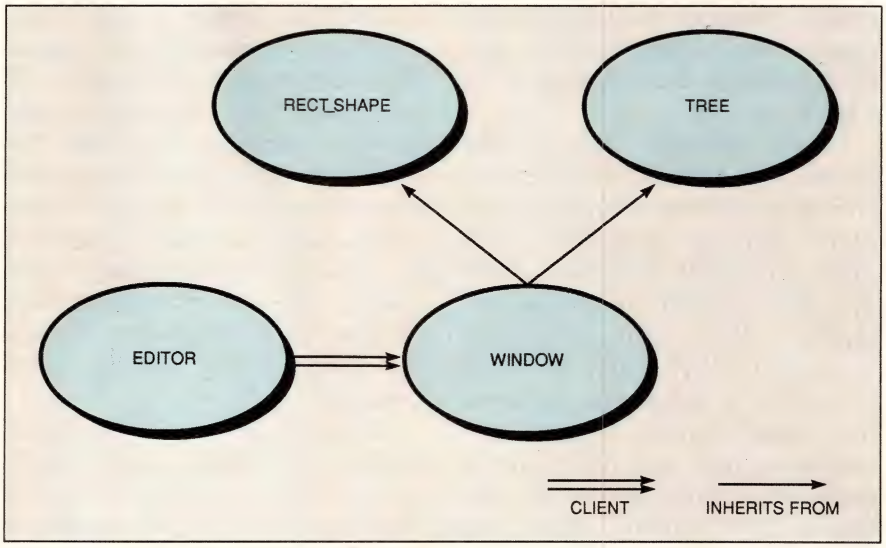

Fig 1—Multiple inheritance allows *the class WINDOW to inherit graphical properties from class RECT_SHAPE and nesting properties from class TREE. Eiffel allows you to rename properties for the convenience of a user (EDITOR) of windows.*

Watch your languages

Which of the object-oriented languages (OOLs) you select may depend upon your background in other languages. The purists say that you should choose Smalltalk, Actor, or Eiffel, all of which are designed from the ground up as object-oriented languages and make maximum use of object-oriented concepts.

Smalltalk is probably the best known OOL. Alan Kay and his colleagues at the Xerox PARC (Palo Alto Research Center, Palo Alto, CA) developed the language, which originally ran only on large computers. Digitalk Inc has, in the last few years, produced versions of Smalltalk/V for the IBM PC ($99.95), for 80286-based machines running under PC-DOS ($199.95), and for Macintosh computers ($199.95). Smalltalk is implemented as an interpreter, and is therefore generally considered a single-user language. It gives you all the features of a pure OOL, but you pay the price of an interpreter's lower execution speed. If you're going to be working with the OS/2 Presentation Manager graphic interface, keep an eye out for the appearance of a fully compiled version of Smalltalk that will greatly simplify your task—it's in development, but no details have yet been released.

Interactive Software's Eiffel is a complete development system that runs on most Unix machines and generates standard C as an intermediate output language. Prices start at $995 for a version that runs under Xenix on an 80386-based computer. The Eiffel language provides all of the features of a pure OOL, including generic classes and multiple inheritance; the latter feature allows you to define a new class that inherits characteristics from more than one parent class. If you want to create nested windows, for example, you could define a class WINDOW, which would inherit its nesting capabilities from TREE, (a standard library class describing tree implementations) and its graphic features from RECTANGLE (another library class) (**Fig 1**).

If your previous programming experience has been in Basic, Fortran, or Cobol, a pure OOL may be your best choice. You'll have to learn the language from scratch, so it may take quite a while before you're comfortable with it. However, if you are an experienced C or Pascal programmer, there are object-oriented extensions to these languages that may ease your transition to the world of objects. Be aware, however, that at first you'll find yourself building a standard system in an OOL—you won't start writing true object-oriented code until you're familiar enough with the underlying concepts to make the switch in viewpoint that Mullin describes.

If you're a Pascal expert, and want to build on your expertise, then Borland's Turbo Pascal 5.5 is, at present, your only choice. This version, which is source-code compatible with versions 4.0 and 5.0, provides inheritance, static and dynamic objects, constructors and destructors for creating new objects or deleting old ones, and many other object-oriented features. You can upgrade from earlier versions (from 5.0 for $34.95, or from 4.0 for $75). Turbo Pascal 5.5 Professional includes Turbo Debugger and an object inspector and hierarchy browser; an upgrade from 5.0 or

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If you're a C programmer, there's a whole raft of C++ implementations. AT&T's C++ version 2.0 is a preprocessor that adds object-oriented facilities to the standard C language, and most implementations are preprocessors that follow the standards set by AT&T's version 2.0. There's also at least one implementation that generates native code for IBM PCs and compatibles. Version 2.0 of the language supports multiple inheritance, strong typing, and dynamic binding. However, in keeping with traditional C techniques, all memory management and garbage collection is left to the programmer, whereas in pure OOLs memory management and garbage collection are performed automatically.

At the top of the C++ line is HCR Corp's HCR/C++ ($995) for 80386-based Unix machines. A complete development system that implements the AT&T release 2.0 of C++, it comes with dbXtra (a source-level debugger that lets you debug the C++ code via a window interface), release notes, a reference manual, and a library manual.

Objective C from Stepstone ($250 for a PC version, $2000 and up for workstations) is another development system that provides object-oriented extensions to the C language. One of its advantages is that you can mix object-oriented code with standard C. Also, unlike C++, Objective C lets you choose between static and dynamic binding, and also provides full memory-management and garbage-collection facilities. The package comes with a *make* utility and other routines that automate the complexity of releasing objects that form part of more than one system.

At a more modest price ($149.95) you can get Zortech's C++ compiler, which generates native code for IBM PCs and compatibles. The compiler does not yet support the features added to C++ by AT&T's release 2.0 (although a new release is imminent), but it comes complete with the vendor's C compiler. The C++ compiler is compatible with Microsoft's CodeView debugger, and with Zortech's own debugger, which is available at an extra cost of $89.95. You can also obtain (for $89.95) a toolkit of C++ classes covering a wide range of common programming tasks such as binary searching, time/date/clock functions, error handlers, string editing, and windows.

The general popularity of C for all kinds of applications, including real-time embedded systems, seems to give C++ an edge over pure OOLs, especially because object-oriented database managers written in C++ are already on the market. However, graphic interfaces to make life easy for end users may prove easier to implement in pure OOLs. In any event, today's languages and techniques are likely to be only the starting point of sweeping changes in our view of how best to build complex systems; the experiments and changing techniques will go on for years before any clear-cut judgments can be made.

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1. Mullin, Mark, *Object-Oriented Program Design With Examples in C++*, Addison-Wesley, Reading, MA, 1989, pg 290.

2. Dlugosz, John, "Object-oriented programming for C," *Computer Language*, August, 1989, pg 103.

3. Floyd, Michael, "A Class Act," *Dr Dobb's Journal*, April, 1989, pg 58.

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For more information . . .

For more information on the programming languages discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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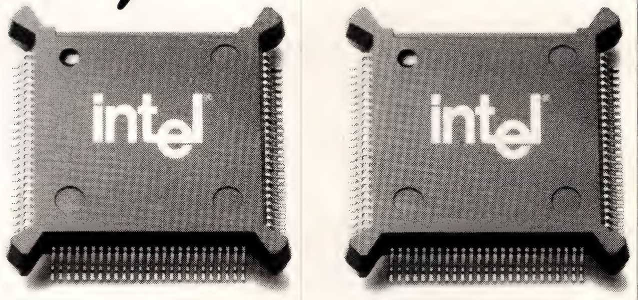

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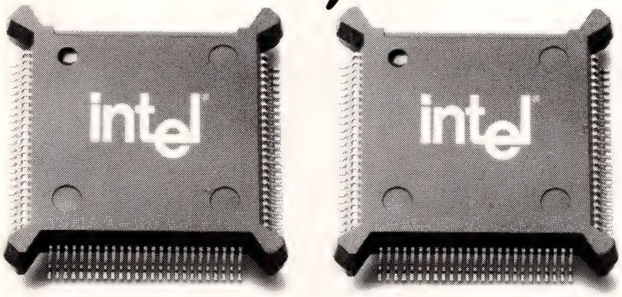

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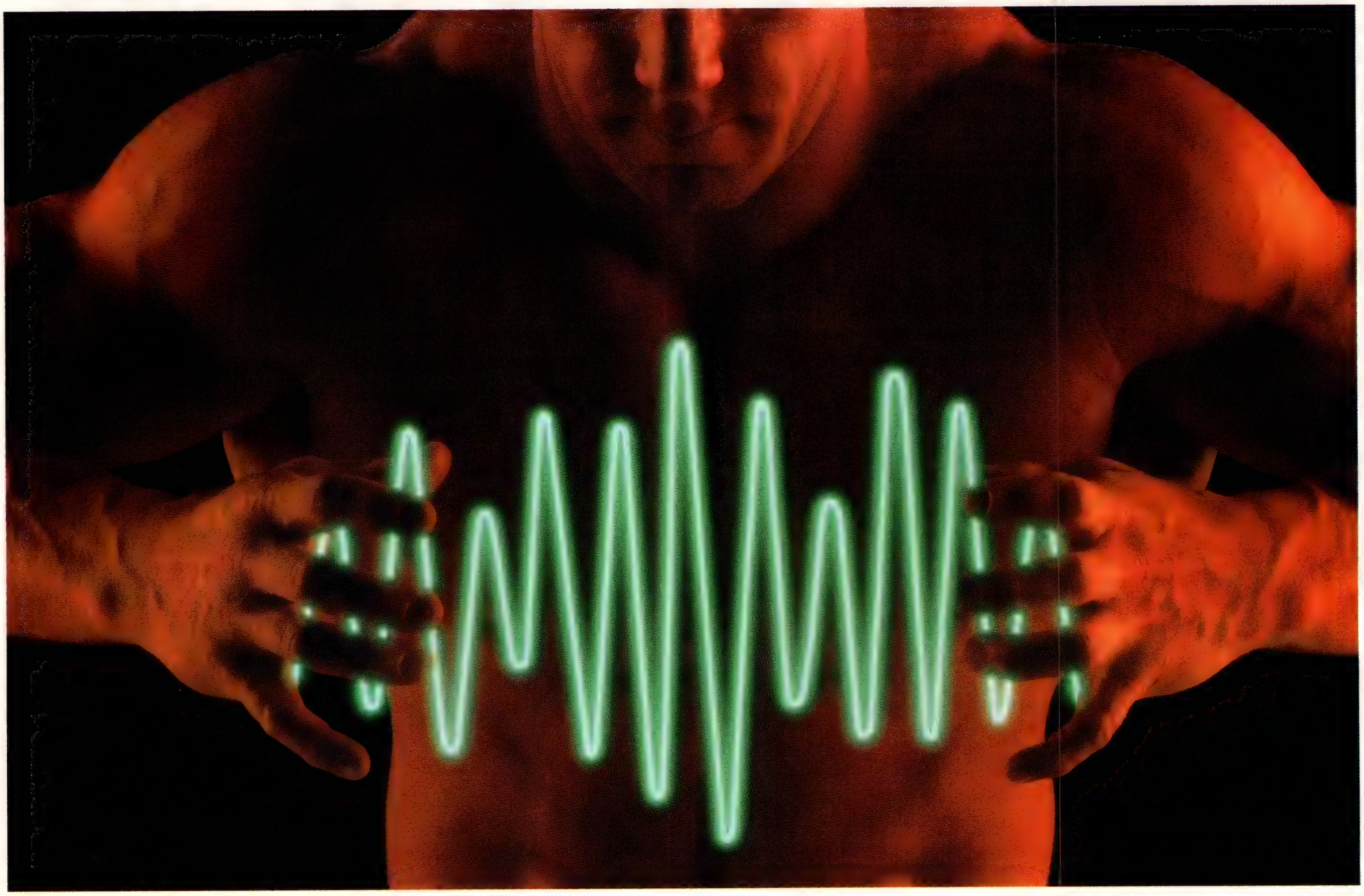

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Devices refine the art of frequency synthesis

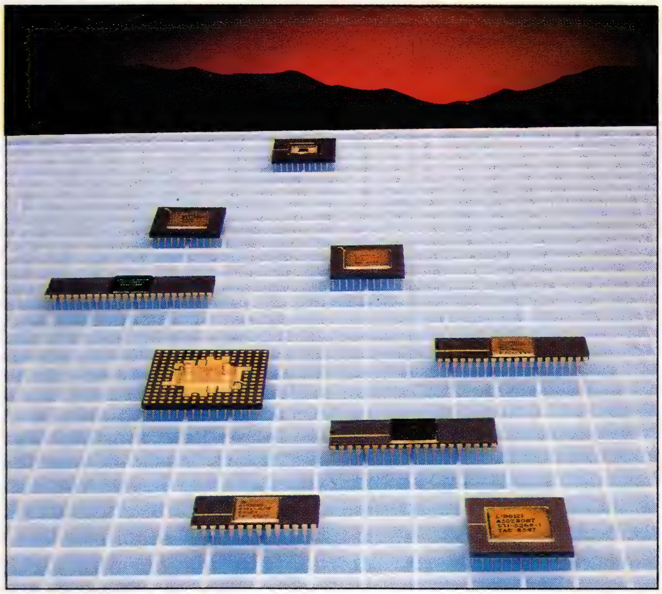
If you need a frequency synthesizer that has switching speeds in the nanoseconds and can achieve a frequency resolution of a fraction of a hertz, a direct digital synthesizer (DDS) is for you.

John A Gallant,
Associate Editor

Direct digital synthesizers (DDSs) offer many advantages over their PLL counterparts. PLLs have operating limitations based on loop bandwidths, settling times, and phase-noise tradeoffs. DDSs also have certain settling-time and phase-noise constraints, but they can attain a frequency resolution of a fraction of a hertz and switching speeds in the nanoseconds. In addition, a DDS can switch from one frequency to another in a phase-continuous manner, whereas a PLL must wait for phase transients to settle during a frequency change. These performance features make the DDS an ideal tool in spread-spectrum communications and arbitrary-waveform generation. Further, recent advances in DAC technology, memory circuits, and digital controllers have opened up applications for the DDSs that were once exclusively in the PLL domain: electronic warfare, digital data links, test-signal generators, commercial-satellite systems, and very-small-aperture-terminal systems.

To construct a basic DDS, you can use a counter that addresses a digital look-up table that contains samples of a specific waveform. The output of the look-up table drives a DAC that generates an analog representation of the waveform. This method is inflexible, however; the only way to change the waveform frequency is to alter the clock frequency that drives the counter. To escape this problem, modern DDS systems use a phase accumulator instead of a counter to generate the addresses for the look-up table.

The phase accumulator consists of a storage register that contains the frequency-step size and a digital adder with a latched output. The latched output addresses the look-up table and feeds back to one of the adder's inputs (**Fig 1**). The phase accumulator rotates a vector around a phase circle in discrete increments at a constant clock rate. An accumulator with an 8-bit resolution provides 256 discrete phase steps. The step size alters the waveform frequency according to the DDS tuning equation:



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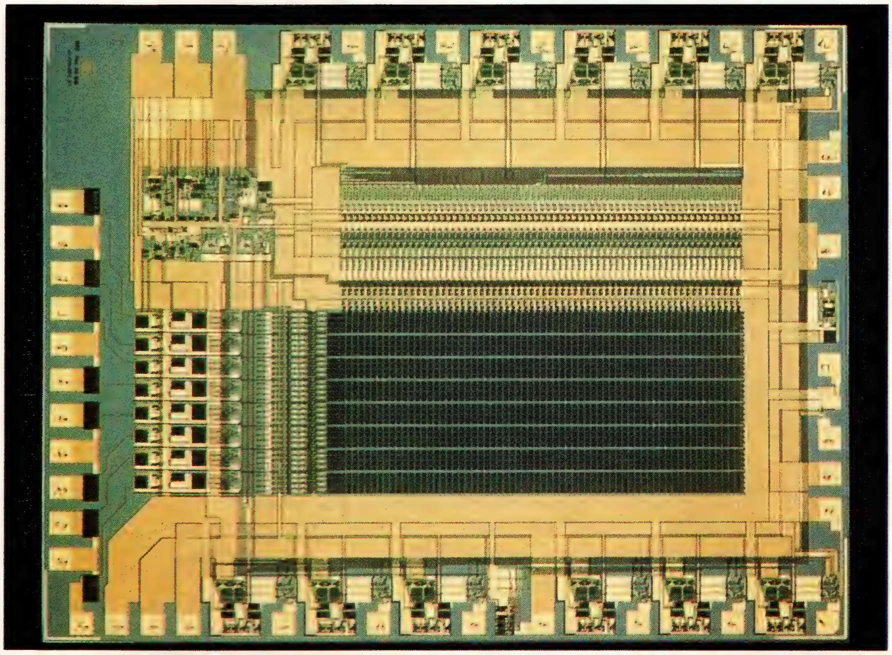
$$F_0 = M \times F_C/2^N,$$

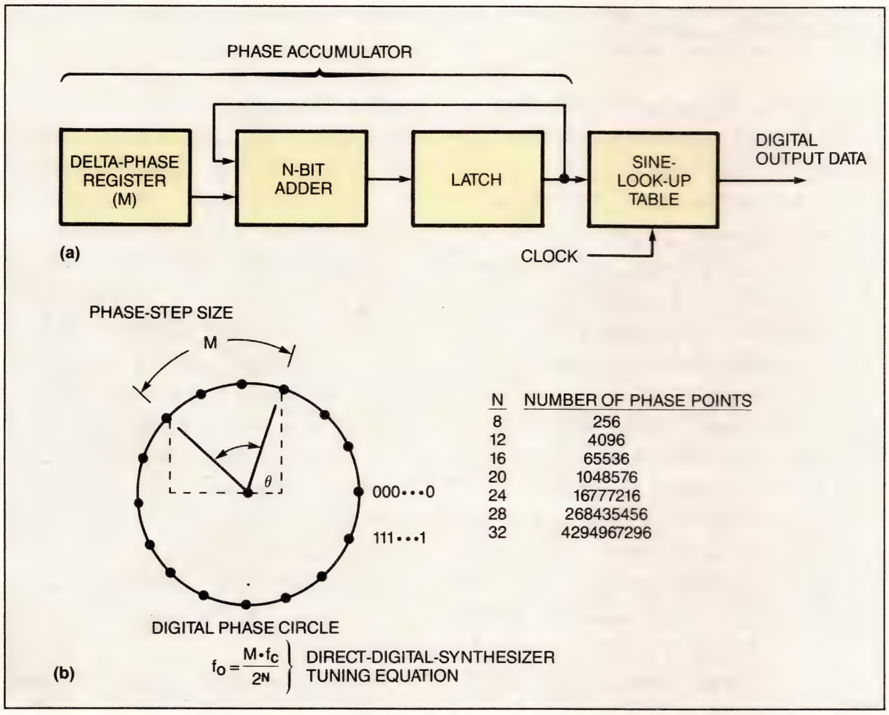
where F_0 = the output-waveform frequency; M = the step size programmed into the storage register; F_C = the clock rate; and N = the length of the accumulator in bits.

The DDS behaves as a sampled data system and therefore is subject to Nyquist's theorem. Because you must take a minimum of two samples to define a sine wave, the maximum frequency that a DDS can generate is half the clock frequency (½f_C/2). In practice, however, the maximum sine-wave frequency usually is limited to 40% of the clock rate to provide enough of a margin for an output filter to suppress aliasing frequencies.



A mask-programmable ROM can serve as the sine-wave look-up table. *The GaAs 14GX048 ROM from GigaBit Logic has a 512 × 8-bit organization and a 1-nsec access time.*

The DRFS-350 Number Controlled Modulated Oscillator (NCMO) from Digital RF Solutions Corp represents a CMOS solution for employing a phase accumulator in a DDS system. The NCMO, which costs $110 (100), operates with clock frequencies of 0 to 40 MHz. The phase accumulator is 24 bits long, which results in a tuning resolution of 0.5 Hz when using a 10-MHz clock. You can hop between two addresses in two clock periods (200 nsec when operating at 10 MHz). You can also cascade multiple devices in applications that require finer resolution.



N	NUMBER OF PHASE POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

Fig 1—Modern DDS systems employ a phase accumulator *with an N-bit adder to address a waveform look-up table **(a)**. The digital number (M) stored in the phase register defines the step size on a phase circle with N discrete phase increments **(b)**.*

In addition, the NCMO contains modulation units integrated onto the IC so that the software can perform frequency and phase modulation. A frequency modulator in front of the phase accumulator has 24 bits of resolution and provides a modulation bandwidth equal to the tuning bandwidth. A phase modulator following the accumulator uses the 12 most significant bits, which provides 4096 phase points (0.09° resolution).

An output-mode selector lets you reduce the size of the waveform map for waveforms with odd symmetry, where the second half of the waveform is a mirror image of the first half (such as a cosine wave). An up/down mode progresses through the first half of the cycle and then reverses the count direction in midcycle to access the waveform in reverse order for the second half. In addition, you can input the step size (M) through three tuning methods: a 24-bit, parallel-input mode; three 8-bit, data-bus words; or a quadrature-clocked serial input for optical encoders. The unit dissipates a maximum of 300 mW and comes in an 84-pin plastic leaded chip carrier (PLCC) or ceramic leaded chip carrier.

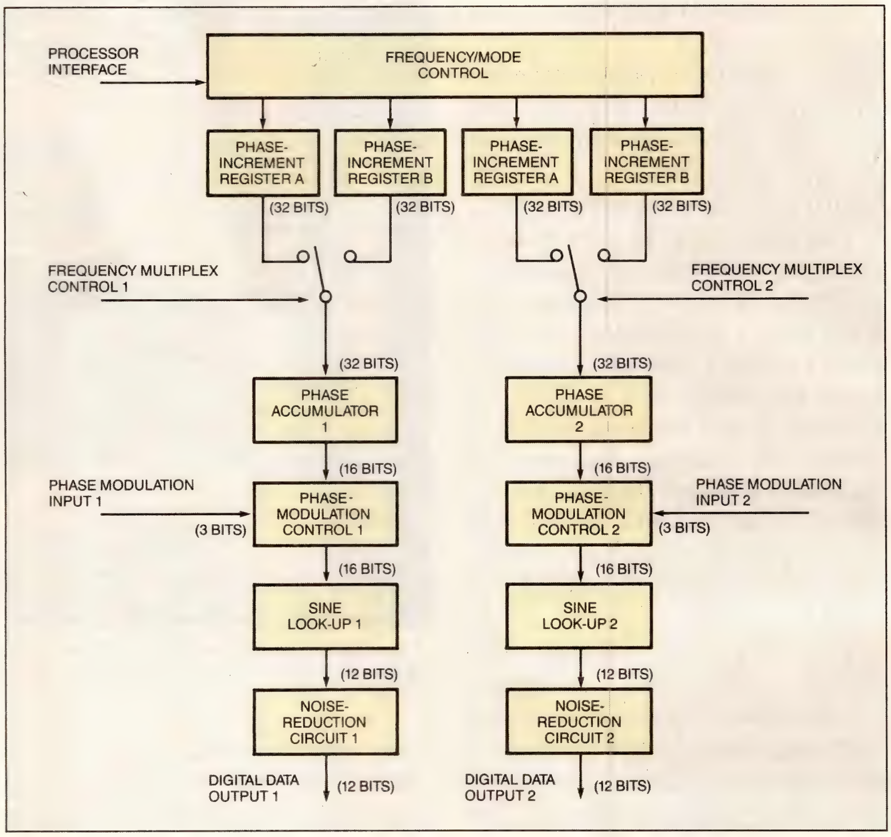


***Fig 2—DDS ICs include many features on a single chip.** The Q2334 from Qualcomm contains dual sine-wave look-up tables and two independent DDS functions with BFSK and quad PSK capabilities.*

Minimize spurious signals

The output of the NCMO can drive a commercially available RAM or ROM or one of the company's sinusoidal waveform-map ICs. The DRFS-3252 and DRFS-3254 ($40 (100)) are CMOS ROMs with 8-bit data outputs and 12 address inputs. A memory unit with at least two more address bits than data bits eliminates spurious signals generated because of phase truncation. These ROMs provide 25-nsec access to half of a cosine wave. The company also offers the DRFS 3253 ($40 (100)), which provides 25-nsec access to full cosine or sine waves with an 8-bit data output and eight address inputs. The units dissipate 330 mW and come in a 24-pin DIP. The waveform maps don't have registered outputs; they're designed to reduce the in-band spurious signals that are caused by the amplitude-quantization errors produced in commercial memory units.

Another way to minimize spurious signals due to amplitude-quantization errors is to integrate the waveform look-up table onto the phase-accumulator chip. On its 30-MHz Q2334 IC ($98 (100)), Qualcomm Inc includes a sine-wave look-up table with a 16-bit address input and a 12-bit data output. In fact, the IC contains two independent DDS functions that are controlled by a single microcontroller (μC) interface (**Fig 2**). The chip contains two 32-bit phase accumulators that can operate at 30-MHz clock rates. When operating at 30 MHz, the IC provides a frequency resolution of 0.007 Hz. The company specifies the amplitude-quantization spurs to be 72 dB below the carrier amplitude.

Each channel in the Q2334 has two double-buffered, phase-increment registers. A synchronous-control register multiplexes the data in the registers into the accumulator. A μC can load each of the phase-increment registers with a frequency increment for binary frequency-shift keying (BFSK).

Because the multiplex operation is synchronous with the clock frequency, the DDS can generate the BFSK signal with smooth phase changes, which reduces transient spurious signals during switching. The ability to quickly switch frequencies while maintaining phase coherency is one of the main advantages the DDS has over PLL techniques. The Q2334 also has phase-modulation inputs that can synchronously modify the output sine wave in 45° increments to generate phase-shift-keyed (PSK) signals.

Stanford Telecommunications Inc offers a number of numerically coded oscillators (NCOs) with a phase modulator and a waveform look-up table on the IC. The STEL-1175, which costs $100 (100), is one of the company's latest CMOS devices and operates with clock frequencies as high as 60 MHz. The device has a 32-bit phase accumulator that provides a frequency resolution of 0.014 Hz when operating at 60 MHz.

A selectable sine- or cosine-waveform look-up table has a 12-bit data output. You can phase modulate the output of the accumulator with 12 bits of resolution (0.09°). In addi-

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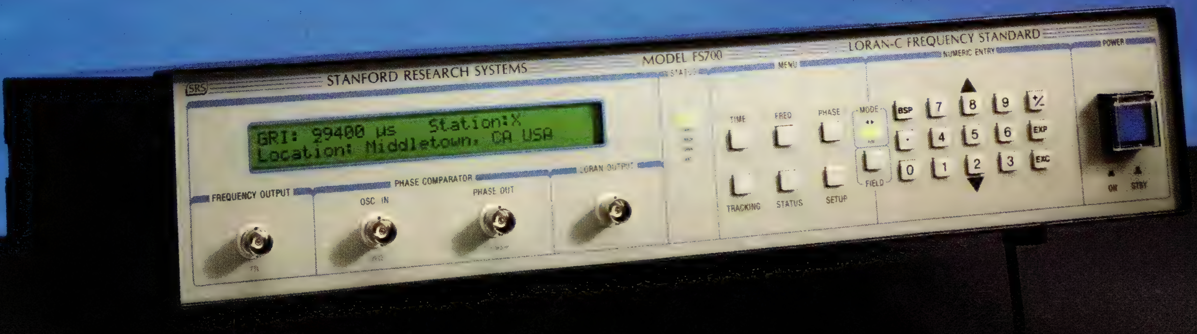
Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.



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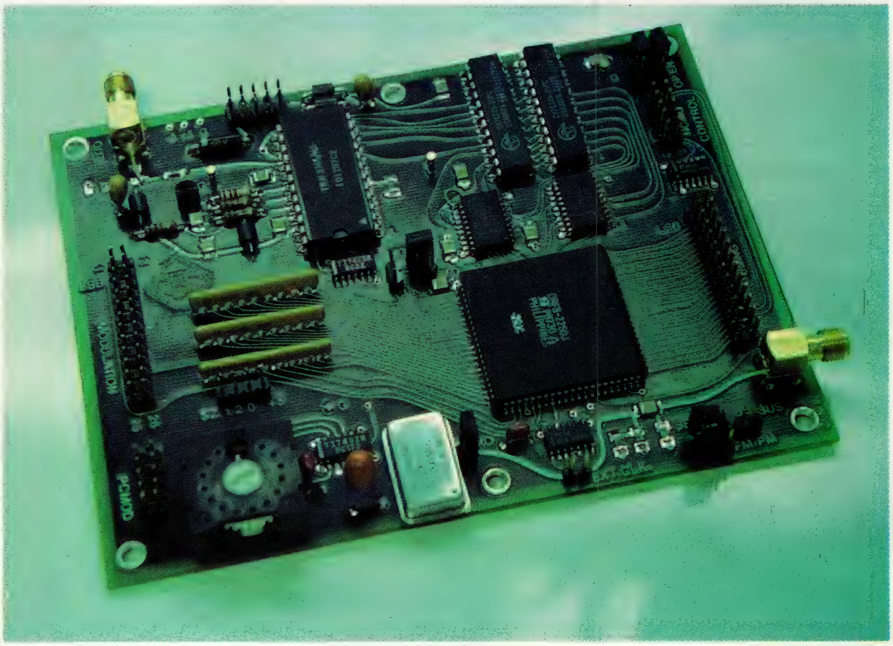
tion, you can switch in as fast as 66 nsec. The IC has two multiplexed, step-size storage registers for BFSK signal generation; these registers interface to a μC via an 8-bit bus.

The company also offers an ECL NCO, the STEL-2172, for $625 (100). This device has a 28-bit phase accumulator and can operate at clock rates as high as 300 MHz. It can generate a 130-MHz, sine-wave frequency with 1-Hz frequency resolution. Its on-chip, sine-wave look-up table provides an 8-bit data output. Although the device uses ECL technology, you interface with the unit via TTL-compatible control inputs. The unit switches in 110 nsec and comes in a 156-pin, ceramic pin-grid array with heat-sink mounting studs.

In the first quarter of 1990, Stanford Telecommunications will also offer a GaAs NCO, the STEL-2173. The NCO contains a 32-bit phase accumulator, which can provide a frequency resolution of 0.2 Hz when operating at 858 MHz. The device operates at clock frequencies as high as 1 GHz. Its on-chip look-up table provides either 8-bit sine- or cosine-output data. Every fourth clock period, you can switch between frequencies using ECL-compatible control lines.



***A board-level system solution can minimize spurious signals** created by many direct-digital-synthesizer sources. The DX2070 (Digital RF Solutions Corp) operates with a 20-MHz clock and features a 70-dB spurious-free dynamic range.*

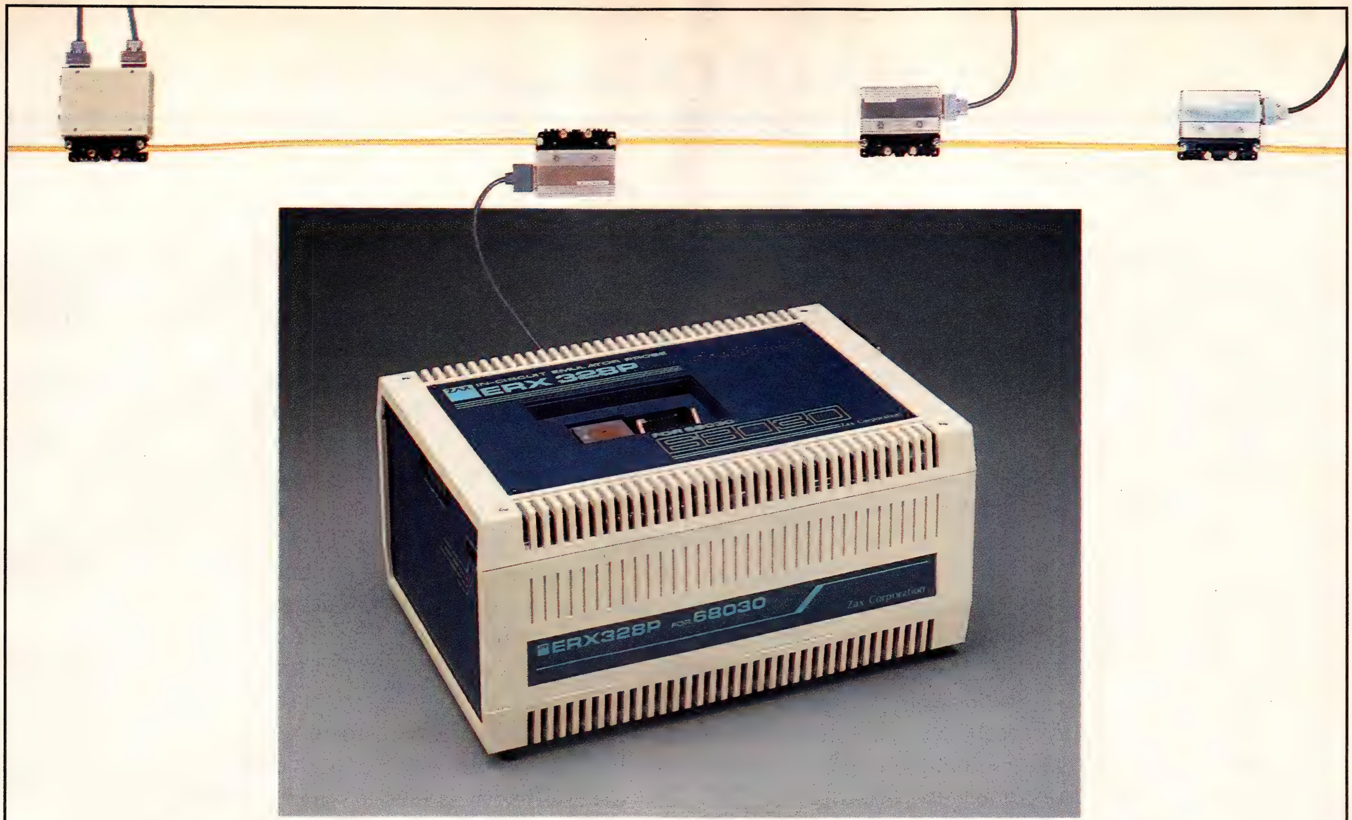
GaAs chips for those special needs

GigaBit Logic also offers some GaAs chips for wide-bandwidth DDS systems. The 10G102 and 10G103 32-bit, phase-accumulator chips ($209 (1000)) can operate at 750 MHz. (1-GHz versions will be available by the end of the year.) The accumulator uses a 32-bit pipelined adder that computes a 2-bit addition on each clock cycle. The pipelined architecture reduces capacitive loading on the clock line and maintains a chip power dissipation of less than 4.5W. The adder requires 17 clock cycles plus a 500-psec delay time to complete an addition. Therefore, the time required to switch frequencies is slightly longer than 17 clock periods (approximately 18 nsec when operating at 1 GHz).

The 12 MSBs of the phase accumulator drive an on-chip, time-aligned output register that provides 12 address outputs for one of the company's 14GX048 GaAs ROM ICs. The mask-programmable ROMs ($104 (1000)) are arranged in a 512×8-bit organization, have typical access times of 1 nsec, and dissipate less than 0.8W. Because the 10G102 phase-accumulator chip contains 1's complement output-logic circuitry, it can generate a full sine wave with a ROM containing data for only one quadrant of a sine or cosine wave. The 10G103 doesn't have 1's complement circuitry, so it's typically used with a full sine-wave ROM. Custom ROM patterns are available with a minimum order of 25 units and a $4000 nonrecurring engineering cost.

By now you may be asking if any DACs are designed for DDS applications. The DAC is an essential part of the DDS system, and it's also a major contributor to in-band spurious signals. The sampling theorem only predicts that a minimum aliasing frequency will occur at $f_C - f_0$, a frequency that can be suppressed by a low-pass output filter. However, circuit nonlinearities can contribute to spurious signals within the filter's bandpass. To minimize in-band spurious signals, use a DAC with good integral and differential nonlinearity specifications.

Time skew is another contributor to in-band spurious signals. Time skew results when the arrival times of the input bits to the DAC differ by a few nanoseconds. If the skew is substantial compared with the DAC's settling time, the DAC's output will respond to the changing input data. Latching the data before applying it to the DAC removes any system contribution to the time skew; however, the DAC's internal time skew is a result of the



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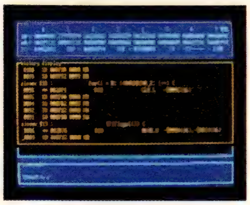

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design, and thus each individual design is subject to scrutiny.

Glitch energy also creates in-band spurious signals. The term refers to the spike that occurs on the analog output while a transition settles. This spike is measured in volt-seconds (V·sec)—a measure of impulse area rather than energy. (Thus, "glitch energy" is actually a misnomer, because the unit of measurement isn't in energy.) Both the time skew and the bandwidth of the analog portion of the DAC determine the amount of glitch energy. A high-speed DAC with no time skew should exhibit smaller glitch pulses. In addition, the output stage should be balanced so that toggles between the two analog-output levels are mirror images of each other.

TRW's TDC1012 12-bit DAC is often used in TTL and CMOS DDS applications. The unit costs between $28 and $56 (1000) and can convert digital data into an analog current at 20M samples/sec. The DAC specifies a maximum settling time of 35 nsec to be within ±½ LSB for a full-scale step change, and it features a maximum glitch energy of 40 pV·sec without a deglitching circuit. The device has a ±½ LSB specification for both integral and differential linearity. It provides 40 mA of complementary output current, which can produce an output of 1V when driving a double-terminated, 50Ω transmission line. To eliminate time skew, the DAC also has registered inputs with feedthrough control.

Analog Device's AD9712 and AD9713 are 12-bit DACs for DDS applications. Each costs ($14 (100)) in a plastic DIP. The AD9712 is an ECL-compatible device that converts data at 100M samples/sec; the AD9713 is a TTL-compatible device that converts data at 80M samples/sec. Both devices feature 100 pV·sec glitch energy and output settling times of 30 nsec to be within ±1 LSB of a full-scale step change. They have a maximum-differential-nonlinearity specification of 0.75 LSB and maximum integral nonlinearity of 2 LSB. In addition, the DACs feature transparent latches on the inputs to eliminate time skew.

For wide-bandwidth applications, TriQuint's 8-bit GaAs TQ6111 ($199 (100)) and TQ6112 ($299 (100)) DACs can operate at 600M samples/sec and 1G samples/sec, respectively. These DACs feature differential nonlinearity of ±0.5 LSB and glitch energy of <25 pV·sec. The settling time is 1 nsec to be within 1% of the full-scale step value. The DAC accepts ECL-compatible data into an on-chip, 2-to-1 data multiplexer and delivers a 1V full-scale output into complementary 50Ω loads. The device is available in die form or in a 44-pin ceramic leaded chip carrier. The TQ6111 typically consumes 2.5W, and the TQ112 typically dissipates 3.5W.

A total package relieves headaches

Although manufacturers of DDS ICs often quote a spurious-free dynamic range for their products, the system's layout has a substantial ef-

For more information . . .

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fect on the spurious-signal performance. Real-world bugaboos such as clock feedthrough, faulty grounds, and inadequate power-supply decoupling can also contribute to in-band spurious signals. With so many factors affecting the device's performance, it's not surprising that many developers want a total, packaged solution to their DDS problems.

Most manufacturers of phase-accumulator ICs offer total system solutions for their digital-frequency-synthesizer products. The systems are either board-level or modular packages that specify an operating bandwidth, a maximum clock frequency, a frequency-step resolution, a switching speed, and a spurious--free dynamic range. In fact, Stanford Telecommunications' STEL-1375 is a complete digital frequency synthesizer in a DIP package that measures 1.7×0.9 in. and costs $435 (100). The thick-film hybrid uses the STEL-1175 MNCO (modulated NCO) driving a 10-bit CX20202A-1 DAC from Sony Corp (Cypress, CA).

The hybrid specifies an operating bandwidth from 0 to 25 MHz and a maximum clock frequency of 60 MHz. It provides a frequency-step resolution of 0.014 Hz, and it can be phase and frequency modulated at 25% of the clock rate. The hybrid can operate from 0 to 70°C and has a measured spurious-free dynamic range of 60 dB.

Digital RF Solutions offers a variety of board-level digital frequency synthesizers that utilize the DRFS-3250 NCMO chip. The DRFS-VR1070 ($995 (100)), for example, has an operating bandwidth of 3.3 MHz when using either an on-board or external 10-MHz clock frequency. It uses a patent-pending, variable-resolution technique to provide exact decimal-frequency resolution that isn't constrained by the 2^N factor in the DDS tuning equation. Tuning resolution is specified as 1.000000 Hz; settling time for switching is 500 nsec max. The unit uses an 8-bit DAC to achieve a spurious-free dynamic range of greater than 70 dB.

One of the most prolific manufacturers of modular and board-level digital frequency synthesizers is Sciteq Electronics Inc. The company uses either commercially available or custom DDS ICs in products that cover a wide range of operating bandwidths. The company also includes phase-noise plots in dBc/Hz vs carrier-offset frequency as well as spurious-signal performance. Because the phase noise of the synthesized waveform is directly related to the phase noise of the clock signal, the products use a SAW resonator, which is phase locked to either an onboard reference or an external 10-MHz reference, to generate the clock frequency.

The company's VDS-3125 ($5700 each), for example, is a digital frequency synthesizer on a 6U VMEbus card. The device features an operating bandwidth of 110 MHz; a worst case, spurious-free dynamic range of 40 dB; a frequency-step resolution of 0.93 Hz; a 150-nsec switching speed; and an optional upconversion unit that translates the bandwidth between 540 and 600 MHz. The board costs $5700 and consumes less than 20W.

The Multigen ($2000 each) is a digital frequency synthesizer for the Industry Standard Architecture (ISA) bus. The card has an operating bandwidth of 8 MHz, a spurious-free dynamic range of 50 dB, a frequency-step resolution of 0.1 Hz, a switching speed of less than 0.5 µsec, and a phase generator that can increment the phase in 0.18° steps. To control the synthesizer, the board also has a 68000 µP and 2k bytes of RAM, which can receive commands from either the ISA bus or an IEEE-488 interface.

The ADS-2 is a GaAs digital frequency synthesizer in a 7×5×1.25-in. modular housing. The unit's output is ac coupled to provide an operating bandwidth from 1 MHz to either 180 or 300 MHz. It has a frequency-step resolution less than 0.15 Hz, a spurious-free dynamic range of 45 dB, and a switching speed of 20 nsec. In 1990, the company plans to offer the product, which costs $4000, in a thick-film hybrid that will occupy approximately 2 in^2.

Sciteq also offers a variety of synthesized sources that combine a DDS with a PLL to achieve DDS performance figures in different spectral bandwidths. These units also can employ BCD dividers to achieve exact decimal-frequency resolution.

Compare apples with apples

A word of caution when comparing the spurious performance of digital frequency synthesizers: to achieve wider-bandwidth synthesizers, manufacturers must use DACs with smaller bit precision. The conventional wisdom in the DDS community is that, for every quantization bit, nonharmonic spurious signals will be suppressed 6 dB below the carrier frequency.

With an 8-bit DAC, you can expect nonharmonic spurs that are 48 db (6×8) below the carrier frequency. To achieve 60-dBc spurious signals, you need a 10-bit DAC. Often, a 100-MHz digital frequency synthesizer that uses an 8-bit DAC and features a 50-dB dynamic range can achieve a better spurious performance than a 50-MHz synthesizer with a 10-bit DAC that has a 60-dB dynamic range.

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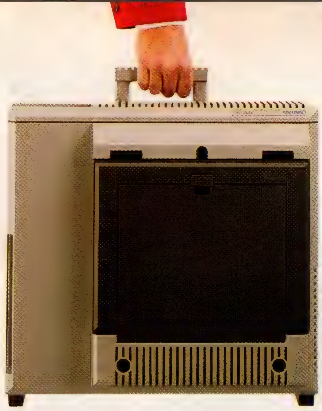
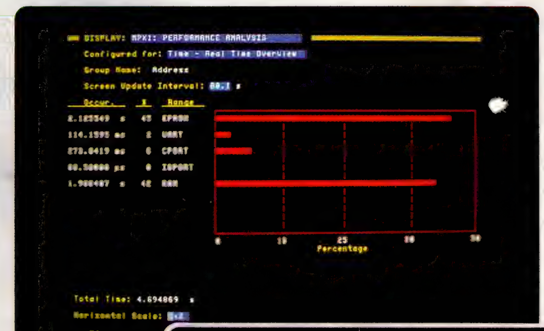
CIRCLE NO 89

TEK'S NEW PRISM 3000 FAMILY BREAKS THE LOGIC ANALYSIS BARRIER.



The new Prism 3000 Series is nothing less than a breakthrough in the evolution of logic analysis: once you see what it can do, you may scarcely imagine doing without it.

Now digital designers and integrators can start with all the speed, channels and memory depth they need— without tradeoffs. They can mix-and-match tools for their specific needs, including 8, 16 and 32-bit microprocessor debug modules brimming with features never before possible in a logic analyzer. They can add other modules, such as for high-speed timing and waveform analysis, later.

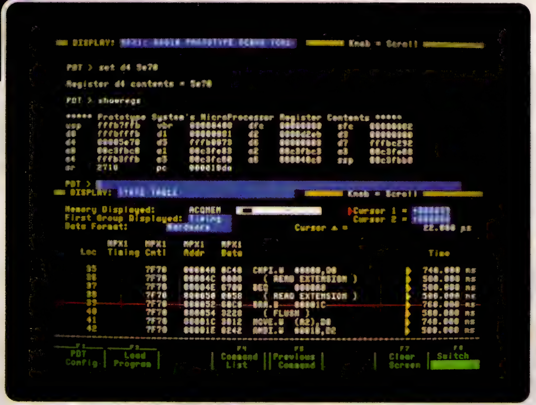


```
DISPLAY: MPX1: PERFORMANCE ANALYSIS
  Configured for: Time - Real Time Overview
  Group Name:  Address
  Screen Update Interval: 00.1 s
 Occur.        %   Range
2.123549  s   45   EPROM
114.1995  ms   2   UART
273.0419  ms   6   CPORT
00.50000  µs   0   IOPORT
1.900487  s   42   RAM

 Total Time: 4.694869  s
 Horizontal Scale: [illegible]
    F1
  Begin
 Sampling
```

You can view 200 MHz timing and 8K of state data per channel, all time-correlated and integrated on the same display.

Observe data from multiple microprocessors or time-bases simultaneously. Set up



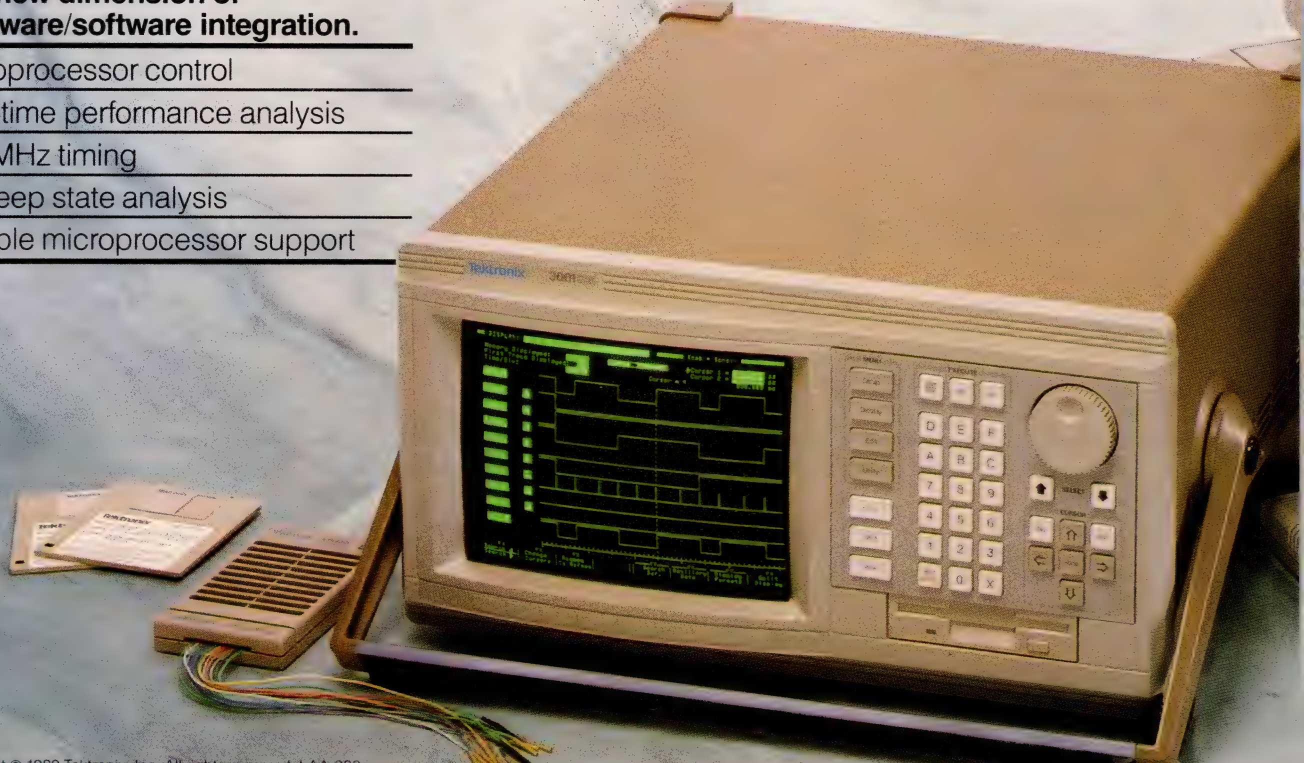
```
DISPLAY: [illegible]                          Knob = Scroll

 PDT > set d4 5e70
 Register d4 contents = 5e70
 PDT > showregs
 ***** Prototype System's MicroProcessor Register Contents *****
 usp   fffb7ffb   vbr   00000400   dfc   00000000   sfc   00000002
 d0    fffbfffb   d1    00000001   d2    0000d2eb   d3    00000000
 d4    00005e70   d5    fffb0078   d6    00000000   d7    fffbc292
 a0    00c3fbc0   a1    00c3fe03   a2    00c3fbc3   a3    00c3fe00
 a4    fffb3ffb   a5    00c3fc00   a6    000040c0   ssp   00c3fbb0
 sr    2710       pc    000010da
 PDT >
DISPLAY: STATE TABLE                          Knob = Scroll
 Memory Displayed:        ACQMEM                Cursor 1 = [illegible]
 First Group Displayed:   Timing                Cursor 2 = [illegible]
 Data Format:           Hardware          Cursor Δ =          22.000 µs
         MPX1    MPX1    MPX1    MPX1
   Loc  Timing   Cntl    Addr    Data                            Time
    35           7F70   00004A  0C40  CMPI.W  00000,D0         740.000 ns
    36           7F70   00004C  0000    ( READ EXTENSION )     500.000 ns
    37           7F70   00004E  6700  BEQ     000000           500.000 ns
    38           7F70   000050  0058    ( READ EXTENSION )     500.000 ns
    39           7F70   000052  60C0  BRA.B   00001C           760.000 ns
    40           7F70   000054  3220    ( FLUSH )              500.000 ns
    41           7F70   00001C  3012  MOVE.W  (A2),D0          740.000 ns
    42           7F70   00001E  0242  ANDI.W  0001E,D2         500.000 ns
    F1        F2                  F4         F5                 F7      F8
   PDT       Load             Command    Previous            Clear   Switch
  Config    Program             List      Command            Screen
```

(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.

The new dimension of hardware/software integration.

- Microprocessor control
- Real-time performance analysis
- 200 MHz timing
- 8K deep state analysis
- Multiple microprocessor support



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The Prism 3002P configuration features a slide-away keyboard and a 640x400 flat panel display that folds against the mainframe when not in use.

state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into emulator-like microprocessor *control*.

With its unprecedented Prototype Debug Tool, Prism is the first logic analyzer to let you set breakpoints, patch registers and memory, restart the system, and more—without an emulator's intrusiveness (or the long wait for new emulator availability).

Use real-time performance analysis to get a true, non-statistical view of system performance.

Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

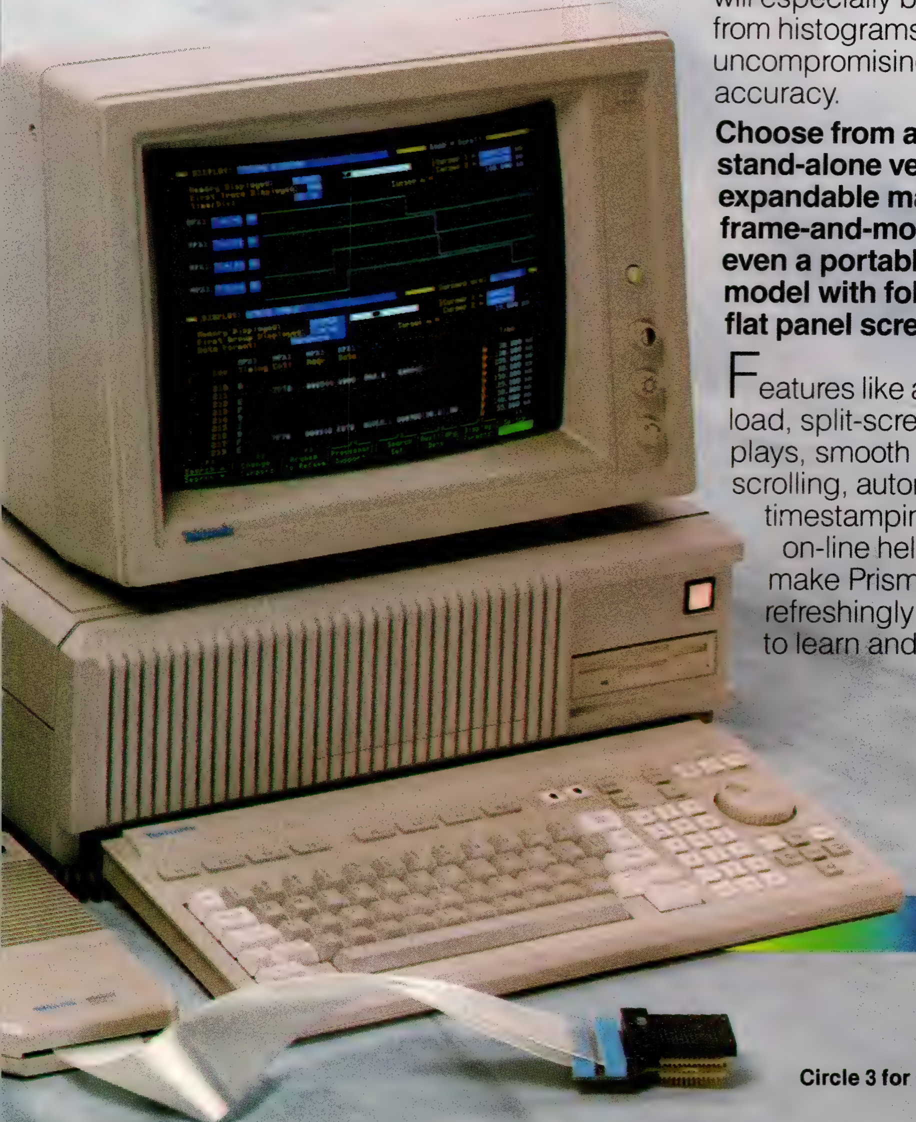
Choose from a stand-alone version, expandable mainframe-and-monitor, even a portable model with fold-up flat panel screen.

Features like autoload, split-screen displays, smooth scrolling, automatic timestamping and on-line help notes make Prism refreshingly simple to learn and use.

Complete front panel controls are included on the Prism keyboard, enabling users to move easily from one Prism mainframe to another.

The clincher? You can step into this new generation of logic analyzers at prices starting at $8600.

Call 1-800-426-2200 for our free video demo and literature packet. Prism breaks so much new ground and offers so much to build on, you owe yourself a look. For a hands-on introduction, call your Tek sales engineer soon.



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GENERAL CAPABILITIES

	ITEM	SPECIFICATIONS		CONDITIONS
CONDUCTOR	CONDUCTOR RESISTANCE	AgPd . . . . 15-50mΩ/□ AgPt . . . . 2-4mΩ/□ Au . . . . 2-4mΩ/□		—
	ADHESION	≥2.5 KGS — INITIALLY		0.6 COPPER WIRE COVERED WITH SN 2MM □ PAD
	SOLDER LEACH RESISTANCE	≥2.0 KGS AFTER AGING (@150°C, 48 HRS.)		62 SN/Pd/2 Ag SOLDER
	ITEM	STANDARD	MAX. AVAIL.	CONDITIONS
RESISTOR	RESISTOR VALUE	10Ω-2MΩ	20mΩ-20MΩ	—
	TCR	±250 PPM /°C	±100 PPM/°C	—
	TRACKING TCR	±100 PPM/°C	±10 PPM/°C	—
	LOAD WATTAGE	150mW/MM²	—	—
	RESISTOR TOLERANCE	> ±1.0%	+0.3%	—
	STABILITY: TEMPERATURE	≤ ±1.5%	—	430°C, 5 MIN.
	HUMIDITY	≤ ±2.0%	—	60°C, 95%
	HEAT CYCLE	≤ ±2.0%	—	125°C↔−40°C (10 CYCLES)
	HIGH TEMP. STORAGE	≤ ±1.5%	—	125°C, 1000 HRS.
INS.	INSULATION RESISTANCE	≥100MΩ	—	—

REPRESENTATIVES

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CIRCLE NO 306

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☐ HIGH VISIBILITY ☐ LOW POWER

☐ SURFACE-MOUNT TECHNOLOGY

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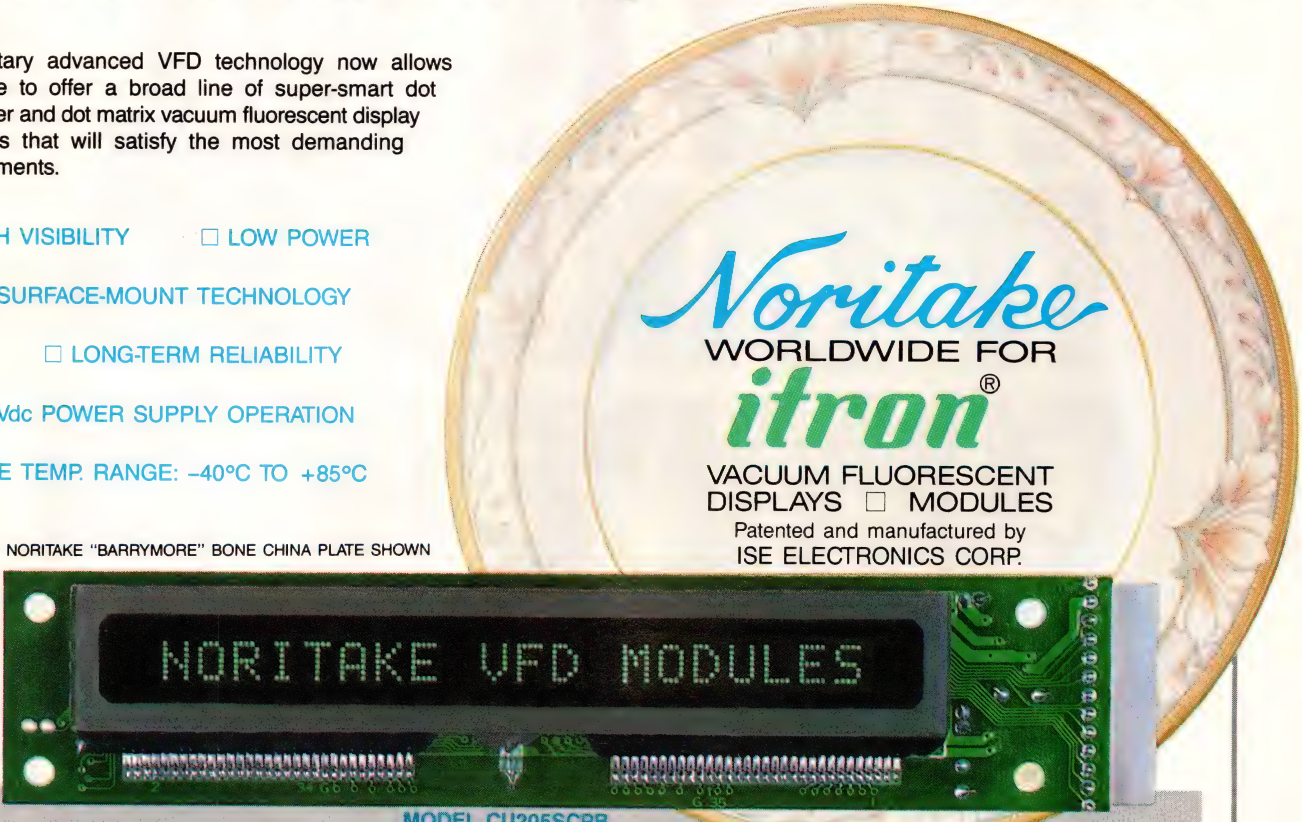
☐ 5Vdc POWER SUPPLY OPERATION

☐ WIDE TEMP. RANGE: –40°C TO +85°C



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NORITAKE "BARRYMORE" BONE CHINA PLATE SHOWN

MODEL CU205SCPB

DOT CHARACTER DISPLAY MODULES

CHARACTER FORMAT	MODEL NUMBER	NUMBER OF CHARACTERS	CHARACTER HEIGHT (MM)	INPUT (SERIAL/ PARALLEL)	BI-DIRECT BUS	★ WIDE TEMP. RANGE MODELS
5 × 7 DOT MATRIX	CU165SCPB-S	1 × 16	5.0	S/P		
	CU169SCPB-L	1 × 16	9.0	P	x	
	CU205SCPB-S	1 × 20	5.0	S/P		
	CU209SCPB-L	1 × 20	9.2	P	x	
	CU2015SCPB-L	1 × 20	15.1	P	x	
5 x 7 DOT MATRIX PLUS CURSOR	CU406SCPB-S	1 × 40	5.0	P	x	
	CU20026SCPB-S	2 × 20	5.1	P	x	x
	CU40026SCPB-S	2 × 40	5.0	P	x	x
	CU40046MCPB-S	4 × 40	5.0	S/P	x	x
	CU40066MCPB-S	6 × 40	5.0	S/P	x	x
	CU40086MCPB-S	8 × 40	5.0	P	x	x

★OPTIONAL

DOT MATRIX DISPLAY MODULES

DOT MATRIX FORMAT (DOTS/LINE × NO. OF LINES)	MODEL NUMBER	NO. OF LINES AND CHARACTERS/LINE (5x7 DOT CONFIGURATION)	GRAPHICS CAPABILITY
192 × 16 (3072 DOTS TOTAL)	GU192X16	2 × 32	YES
256 × 16 (4096 DOTS TOTAL)	GU256X16	2 × 42	YES
256 × 64 (16,384 DOTS TOTAL)	GU256X64	8 × 42	YES

The models shown are typical of the broad selection available on an immediate delivery basis. Contact our nearest sales office or representative for counsel on the best Noritake VFD for your application, as well as for details on costs, custom designs, deliveries, etc.

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CIRCLE NO 90

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It's our *lowest cost* AT solution ever. Offering you unmatched integration. So you can get to market fast.

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Like all of our products, SCAT is fully backed by the most comprehensive technical support in the industry.

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It's all you really need.

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CIRCLE NO 91

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Here's something that will help everyone sleep better. Except our competition.

At UPS, we have something that will help assure you a restful night's sleep when it comes to overnight delivery.

It's guaranteed UPS Next Day Air.*

For some time UPS has been the only company fast and reliable enough to deliver overnight to every single address coast to coast. And we guarantee it, or you don't pay for it.

What's more, we'll even guarantee delivery in the morning to the vast majority of people across the country.

And because of our efficiency, we're still able to do all of this for up to half what other companies charge.

All of which is guaranteed to give our competition a restless night's sleep.

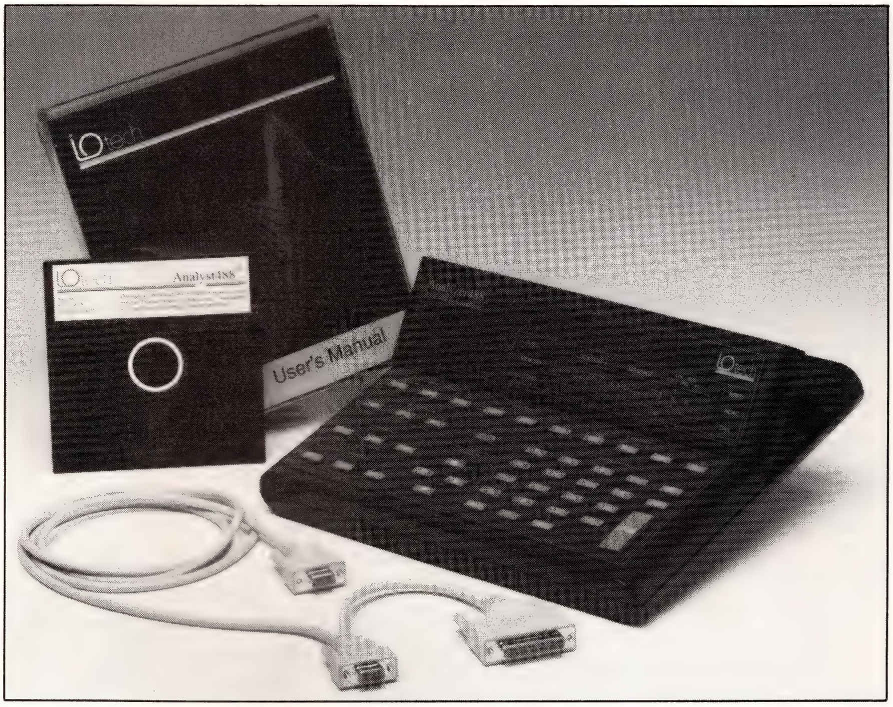
And you a comfortable one.

We run the tightest ship in the shipping business.

*See our current Next Day Air Service Explanation and Air Service Guide for complete guarantee details.

CIRCLE NO 92

IEEE-488 bus analyzer operates on its own or through a PC's serial port



You can analyze IEEE-488 bus transactions *by examining the Analyzer488's internal display or by connecting the unit to a PC and using one of three data-display modes. The instrument stores as many as 32,000 bus transactions.*

Although the IEEE-488 instrument bus has been in use for many years, there are few sophisticated development and debugging tools for this bus. The Analyzer488 troubleshooting tool transcends the usual lights-and-switches boxes that are today's common IEEE-488 troubleshooting tools. This stand-alone benchtop unit provides a small keypad and a 20-character alphanumeric display. Displaying bus operations in several formats, the unit includes a message mode that translates bus commands into mnemonic bus messages. The unit also allows you to monitor control signals.

If you have a PC at hand, you can use one of its RS-232C ports to control the Analyzer488. The manufacturer supplies Analyst488 software that lets you control the analyzer from the computer. Display windows and menus let you set up the analyzer and observe the data in three formats: message, hex, or mixed. The message mode displays individual bus messages in standard mnemonic form. If you need to examine individual bits and codes, the hex mode displays the bus transactions in hexadecimal columnar format. The mixed mode mixes data-transfer and bus commands on the screen, but it displays them in separate areas of the screen.

Whichever way you choose to control the unit, you can select from three modes of operation: a bus-analyzer/monitor mode; a bus-controller mode; or an instrument-simulator mode. When operated as a bus monitor or analyzer, the unit resides on the IEEE-488 bus in a nonintrusive mode. It samples as many as 32,000 transactions at a rate as high as 1M byte/sec. Unlike logic analyzers, the unit stores bus transactions, not logic states that are sampled at uniform intervals. Triggering sequences let you capture pretrigger and post-trigger transactions. You can also use a search and mark feature to scan through the collected information.

When operating as a bus controller, the Analyzer488 receives high-level commands through its RS-232C connection, then manipulates the IEEE-488 bus signals. In this mode, the unit can also monitor and record bus transactions. As an instrument simulator, the Analyzer488 supplies preset waveforms from an internal ROM. The waveforms provide a source of known data that you can use when testing IEEE-based instruments and software.

Whichever mode you choose, the instrument will provide a printed record of bus transactions through its RS-232C port or through an attached IEEE-488-compatible printer. The complete package of the analyzer, the software, the manual, and the interface cable costs $1495.—***Jon Titus***

IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX 216-439-4093. TWX 650-282-0864.

Circle No 730

IEEE 488

Interfaces & Software

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IEEE extenders, expanders & buffers.

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CIRCLE NO 94

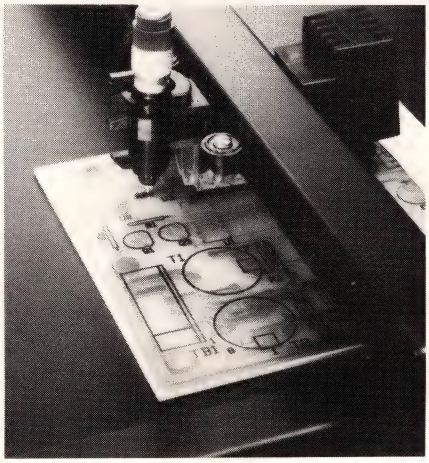
Prototyping system produces pc boards in one day

A complete pc-board design and fabrication system, the Plot-A-Board system lets you produce a prototype board from a CAE board layout in a matter of hours. Using the system, you can produce rigid or flexible printed circuits, and you can even produce multilayer boards. The system can produce pc boards with line widths and spacing as narrow as 0.010 in. You must have an IBM PC/AT or compatible computer with 640k bytes of RAM to use the system, and the vendor recommends a hard-disk drive.

To make a prototype board, a modified pen plotter deposits a resist pattern on a standard copper-clad pc-board substrate. The system then etches the board in the traditional manner. This scheme eliminates the photo-plotting, film-tool, and photo-resist steps that traditional pc-board manufacturing techniques require.

The complete Plot-A-Board system includes CAE software for pc-board layout and autorouting; a shear; an etcher; a drill press; a modified plotter; and consumables such as pc-board substrate, ink, and chemicals. The CAE software is Tango-PCB and Tango-Route from Accel Technologies (San Diego, CA). It accepts input from a companion Tango schematic-capture program or from a number of other popular schematic-capture programs.

A pattern-generation program takes the output file from the Tango software and drives the plotter. The system can handle patterns and, therefore, board sizes as large as 16 × 9.75 in. The plotter deposits resist with proprietary pens at 40 mm/sec; the system can draw a pattern on the prototype or on paper at 420 mm/sec. The system can handle boards as thick as 0.062 in.



A modified plotter applies resist *with proprietary pens and eliminates the traditional photography stages, thus letting you build pc-board prototypes in a few hours with the Plot-A-Board system.*

The spray-type etcher accepts 1- or 2-sided boards, includes a bath heater with temperature control, and uses sodium persulfate as an etchant. The 12-in. shear cuts laminate as thick as 0.093 in. and sheet metal as thick as 0.04 in. The drill press accepts bits ranging from 0.016 to 0.125 in. and includes a vacuum and a magnifier lens.

You can build a typical 4 × 4-in. prototype board with the Plot-A-Board system in a few hours for less than $25 in materials. A typical pc-board fabrication service would charge $500 or more to build such a prototype in a week. The vendor can fabricate your prototype boards with its system in a few days.

The complete prototyping system costs $9800; delivery is 30 days ARO. The system includes enough materials to make at least a dozen boards.—***Maury Wright***

HiTech Equipment Corp, 9400 Activity Rd, San Diego, CA 92126. Phone (619) 566-1892. FAX 619-530-1458.

Circle No 731

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We've got the experience. Our PS Series triple-output, 80W converter is serving in the newest attack helicopter.

Need a special converter or power hybrid? Call us and we'll work with your team to get the best solution for your needs.

DC/DC Converters

	Output Power	Output Voltage (V) Current (A)
AHE2805S	15	5V, 0 - 3A
AHE2812S	20	12V, 0 - 1.67A
AHE2812D	15	±12V, 0 - 625mA
AHE2815S	20	15V, 0 - 1.33A
AHE2815D	15	±15V, 0 - 500mA

-55°C to +85°C and -55°C to +125°C
Input voltage range is 17 - 40V

MIL-STD-1772
Qualified

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CIRCLE NO 93

Chip set provides 1000M-bps transfer with 40-bit parallel-system interface

***Serial-data rates as great as 1000M bps** are attainable with this transmitter/receiver pair. The GA9011 and GA9012 handle 40-bit parallel data at bus speeds to 25 MHz.*

If you need to quickly transfer large amounts of data from your processor to a distant location but are limited by transfer rate, your data-transportation problems may be over. Both the GA9011 and GA9012 are ends of a 1000M-bps serial-data link with parallel-system interface. You can use the pair to extend your processor bus at full speed.

Using an asynchronous handshaking protocol to control data transfer, the GA9011 transmitter accepts 40-bit-wide data. It encodes the data into a 50-bit serial word, using FDDI-standard 4B/5B encoding, then transmits the data. The GA9012 receiver accepts the serial data, recovers the clock, decodes the data, and presents your system with 40-bit parallel data and a data-valid signal. The parallel interfaces are TTL compatible; the serial signal is positive-referenced differential ECL.

The transmitter generates its serial clock by frequency multiplying a reference clock. This clock may come from your system, or you may use the device's built-in crystal oscillator. The reference clock can range from 20 to 25 MHz, and you can set the multiplication factor to be 5, 10, 20, or 40. You can, therefore, obtain a serial-data rate ranging from 100 to 1000M bps without designing high-frequency circuitry.

The receiver also requires a 20-to 25-MHz reference clock, but this must come from your system; the receiver has no built-in oscillator. The reference clock is the only external signal required, however. All other clock and data recovery circuits are built in and do not require external components. The receiver has limited error-detection capability and will assert an error signal if the word at its output contains an error.

The serial-data link is always running in order to maintain bit synchronization. If there is no user data available to the transmitter, it sends a frame-synchronization pattern. The receiver does not decode the frame synchronization, however; it only presents user data on its output lines. If the receiver loses synchronization, it generates a sync-loss signal.

You can connect the pair together with coaxial cable for distances <10m. If you are going farther, you will need to use fiber optics.

The serial-data link is unidirectional; you will need two links to create a bidirectional data path. If you need to handle more than 40 bits at a time, you can easily create parallel links. By cascading the system clock, you can synchronize the operation of parallel transmitters. The parallel receivers will automatically be synchronized.

The devices operate from a 5V supply and dissipate 2W each. They come in a 68-pin ceramic J-leaded chip carrier and sell for $370 (100).

Gazelle Microcircuits, 2300 Owen St, Santa Clara, CA 95054. Phone (408) 982-0900. FAX 408-982-0222.

Circle No 732

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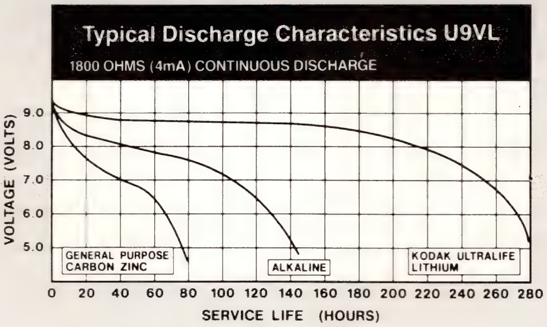

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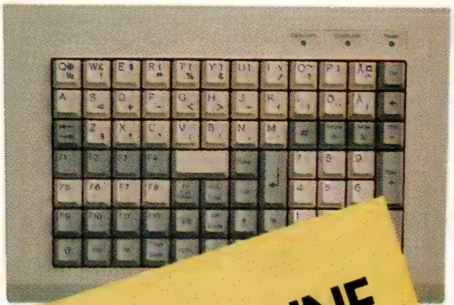

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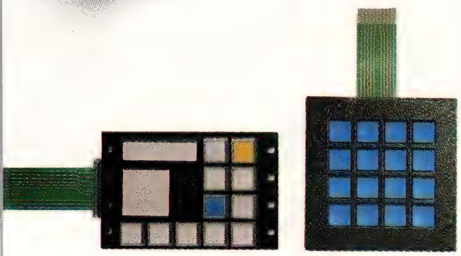

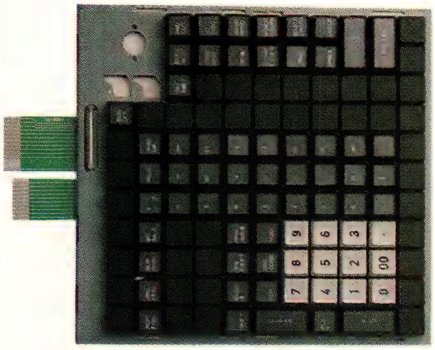

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POSITION YEARS THERE

ANNUAL SALARY $ OTHER INCOME $

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MOTHER'S MAIDEN NAME
(For use when you request special action on your account)

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My MasterCard®/VISA® Account # is

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Annual Fee(s) (Fee Waived first year)	$40 for Gold MasterCard or VISA Gold, $50 for Combination
Annual Percentage Rate	16.9%
Grace Period For Repayment Of Balances For Purchases	At least 25 Days from statement closing date
Method Of Computing The Balance For Purchases	Average Daily Balance (including new purchases)
Transaction Fee For Cash Advances, And Fees For Paying Late Or Exceeding The Credit Limit	Transaction Fee For Bank and ATM Cash Advances: 2% of each Cash Advance, $2 Minimum, $25 Maximum Transaction Fee For Access Check Cash Advances: 1% of each Cash Advance, $2 Minimum, $10 Maximum Late Payment Fee: $15; Over-the-Credit-Limit Fee: $15

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CIRCLE NO 98

TEXAS INSTRUMENTS REPORTS ON

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IN THE ERA OF MEGACHIP™ TECHNOLOGIES

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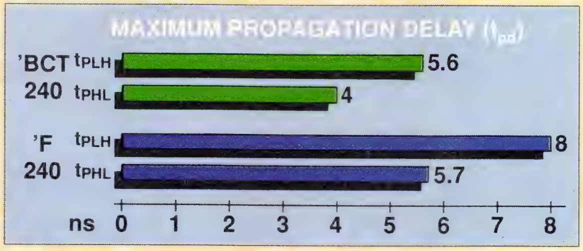
TI's BiCMOS logic gives you drive and speed up to par with advanced bipolar devices.

The chart says it all. Switching speeds of our BiCMOS family, designed specifically for bus interface implementations, are comparable to advanced bipolar counterparts. Drive currents meet the requirements of today's industry-standard buses: 48/64 mA commercial, 24/48 mA military.



TI's speed advantage: In a one-on-one comparison, a TI '74BCT240 BiCMOS octal bus driver proves to be much faster than a standard advanced bipolar equivalent.

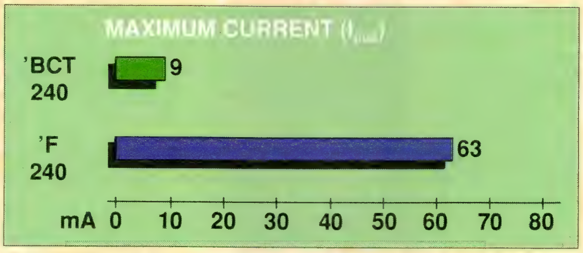
For example, our BCT2XXX memory drivers are two times faster than the competition's memory drivers. They not only solve the undershoot/overshoot problems associated with driving DRAM memories but also conserve real estate by incorporating a 25-ohm series damping resistor on chip.

With this speedy family comes a bonus, reduced switching noise. Case in point: An independent analysis* found our SN74BCT240 octal bus driver to have the fastest propagation delay (3.8-ns t_{PHL}) with the highest signal integrity (0.8-V simultaneous switching noise).

But there's another impressive side to the BiCMOS family story. Read on.

TI's BiCMOS logic cuts power consumption down to CMOS levels.

As you've gathered by now, our BiCMOS logic combines high-speed bipolar with low-power CMOS. Disabled currents can be reduced as much as 95% (*see chart*) while active currents are cut as much as 50% compared to advanced bipolar equivalents.



TI's power advantage: Here again, the BiCMOS driver wins over the advanced bipolar counterpart, exhibiting far less power dissipation.

As a matter of fact, total system power savings can be more than 25%.

Our BiCMOS family now numbers more than 40 members and will top 90. All members are compatible with advanced bipolar sockets, allowing easy plug-in upgrades.

BiCMOS technology is also enabling us to solve other problems that crop up in bus interface design. For example, the family will soon include a series of SCOPE™ Octals to provide system-embedded test capability. Also, the forthcoming BCT25XXX IWS line drivers will assure incident wave switching (IWS) down to 25 ohms.

For free samples of our BiCMOS logic family: **In Europe** call 44-234-223000, fax 44-234-223459, or write Customer Response Centre, MS 09, Texas Instruments Limited, Manton Lane, Bedford MK41 7PA, England. **In Asia** call 852-3-7351223, fax 852-3-7354954, or write Texas Instruments Hong Kong Limited, Market Communications Manager, 8/F World Shipping Centre, 7 Canton Road, Tsimshatsui, Hong Kong.

TEXAS INSTRUMENTS

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* David Shear, "EDN's advanced CMOS logic ground-bounce tests," *EDN*, Special Report, March 2, 1989.

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08-9238

Low-cost workstations

Even the world's fastest workstation will do you no good if it can't run the software you need. Before you select a workstation, make sure it can run your CAE software.

Margery Conner,
Regional Editor

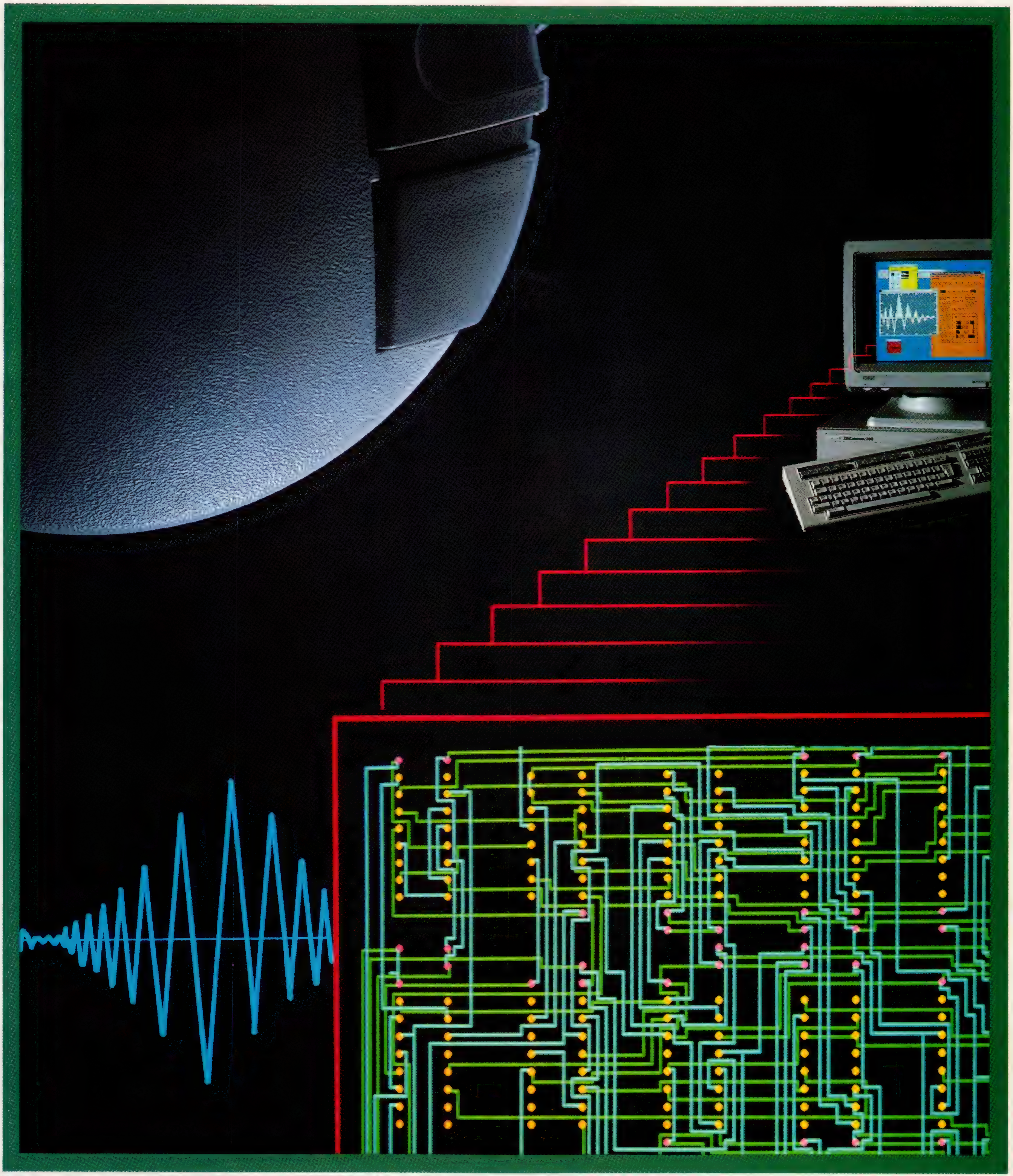
An abundance of Unix-based workstations costing from $4000 to $20,000 are now available, their vendors touting processor performance as if that were workstation users' only concern. Realistically, third-party software support *coupled* with execution speed, rather than CPU performance alone, determines workstation choice for most users.

Clearly, selecting a workstation is more complex than it was even two years ago, when Apollo (recently purchased by Hewlett-Packard) and Sun, with their 68020-based machines, were the unquestioned leaders in the field. Bob Weinberger, director of systems product marketing for HP's Apollo Systems Division, says that in the past, people bought a workstation first and then selected from the available software. Now, he says, "The software drives the sale." So before you become enraptured by the siren song of a high MIPS number, first select the software you'll be running, and then compare workstation-performance specs to select the workstation that makes your software run the fastest.

To get a feel for which workstations can run CAE software, EDN took an informal poll of representative CAE software vendors. The poll held no surprises. Sun and Apollo have the most support; Digital Equipment Corp (DEC) runs a close third. The rest of the workstations have only scattered support. Therefore, if you decide to purchase a workstation other than one offered by Sun, Apollo, or DEC, keep in mind that your and software choices will be limited.

Although two of the oldest and most popular CAE vendors, Mentor and Daisix, each port their software to only one manufacturer's work-

Of the current crop of workstations, the Apollo Series 2500, at a base price of $3990, is the least expensive. The 68030-based system performs at an unspectacular but respectable 4 MIPS, and you have access to a plethora of third-party software packages.



Unix-based workstations have broken the $20,000 price barrier. (Photo courtesy Digital Equipment Corp)

Select the software package you need before becoming enraptured by the siren song of a high MIPS number. Then pick the workstation to optimize the software.

station (Apollo and Sun, respectively), they are exceptions. (Daisix software also runs on its own proprietary hardware.) In general, most CAE vendors support many different workstations, with engineers' demands determining which workstation third-party software vendors port their packages to.

CISC versus RISC tradeoffs

Apollo, Sun, and DEC have all recently introduced workstations with base prices in the $4000 to $10,000 range. (For a complete list of workstations with a base price under $20,000, see **Table 1.**) Apollo's Series 2500 Personal Workstation uses Motorola's 68030 CISC (complex-instruction-set computer) chip. Sun's SPARCstation 1 and DEC's DECstation 2100 and 3100 use different RISC (reduced-instruction-set computer) processors.

In general, workstations based on one of the 680X0 family of CISC processors are less expensive than their RISC counterparts, and have a wide base of third-party software. Apollo's 2500 workstation, for example, has a base price of $3990, almost half the price of a RISC-based workstation. The system is fully compatible with Apollo's other 680X0-based sytems, the Series 3000 and 4000, so you have access to a large base of application software. The more expensive RISC-based workstations, on the other hand, have a smaller software base because their processors are newer. They do, however, run at least twice as fast as CISC-based workstations.

One reason Apollo can price the 2500 so low is that it is highly integrated and requires fewer, less-expensive components than do RISC-based systems, which require more expansive and faster memory to support their fast processor. RISC-based systems in general require at least 8M bytes of RAM; you can build a 68000-based system with only 4M bytes.

Another reason for the 2500's affordability is that its mother board has no expansion slots—any add-ons must go through the SCSI interface. Apollo's 2500 actu-

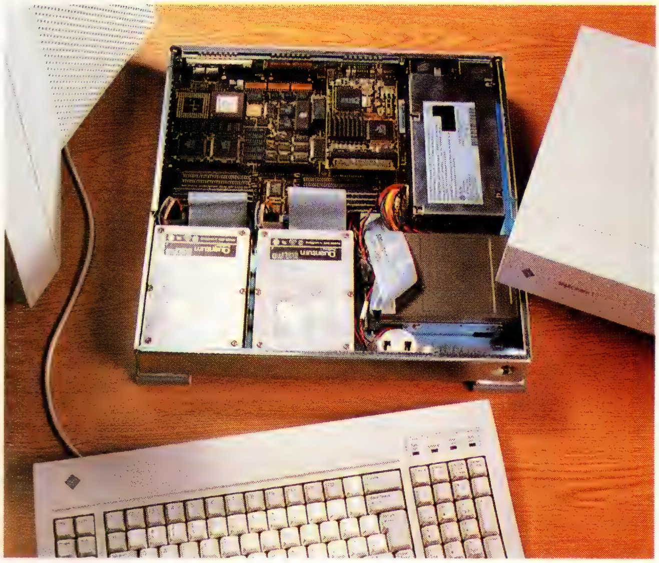
Table 1—Unix-based workstations with base price less than $20,000

Company	Product	Base price	CPU	System speed (MIPS)	Clock frequency (MHz)	Memory (min-max) (M bytes)
Data General Corp	AViiON	$7450	88000	17	16.67 or 20	4 to 28
Digital Equipment Corp	DECstation 2100	$7950	R2000	10	12.5	8 to 24
	DECstation 3100	$11,900	R2000	14	16.67	8 to 24
Hewlett-Packard Corp	Model 340/360/370	$8500	68030	4/5/8	16.7/25/33	4 to 16
	Model 834CH	$19,375	HP-PA (HP proprietary RISC)	14.8	15	8 to 48
Hewlett-Packard, Apollo Systems Div	Series 2500 Personal Workstation	$3990	68030	4	25	4 to 16
	Series 3500 Personal Workstation	$8495	68030	5	25	4 to 32
	Series 4500 Personal Super Workstation	$19,990	68030	8	33	8 to 32
Intergraph Corp	Interpro 125	$16,000	Clipper	4	25	6 to 12
MIPS Computer	RS2030	$17,000	R2000	12	16.67	8 to 16
Opus	Personal Mainframe/8000	$9995	88000	17	20	4 to 20
Silicon Graphics Corp	Personal iris	$13,500	R3000	16	20	8
Solbourne Computer	Series 4/500	$17,100	Sparc	9.5 to 17	16.67	16 to 96
Sony Microsystems	News 1700 series	$11,495	68030	4.3	25	4 to 32
Sun Microsystems	SPARCstation 1	$8995	Sparc	12.5	20	4 to 16
	Sun 3/80	$5995	68030	3	20	4 to 16
	Sun 386i/150 and 250	$8990	80386	3/5	20/25	4 to 16
Tektronix	XD 88/10	$16,000	88000	17	20	8 to 32

ally does have one card slot—but it's virtually invisible to the user. Apollo uses the slot to configure the system for a native Ethernet, IBM Token Ring, or Apollo Token Ring network interface. The 2500 comes standard with a 15-in., 1224 × 800-pixel black-and-white display. No color display is available. It also comes with 4M bytes of RAM, which you can expand in increments of 4M bytes (at $650/M byte), to a maximum of 16M bytes. A 68882 FPU (floating-point unit) is standard.

Keep in mind that you've got to balance an initial wide software base and a low cost against system performance. The 2500 clocks in at a respectable, though unremarkable, 4 MIPS. Both DEC and Sun, with their new RISC-based systems, have gambled that users will pay a premium for higher system speed, and that customer demand will force third-party CAE vendors to port their 680X0-based software to the new RISC-based systems.

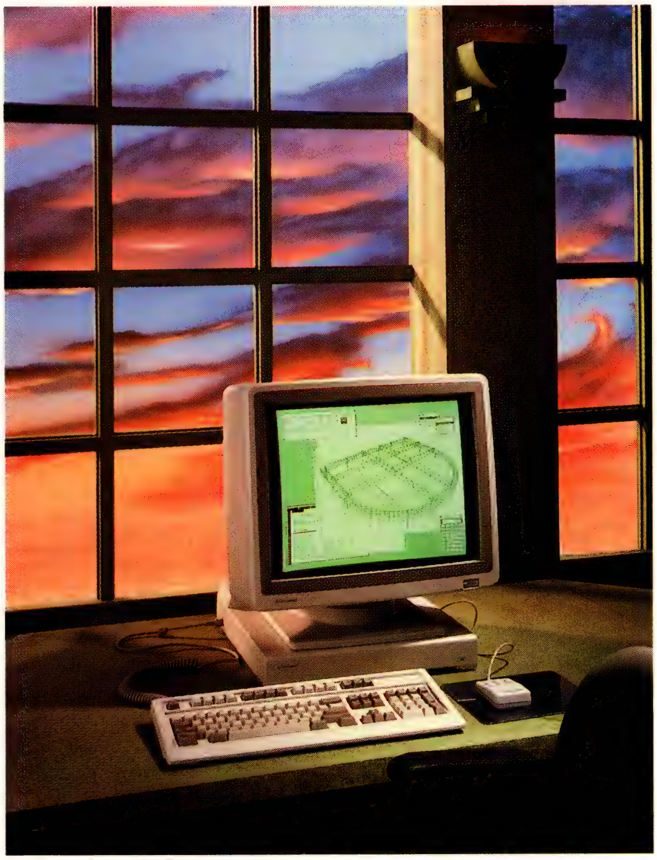
The DECstation 2100 ($7950) and 3100 ($11,900) clock in at 10 and 14 MIPS, respectively. Tom Furlong,



Capable of almost 15 MIPS and 2M flops, the HP 834CH is based on Hewlett-Packard's proprietary RISC architecture.

Graphics-display resolution (pixels)		Floating-point unit	Hard-disk size (M bytes)	Comments
Monochrome	Color			
1280×1024	1280×1024×256	Internal	160 or 320	
1024×864	1024×864×256	R2010	As many as two 105M-byte disks	
1024×864	1024×864×256	R2010	As many as two 105M-byte disks	
1024×768	1024×768×16 1280×1024×256	68882	81 to 571	
1280×1024	1280×1024×256	Proprietary	156 to 300	
1024×800 1280×1024	—	68882	100 or 200	
1024×800 1280×1024	1024×800 or 1280×1024; 16 or 256 colors	68882	155 to 697	Graphics accelerator available for 3500 and 4500
1024×800 1280×1024	1024×800 or 1280×1024; 16 or 256 colors	68882	155 to 697	
—	1184×884×32	Internal	156	
1280×1024	—	R2010	172	
640×480 1664×1200	800×600×256 1280×1024×256	Internal	40	
—	1024×768×256 1280×1024×256	R3010	150 to 344	
1152×900	1152×900×256	Weitek 1164165	2.6G bytes (max)	
816×1024	1280×1024×16 or 256	68882	286	
1152×900	See comments	Weitek 1164165	104M bytes to 1.1G byte	GX version has accelerated color graphics: 1.52×900×256 for $19,995
1152×900	1152×900×256	68882	104M bytes to 1.1G byte	GX version w/accelerated graphics costs $13,995
1024×768	1024×768×256	80387	91 to 327	
—	1280×1024×256	Internal	156M bytes to 3G byte	

DEC's design philosophy was simple—find a processor that runs like a deer and use it as the system's central processor.



Based on Motorola's 88000 RISC processor, the AViiON workstation has a system speed of 17 MIPS, claims manufacturer Data General.

architect of the 2100, points out that the workstation has a simple architecture—it relies on MIPS Computer Systems' R2000 RISC processor to perform all the processing tasks within the system. DEC's design philosophy was to find a processor that runs like a deer and use it as the system's central processor, thereby eliminating the need to balance various distributed processors. This approach contrasts with other workstations, such as the Opus Personal Mainframe/8000, which use distributed processers to handle I/O and graphics duties. (For a more detailed comparison of workstations that use either centralized-processor architecture or distributed-processor architecture, see **box**, "Workstation architectures vie for speed.")

To remain compatible with DEC's VAX minicomputer line, both the 2100 and the 3100 use little-endian data storage. (Little endian means that bit 0 in a byte is the least significant; big endian means that bit 0 is the most significant.) The R2000 RISC-processor architecture allows for either big- or little-endian storage, and indeed, MIPS Computers' own M/120-5 uses the big-endian technique. In addition, the R2000's optimizing compilers can handle either technique. Although the DEC workstations are not compatible with other R2000-based systems at the binary-code level, they are compatible at the source-code level, according to Armando Stettner, principal engineer for DEC's Workstation Systems Engineering.

Stettner notes that because Intel uses the little-endian scheme in its 80X86 processor architecture, the data-storage format of the DECstations is the same as that for PCs. And, since PCs are nipping at the heels of low-end workstations, this similarity could be advantageous in sharing common data bases.

The 12.5-MHz DECstation 2100 has a MIPS number similar to the Sun's 20-MHz SPARCstation 1. Furlong claims that the 2100's R2000 processor can boast a high MIPS number at a lower clock speed than the SPARCstation because the R2000's designers made better selections of the instructions included in the processor's instruction set. Because the 2100 runs at 12.5 MHz, it uses less-expensive parts than a 20-MHz-clock workstation. To further keep a lid on system costs, the 2100, like Apollo's 2500, has a mother board with no expansion bus.

The SPARCstation 1 ($8995), Sun's entry-level machine, is one RISC-based system that does have much software available. Though its instruction set is incompatible with the company's older, 680X0-based workstations, third-party CAE vendors have already ported a wide base of software to SPARC-based systems. This software-vendor support stems, at least partially, from the relative ease with which they can port from the older 680X0-based Sun systems to the SPARCstation. Tom Reeder, vice president of marketing at Eesof, notes that although the SPARCstation has a different processor from the older Sun 4 workstation, the basic system architecture is quite similiar. As a result, porting Eesof's software from the Sun 4 to the SPARCstation took a matter of hours, rather than a major engineering effort.

Unlike Apollo and DEC, which chose to save system costs by allowing no expansion slots on the mother board, Sun's SPARCstation uses the company's proprietary SBus. You can add external hardware, such as a data-acquisition board, through the bus.

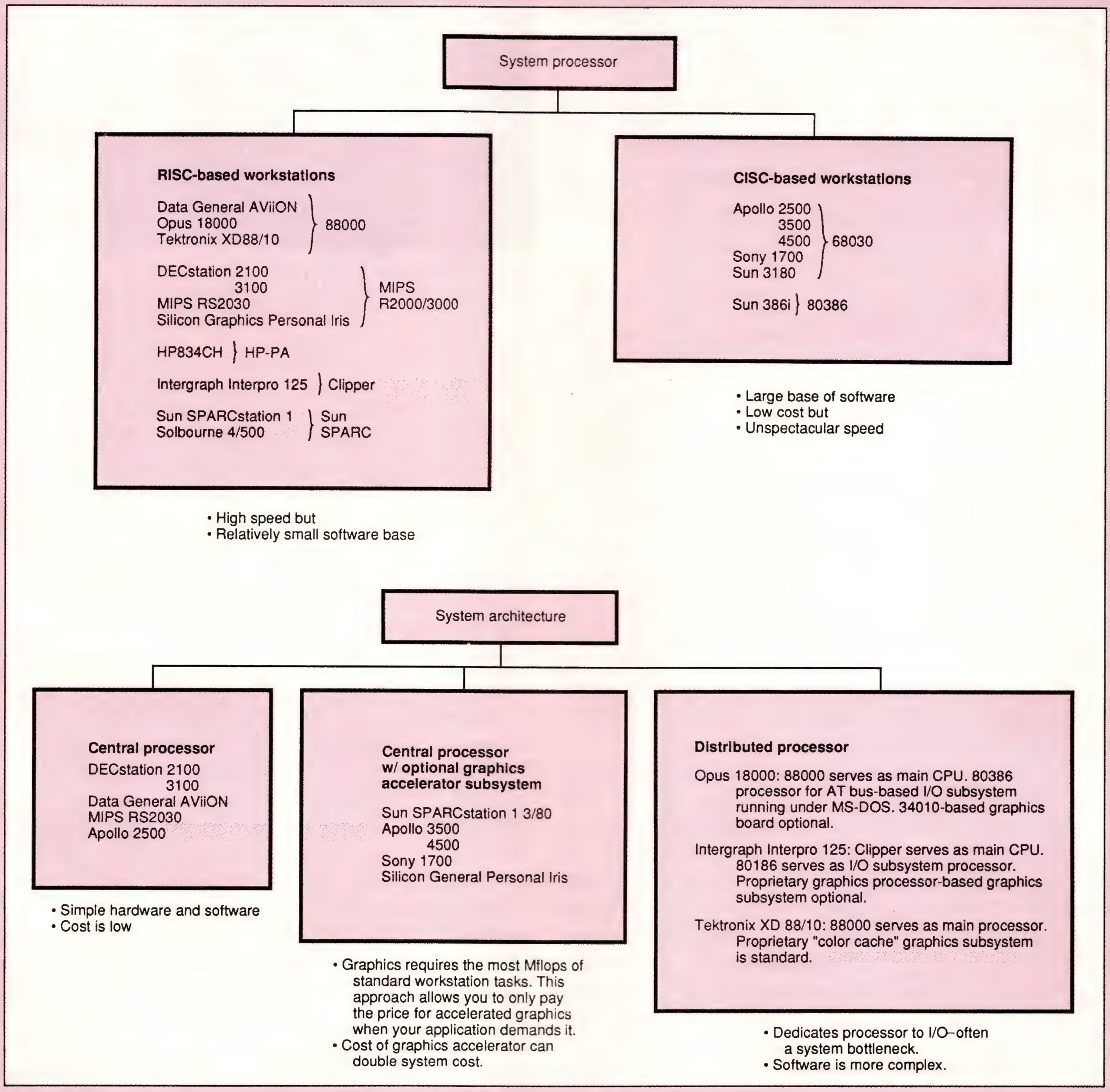
Like any workstation manufacturer, Sun would naturally like to see its system processor and architecture

Workstation architectures vie for speed

System design plays nearly as controversial a part in determining workstation speed as whether the system uses a CISC or RISC processor: Witness the diversity in approaches that workstation manufacturers use. There are two extremes in workstation system design—central processing, where one processor is responsible for virtually all processing, and distributed processing with a separate main processor and I/O processor. Somewhere in the middle of these two approaches are systems that accelerate only the graphics portion of the workstation with an intelligent graphics-display controller.

The DECstation 2100 and 3100 typify the central-processor approach. They use a very fast RISC processor to control all system operations and calculations. This approach simplifies the system software because the software never has to handshake or consider what some other subsystem is doing. On the other hand, the central-processor approach requires that the processor's bandwidth be fast enough to perform all system processing. If it isn't, the workstation is only as fast as its slowest task.

The Opus Personal Mainframe/8000 is an example of distributed-processing architecture. The system comprises an 80386-based PC/AT with an 88000 add-in board. The 80386 handles all system I/O while the 88000 handles all application software processing.



- High speed but
- Relatively small software base

- Large base of software
- Low cost but
- Unspectacular speed

- Simple hardware and software
- Cost is low

- Graphics requires the most Mflops of standard workstation tasks. This approach allows you to only pay the price for accelerated graphics when your application demands it.
- Cost of graphics accelerator can double system cost.

Opus 18000: 88000 serves as main CPU. 80386 processor for AT bus-based I/O subsystem running under MS-DOS. 34010-based graphics board optional.

Intergraph Interpro 125: Clipper serves as main CPU. 80186 serves as I/O subsystem processor. Proprietary graphics processor-based graphics subsystem optional.

Tektronix XD 88/10: 88000 serves as main processor. Proprietary "color cache" graphics subsystem is standard.

- Dedicates processor to I/O–often a system bottleneck.
- Software is more complex.

In general, workstations based on one of the 680X0 family of CISC processors have a wide base of third-party software and are low priced.

Featuring built-in audio capability, MS-DOS compatibility, and an expansion bus, Sun's SPARCstation 1 has a base price of $8995. The $19,995 GX version delivers graphics speeds of 400,000 2-D and 175,000 3-D vectors/sec.

With a total footprint of just 16 × 16 in., the SPARCstation 1's mother board is about the same size as an 8.5 × 11-in. sheet of paper.

become an industry standard, meaning that many independent vendors would offer their own software-compatible versions of Sun's hardware. Standardization also benefits users because add-on hardware, as well as application software, becomes inexpensive. Witness the IBM PC: A major reason PC software is so inexpensive is that hardware and software designers have only one basic processor and architecture to support.

Solbourne Computers' products are all SPARC based and Sun-software compatible—Solbourne licenses Sun's version of the Unix operating system, SunOS. Solbourne currently offers its Series 4/500, which is compatible with Sun's Series 4 machine, but it plans to introduce a low-cost SPARC-based machine at the end of this year. Toshiba (Tustin, CA) and Tatung (Carson, CA) are also planning to introduce SPARC-based systems in the near future.

Although Sun gives much of its promotional effort to the new SPARCstation, the company has not yet abandoned the 680X0 CPU as a workstation processor. Sun's lowest priced workstation, the 3/80 ($5995), is also 68030-based. In keeping with its low price tag, the machine comes in a color version with a relatively low-resolution screen of 1152 × 900 pixels, which may not be high enough for your application. If your system is running IC-layout software and displaying with many layers of interconnects, for example, the 3/80's standard display's low resolution may drive you crazy. But, if you're using the system to run CASE (computer-aided software engineering) programs, the display's resolution will probably be fine.

Again, a wide base of third-party software is key to a workstation's success. Vendors of 88000-based workstations such as Tektronix, Data General, and Opus hope that the efforts of an industry-sponsored consortium, 88open, will result in the ready availability of a large body of 88000-compatible software. The consortium exists to promote standards and certification procedures that will create an open and interoperable system environment for 88000-based systems. The 88open Binary Compatibility Standard (BCS) subcommittee has developed a definition of a standard form for all executable programs on all 88000-based systems. The standard covers data, program, and file representations. It defines common data types, such as integer, floating-point, and character. It specifies how data are aligned on word and page boundaries in memory, and defines how an executable data file is structured on disk.

Third-party software developed for any workstation in the consortium can automatically run on any other machine that conforms to the standard, thereby generating a software base more rapidly. Although Motorola claims a MIPS number of 17 for the 88000—the highest speed claimed by any RISC processor, and the chip has earned praise from engineers evaluating it, the future for 88000-based electronic CAE workstations is bleak because so few CAE software vendors support

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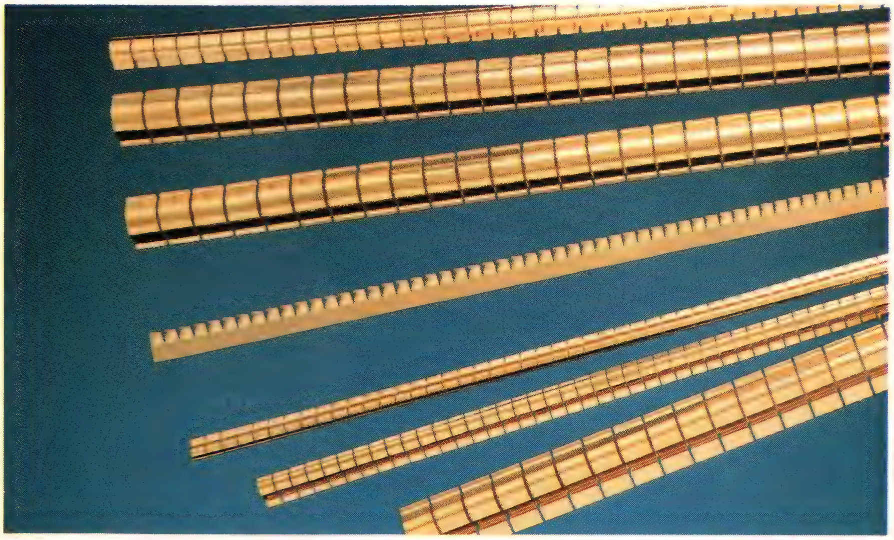

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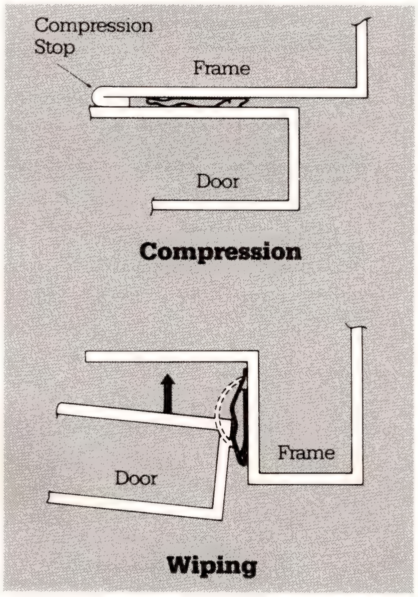

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RISC-based workstations have a smaller software base and are more expensive than CISC-based workstations, but run at least twice as fast.

or plan to support it. None of the CAE software vendors we contacted plan to port their software to 88000 machines, stating that they have seen no demand for the porting by their customers.

However, binary compatibility is no remedy. It places some constraints on the hardware because the software must make some basic assumptions about the system it's running on. For example, one system might have a help key, and another might not.

As well as knowing what software supports which platform, you'll need to know what kind of software you'll be running. If you're running a digital simulator, the workstation needs very fast integer performance. Plus, you'll want to have enough RAM for the simulator's IC-model matrices to fit entirely into RAM. Otherwise, every time the workstation must access the disk to bring in more matrix data, you incur a time penalty. If you're running analog simulation, you'll require fast floating-point capability as well as fast integer performance. On the other hand, if you're running data-base software, which usually requires plenty of memory accesses, a high MIPS number won't be as important as a fast disk-access speed.

The workstation market's preoccupation with system speed begs the question: How do you measure it? For example, Motorola's RISC chip, the 88000, has a MIPS number of 17, the number that Tektronix, Opus, and Data General quote for their 88000-based workstations, and the highest claim of any workstation manufacturer. Yet the 88000 has a relatively poor floating-point performance of 12.3M Whetstones. MIPS Computers, for example, claims a 13.6M Whetstone number for the floating-point unit for the R3000 running at 25 MHz. (The R3000 is a higher-frequency version of the R2000 and is used, for example, in Silicon Graphics' Personal Iris workstation. The Whetstone number for the R2000 is the R3000's Whetstone number derated to 16.6 MHz.)

For an indication of floating-point performance, you'll need to ask the manufacturer for the Whetstone

Manufacturers of low-cost workstations

For more information on workstations costing $20,000 or less, such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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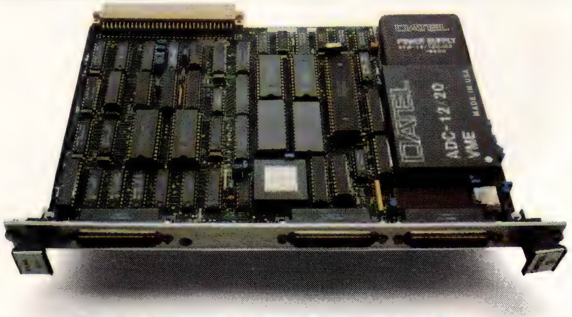

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or Linpack figure. The Linpack figure can be misleading, however, unless you keep in mind that all the numbers used in the Linpack algorithm can fit into a RISC processor's cache memory. It doesn't give an accurate indication of how fast the processor will perform a floating-point calculation that must access the main memory.

Another application that requires lots of number-crunching is graphics. You may associate complex graphics displays with pictorial analysis of scientific research, but sheer graphics-display speed is also important when you're playing "what-if" games for such CAE applications as pc-board and IC layout. Also, the ability to quickly display a new layout is a plus. In a CAE application, the scene being displayed is not complex, but you want to see and be able to change it very fast.

Sun, Apollo, and HP all offer graphical accelerator add-ons, which can double the price of the workstation. Tektronix's XD 88/10 has a color-cache controller and a proprietary processor dedicated to the graphics display, in addition to its main 88000 processor. The complete graphics workstation costs $15,000.

The Holy Grail that is system speed is an elusive goal. What's considered a high MIPS number today will be merely mediocre tomorrow. For example, soon you'll probably be able to upgrade a SPARC-based system with a bipolar SPARC chip and see the MIPS speed increase by 50%. And, plugging in the next generation of the 88000 RISC will likely accelerate its double-precision floating speed as well. So, making sure you have a system that will run the software you need for the foreseeable future is your insurance against obsolescence. **EDN**

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1. Wright, Maury, "Graphics environments,"*EDN*, October 26, 1989, pg 152.
2. Small, Charles H, "RISCs force move to compilers," *EDN*, January 5, 1989, pg 73.
3. Shear, David, "Workstations," *EDN*, October 29, 1987, pg 168.

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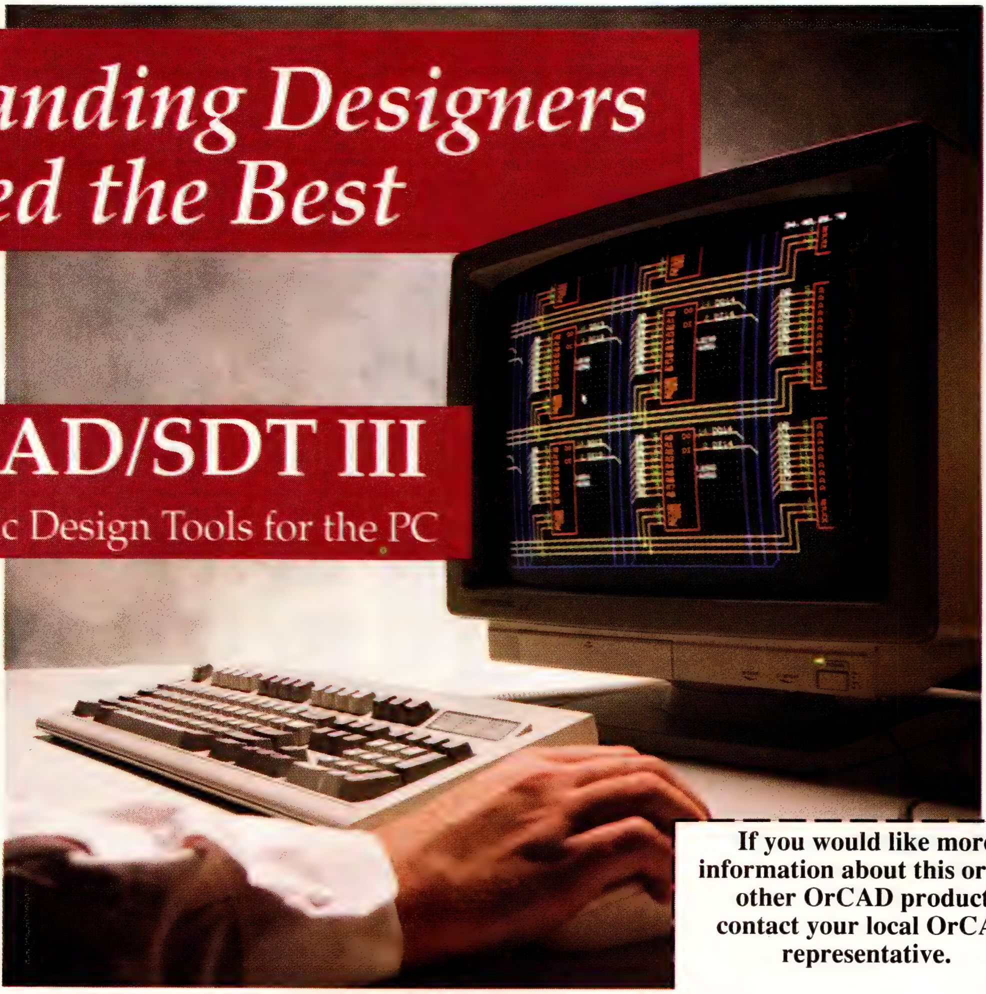

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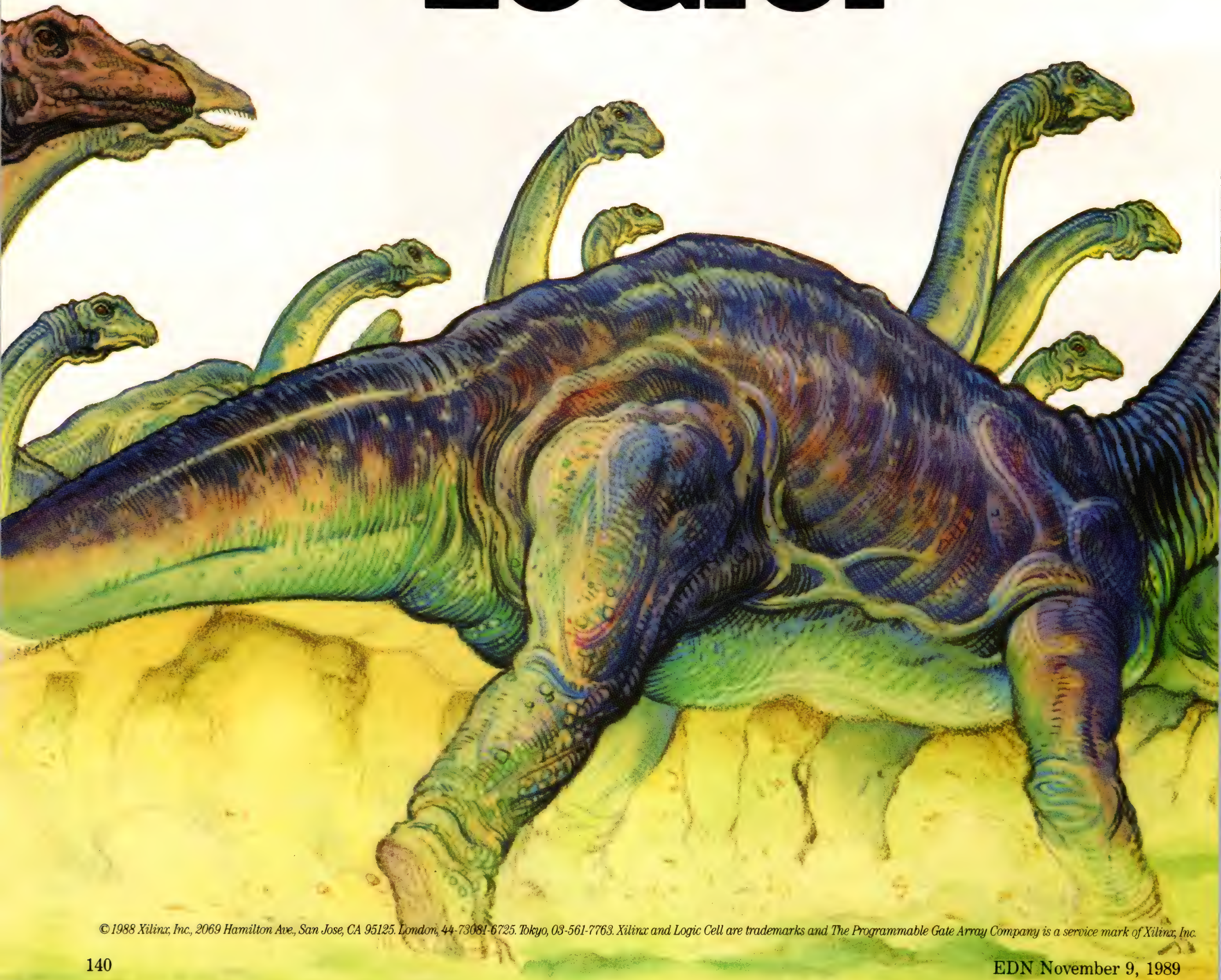

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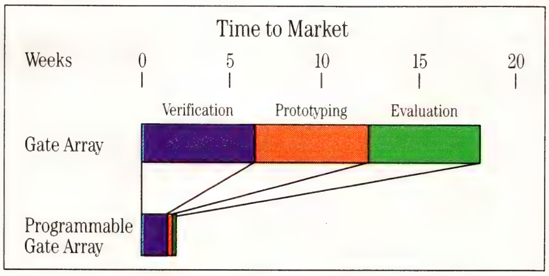

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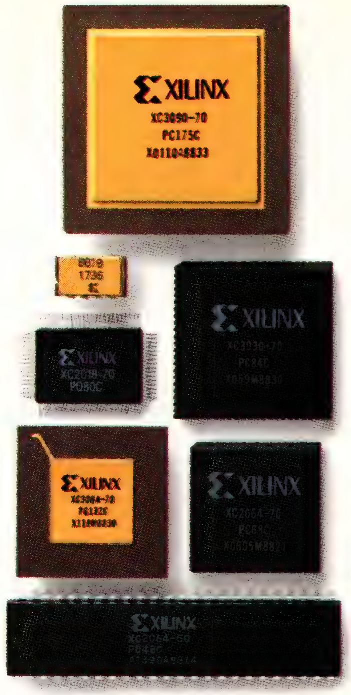

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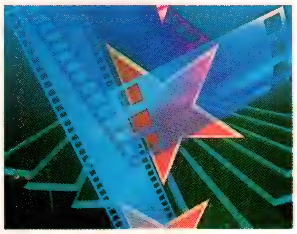
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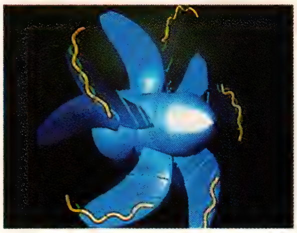
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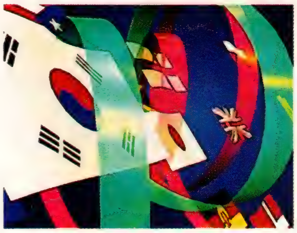
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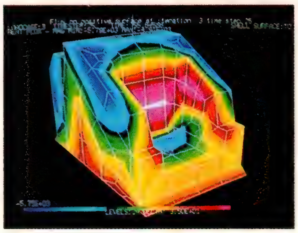
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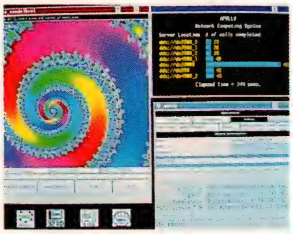
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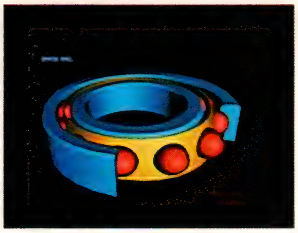
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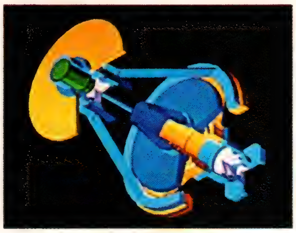
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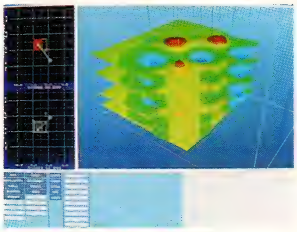
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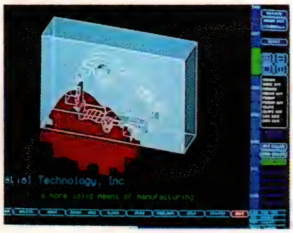

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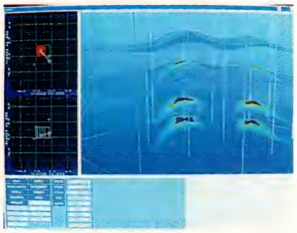
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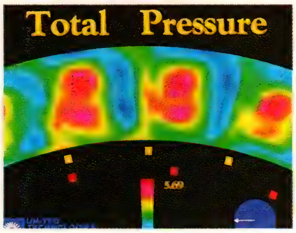

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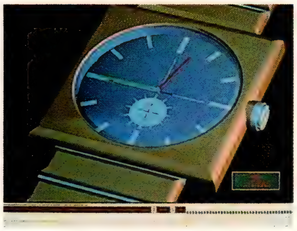
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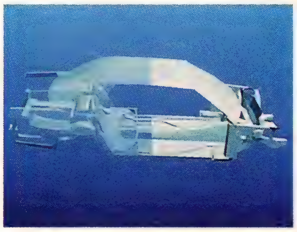
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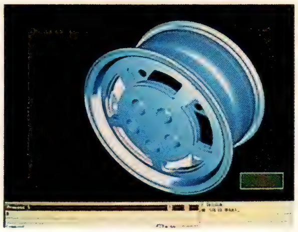
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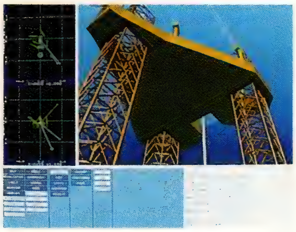
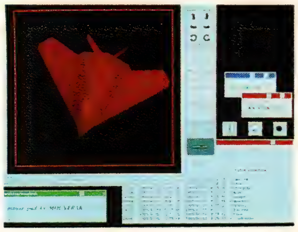
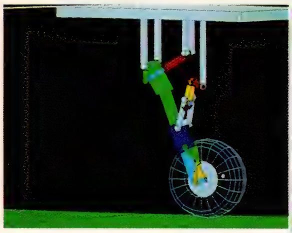

Scientific visualization


Aerospace engineering


Kinematics and dynamics

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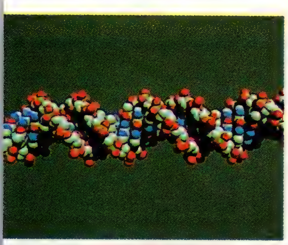
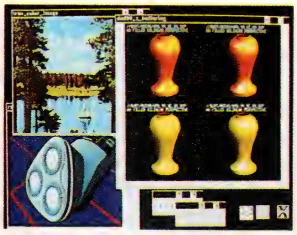
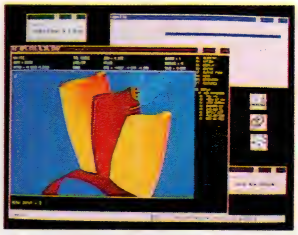
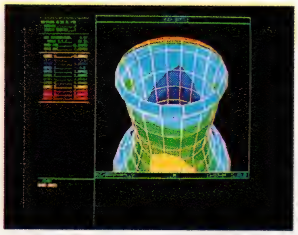
available for any network.

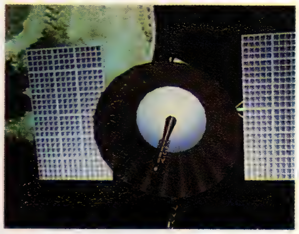

Computer-aided molecular design

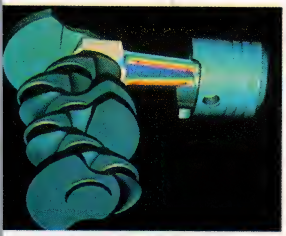

Multi-window industrial design


Computer-aided engineering and design

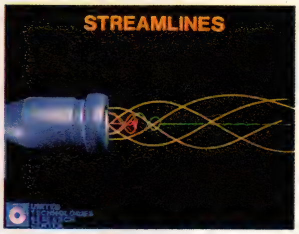
Industrial design


Structural analysis using finite element analysis

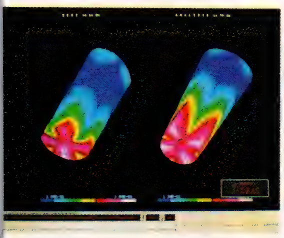

Aerospace engineering

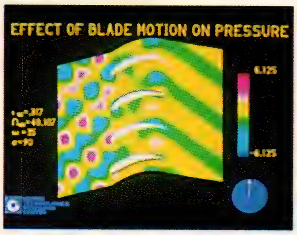

Computer-aided engineering

Automotive engineering



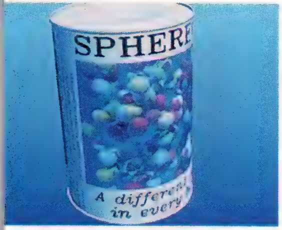
Computational fluid dynamics


Thermal analysis



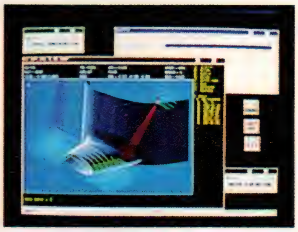
Computational fluid dynamics

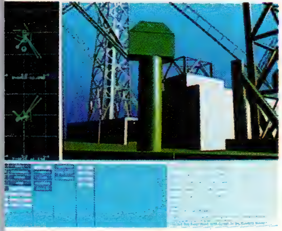
Industrial design

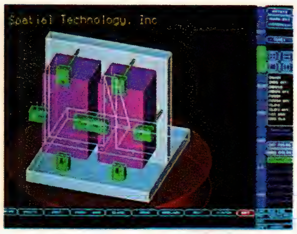


Industrial design

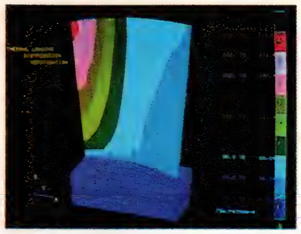
Computer-aided engineering


Computer-aided engineering


Scientific visualization



Computer-aided design


Finite element analysis

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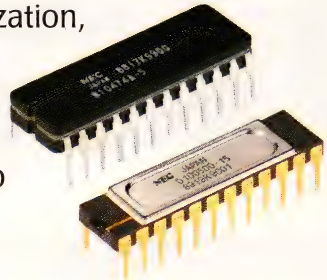

Device	Interface	Organization	Access time (ns)	Power consumption (W)	Supply voltage (V)	Package
μPB10422D-7/-10	ECL 10K	256 x 4	7/10	1.2	−5.2±5%	24-pin ceramic DIP
B10470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B10474AD-5/-6		1K x 4	5/6			24-pin ceramic DIP
B10474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B10480D-10/-15		16K x 1	10/15			20-pin ceramic DIP
B10480B-10/-15						20-pin ceramic flat
B10484D-10/-15		4K x 4	10/15			28-pin ceramic DIP
B10484B-10/-15						28-pin ceramic flat
D10500D-15/-18		256K x 1	15/18			24-pin ceramic DIP
B100422D-7/-10	ECL 100K	256 x 4	7/10	1.0	−4.5±5%	24-pin ceramic DIP
B100422B-7/-10						24-pin ceramic flat
B100470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B100474AD-5/-6		1K x 4	5/6			24-pin ceramic DIP
B100474AB-5/-6						24-pin ceramic flat
B100474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B100474B-8/-10/-15						24-pin ceramic flat
B100474B-45/-50/-60			4.5/5.0/6.0	2.0		
B100474K-45/-50/-60						24-pin LCC
B100480D-10/-15		16K x 1	10/15	1.0		28-pin ceramic DIP
B100480B-10/-15						28-pin ceramic flat
B100484D-10/-15		4K x 4	10/15			28-pin ceramic DIP
B100484B-10/-15						28-pin ceramic flat
B100484K-10/-15						28-pin LCC
D100500D-15/-18		256K x 1	15/18			24-pin ceramic DIP

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Hong Kong Tel:3-755-9008. Telex:54561.
Taiwan Tel:02-719-2377. Telex:22372.

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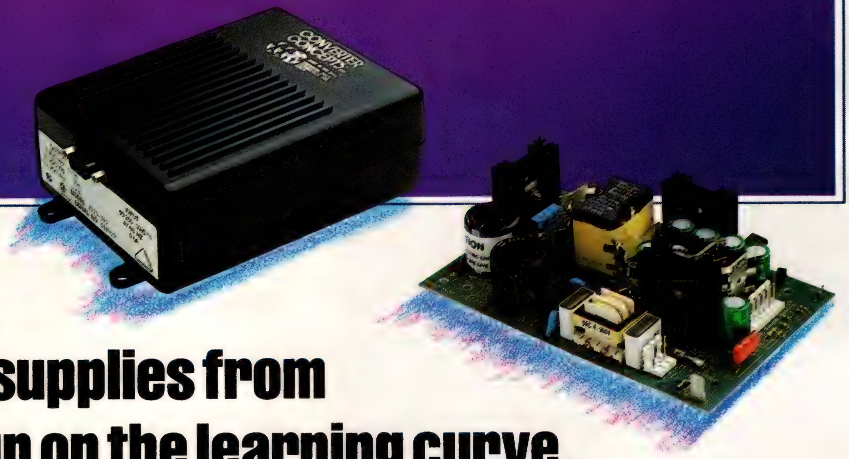
NEC

CIRCLE NO 107

UNIVERSAL INPUT LEARNING CURVE

Thank God. Success. Success. Success. Success. Success. Success.
At last.
How about?
Please.
Maybe.
Almost.
Phooey.
Could be.
Think.
Drat.
Again.
Oh, no.
Adapt.
Rats.
Refine.
Oops.
Nuts.
Test.
Invent.
Approve.
Fund.
Propose.
Assess.
Idea.
Need.



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50 Watts in a 40 Watt Footprint... Off-the-Shelf—Even though the Converter Concepts VL 50 is a 50 watt internal power supply, it fits into the standard 40 watt footprint. Yet, it still offers industry standard I/O configurations.

It's also available for immediate delivery. No waiting.

The VL 50 is UL, CSA and VDE safety approved. It accepts AC inputs of 85-265 VAC, incorporates surface mount technology, provides standard overvoltage protection and includes overcurrent protection, too. At a cost that's competitive with that of any manufacturer, foreign or domestic.

All in all, the VL 50 is quite a package... from way up on the learning curve.

25 Watts for External Use...with Immediate Delivery—Converter Concepts also offers off-the-shelf delivery of our XT 25. It's a little different because it's for external use.

But it's also a lot the same.

It's based on the same proven technology. It's UL, CSA and VDE safety approved. It accepts inputs from any AC power source of 85-265 VAC. It's made in the United States. It's cost competitive. And it comes from way up on the learning curve.

Learn More About What We Offer and What We Know—For more information about off-the-shelf delivery of the Converter Concepts' VL 50 internal power supply, our XT 25 external power supply and our other products and services phone, toll free, 1-800-253-5227. (In Wisconsin, 608-429-2144.) Or write us for more information. We'll be happy to help you learn what we've learned in more than 10 years.

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CIRCLE NO 108

Wescon/89

To satisfy the information needs of today's designers, Wescon/89 features a diverse program of courses and sessions on timely electronics issues.

Tom Ormond, *Senior Editor*

More than 45,000 electronics engineers are expected to attend the 39th annual Wescon, which runs from Tuesday, November 14 through Thursday, November 16 at three San Francisco locations: the Moscone Convention Center, the Brooks Hall/Civic Auditorium complex, and the Meridien Hotel. The show will feature thousands of live product demonstrations from more than 1000 vendors of EDA (electronic design automation) tools; instruments for test, measurement, and inspection; active and passive components; and production equipment, materials, and services.

The 33 technical sessions in the Professional Program have been divided into 12 tracks, spread out over the three days of the show. Wescon/89 will also offer a wide selection of short courses on issues of current interest to the varied audience of circuit and packaging designers, research and development engineers, and test engineers.

A forum of special sessions will explore five of the hottest topics in the electronics industry—HDTV (high definition TV), VHDL (VHSIC hardware-description language), video-systems technology, neural networks, and 32-bit embedded controllers. Many observers feel that the development and use of HDTV technology will have a significant impact on the electronics industry. Each day at Wescon/89, a 2-hour session will explore HDTV systems currently proposed for the FCC standards.

The special session on VHDL—a hardware-description language currently being adopted as a standard by vendors and users for CAD, CAE, and CAT (computer-aided test)—will provide a state-of-the-art report on developments in VHDL design, synthesis, modeling, and testing by experts in each of these areas. In another session, Motorola and Intel will present their ideas on high-level, high-performance embedded-systems designs. The program will present a discussion of evolutionary technology and actual applications from well-known manufacturers. The session on video-systems technology will explore emerging video-systems standards and report on significant developments affecting video systems in imaging, entertainment, and communications.

Two sessions will examine neural-network technology. The session on neural networks in the real world will explore methods of making neural-network technology commercially viable. This discussion will also consider deployment issues and the status of European research and applications. The second session will report on some of the latest neural-network technologies and applications.

The program of 19 short courses spread over the three days of the show will address a variety of topics. "Modern Microwave Semiconductor Devices" will explore microwave transistors, MMICs (monolithic microwave ICs), and present limitations and future trends in microwave technology. This course will complement several presentations in the sessions program.

Many courses will explore specific design issues.

WESCON/89 TECHNICAL SESSIONS

		MOSCONE CENTER			CIVIC AUDITORIUM	MERIDIEN HOTEL
TUESDAY, NOVEMBER 14	8:30 AM–10:30 AM	**SESSION 1** A NEW GENERATION OF ECL CIRCUITS SHATTER SYSTEM PERFORMANCE BOTTLENECKS	**SESSION 2** INTELLIGENT MEMORIES PROMISE PRODUCT AND MARKET NICHES	**SESSION 3** ARCHITECTURAL IMPLICATIONS OF ASIC TECHNOLOGIES	**SESSION 4** CAD FOR MICROWAVE CIRCUITS	
	12:30 PM–2:30 PM	**SESSION 5** ADVANCED LOGIC — MEETING SYSTEM DESIGNER NEEDS	**SESSION 6** SPECIALTY MEMORIES: COST EFFECTIVE SOLUTIONS TO HIGH PERFORMANCE SYSTEMS	**SESSION 7** DESIGN METHODOLOGIES FOR BRIDGING THE 1–100K GATE ASIC SPECTRUM	**SESSION 8** ACTIVE MICROWAVE DEVICES	
	4:00 PM–6:00 PM	**SESSION 9** SILICON INTEGRATED CIRCUIT SENSORS AND MICRO-STRUCTURES	**SESSION 10** CONTENT ADDRESSABLE MEMORY (CAM) APPLICATIONS FROM PATTERN RECOGNITION TO LAN BRIDGING	**SESSION 11** RISC — THE NEXT GENERATION	**SESSION 12** COMMERCIAL APPLICATION OF GaAs IC AND SILKICON MMICs	
WEDNESDAY, NOVEMBER 15	8:30 AM–10:30 AM	**SESSION 13** JTAG/IEEE SERIAL PROTOCOLS REDUCE THE DESIGN CYCLE AND IMPROVE TESTABILITY, MANUFACTURING AND FLEXIBILITY	**SESSION 14** **SPECIAL SESSION** VHDL — A STANDARD HARDWARE DESCRIPTION LANGUAGE FOR CAD/CAE/CAT	**SESSION 15** THE INCREASING SOPHISTICATION OF ELECTROMAGNETIC COMPATABILITY (EMC)	**SESSION 16** ADVANCES IN SIGNAL PROCESSING	**SESSION 17** USING COMPUTER AIDED ENGINEERING TO VERIFY DESIGNS
	12:30 PM–2:30 PM	**SESSION 18** AI/EXPERT SYSTEMS	**SESSION 19** COMPUTER AIDED SOFTWARE ENGINEERING (CASE) TOOLS — IMPROVING PRODUCTIVITY	**SESSION 20** AUTOMATIC CONTROL AND CIM IN SEMICONDUCTOR MANUFACTURING		
	1:00 PM–4:00 PM				**SESSION 21** **SPECIAL SESSION** VIDEO SYSTEMS TECHNOLOGY: EVOLUTION OR REVOLUTION?	**MARRIOTT, ROOM SUNSET A IEEE REGION 6 STUDENT PAPER CONTEST**
	4:00 PM–6:00 PM	**SESSION 22** TEST AND MEASUREMENT APPLICATION SOFTWARE FOR THE PERSONAL COMPUTER	**SESSION 23** DEVELOPMENT TOOLS FOR RISC EMBEDDED CONTROLLERS	**SESSION 24** PC BOARD PROTOTYPES FOR $60 IN 60 MINUTES	**SESSION 25** FUTUREBUS +	
THURSDAY, NOVEMBER 16	8:30 AM–10:30 AM	**SESSION 26** **SPECIAL SESSION** 32-BIT EMBEDDED CONTROLLER	**SESSION 27** HIGH PERFORMANCE. COST EFFECTIVE FIBER OPTIC SOLUTIONS FOR DATA COMMUNICATION APPLICATIONS	**SESSION 28** DISTRIBUTED POWER FOR THE NINETIES		**SESSION 29** **SPECIAL SESSION** NEURAL NETWORKS FINAL APPLICATIONS
	12:30 PM–2:30 PM	**SESSION 30** SOFTWARE FOR RISC ARCHITECTURES	**SESSION 31** **SPECIAL SESSION** FLAT PANEL INFORMATION DISPLAYS	**SESSION 32** APPLICATIONS OF ADVANCED RECHARGEABLE BATTERIES FOR PORTABLE POWER		**SESSION 33** NEURAL NETWORKS IN THE REAL WORLD

Transportation and show details

Parking in downtown San Francisco is severely limited. Avoid parking problems at Moscone Convention Center and Brooks Hall/Civic Auditorium by taking the Cow Palace Shuttle. Park at the Cow Palace (parking costs $4 per day) and take the free shuttle to the show. If you take the BART (Bay Area Rapid Transit), the Civic Center stop is most convenient to Brooks Hall/Civic Auditorium. Powell Street is the stop for Moscone Convention Center. If you travel by bus, take the 21 Hayes or 19 Polk for Brooks Hall/Civic Auditorium; take 45 Union or 30 Stockton for Moscone Convention Center. The exact-change fare is $0.85.

Registration for those not preregistered costs $10 at the door. This fee admits you to both the Exhibits and the Professional Program. Your registration also admits you to the Electronic Theater. As you look through EDN's Wescon product section, you can map out a strategy for covering booths that interest you. Booths numbered lower than 2900 are in Moscone Convention Center, 4000 through 4700 are in the Civic Auditorium, and 5000 through 5900 are in Brooks Hall.

"Applied Modern Error Correction Coding Techniques" will address linear-coding techniques and their applications to modern communications and data-storage systems. "Use of SPICE Power for Modern Analog Circuit Simulation" will deal with the rapidly changing field of Spice-based simulators. Software designers can explore the "Essentials of the UNIX Kernel." Other design-oriented courses include "RISC Microprocessor Technology and Applications," "Grounding and Shielding of Electronic Instrumentation," as well as courses on fiber optics and power-supply design.

Wescon/89 will also highlight courses on "Optics and Computing," "Advanced Packaging for ICs and Semiconductor Devices," "Laser Applications in Material Processing," "Software Project Management Using DoD-STD 1703," and "ISDN, What It Really Is."

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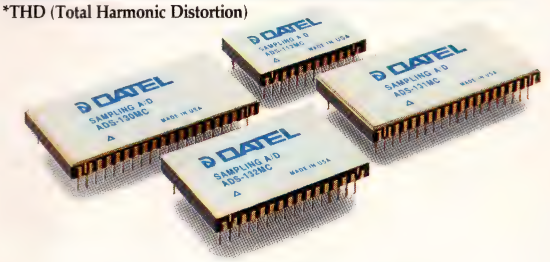
ADS-131	5MHz	10.6	-69 dB	4.2 watts	40-pin TDIP
ADS-130	10MHz	10.6	-69 dB	4.5 watts	40-pin TDIP

*THD (Total Harmonic Distortion)



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CIRCLE NO 111

256-Color Triple RAM + DAC

A second source to an industry standard, the ADV453 is a triple 8-bit video DAC with built-in RAM. The device can display as many as 256 colors from a palette of 16.8M addressable colors, as well as three additional colors from an overlay palette. Fabricated in a low-power CMOS process, the monolithic IC operates from a 5V supply and consumes <1W.

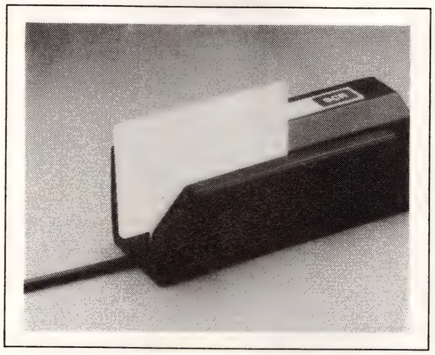
In addition to the triple DAC, the ADV453 contains a 256×24-bit palette RAM and a 3×24-bit overlay register to allow easy implementation of cursors, pull-down menus, and grids. Moreover, the device's 66-MHz video refresh rate makes it suitable for high-resolution color-graphics standards including IBM VGA and Macintosh II.

An independent, asynchronous bus allows the µP to update the color-lookup tables without affecting the input of data via the pixel port. The DAC outputs directly generate the RGB signals without any need for external buffering. The monotonic outputs have integral and differential nonlinearities of < ±1 LSB. Available in a 0.6-in., 40-pin DIP and 44-pin plastic leaded-chip carrier, the ADV543 operates in temperatures ranging from 0 to 70°C. 40-MHz version, from $35; 66-MHz version, from $45 (100).

Analog Devices Inc, Literature Center, 70 Shawmut St, Canton, MA 02021. Phone (617) 658-9400. Booth No. 2618. **Circle No. 439**

Bar-Code Reader

The BCR-6400 bar-code reader for cards or badges operates at scan rates from 10 to 120 ips. You can specify either 3×40-mil-slit or 10×37-mil-diamond viewing apertures as well as visible red (660 nm) or infrared (880 nm) illuminations. Optional indicators include power-on and good-read LEDs. The scanner's outputs are supplied through either an 8-pin modular, a 5-pin DIN, a 9-pin subminiature D, or a 9-pin squeeze-to-release connector. All outputs are either TTL compatible or open collector. The unit comes in a polycarbonate case with a stainless-steel wear plate. It measures 5.6×2.0 in. and weighs 8.5 oz. A mounting kit is sold separately. $240.



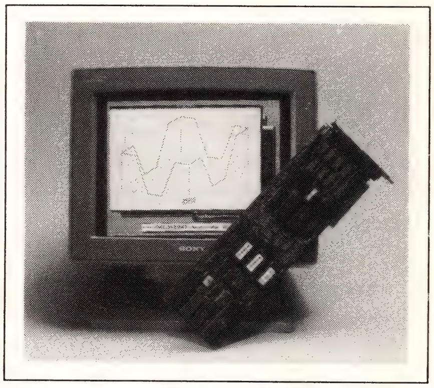
Welch Allyn Inc, Jordan Rd, Skaneateles Falls, NY 13153. Phone (315) 685-8945. FAX 315-685-3172. Booth No. 2532.

Circle No. 440

Motion-Control-Code Translator For PCs

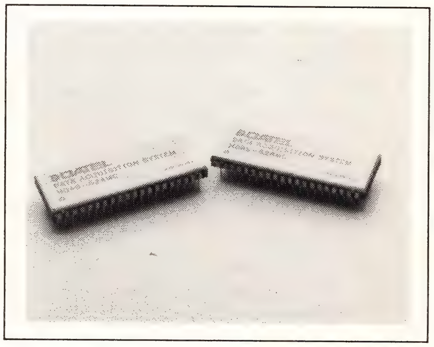
G-CODES-to-DMC is a software package that runs on IBM PCs and compatibles and translates a standard G-code text file into commands for the vendor's DMC-600 series of motion controllers. The program can handle commands for motion-control systems that have either two or three axes of motion. It can translate commands for linear positioning of one, two, or three axes, as well as circular interpolation of two axes. For smooth contouring, you can specify as many as 255 linear and arc segments along a continuous path. You can also synchronize motion commands with other process variables such as time, position, or external inputs and outputs.

The program is menu-driven, and when translation is complete you can either send the commands to the motion controller under control of a runtime executive or download the entire file to the controller's memory to run autonomously. G-CODES-to-DMC, $495; DMC-6202-axis controller, $1495; DMC-6303-axis controller, $1995.



Galil Motion Control Inc, 1054 Elwell Ct, Palo Alto, CA 94303. Phone (415) 964-6494. FAX 415-964-0426. Booth No. 549.

Circle No. 441



High-Speed, Data-Acquisition System

Operating at a throughput rate of 400 kHz, the 12-bit HDAS-524/528 hybrid circuits are complete data-acquisition systems. Each system contains a multiplexer, an instrumentation amplifier, a S/H circuit, an A/D converter, 3-state outputs, an onboard reference, and an internal clock.

The HDAS-524 has four differential inputs, and the HDAS-528 has eight single-ended inputs. A double-level multiplexing scheme enables additional multiplexer channel expansion. The instrumentation amplifier, which is characterized for gains of 1, 2, 4, 8, 10, and 100, allows full-scale unipolar or bipolar input ranges from 100 mV to 10V. An external resistor selects the gain range.

The HDAS-524 and HDAS-528 operate from ±15 and 5V supplies and are characterized for operation over the commercial and military temperature ranges. High-reliability versions are also available. $375 to $531 (1 to 24). Delivery, stock to eight weeks ARO.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX 508-339-6356. TLX 174388. Booth No. 1730, 1732, 1734.

Circle No. 442

MIL-STD-883, Dual-Port Video RAM

The MT42C4064 256k-bit, dual-port video RAM (VRAM) is designed to meet MIL-STD-883 class B, revision C. The company's military fabrication lines recently passed final inspection for JAN (Joint Army Navy) certification to MIL-STD-38510. The VRAM is composed of a standard 64k×8-bit dynamic RAM (DRAM) and four 256-bit data registers, which make up the serial-access memory (SAM) portion.

The MT42C4064 accomplishes data I/O and internal data transfer, using three separate bidirectional data paths: the 4-bit random-access I/O port, the four internal 256-bit-wide paths in the DRAM, and the 4-bit serial I/O port for the SAM. The remaining circuitry consists of the control, timing, and address-decoding logic. Each of the ports may be operated asynchronously and independently of the others except when they are transferring data internally.

The VRAM is available in speeds of 120-, 150-, and 200-nsec. Package

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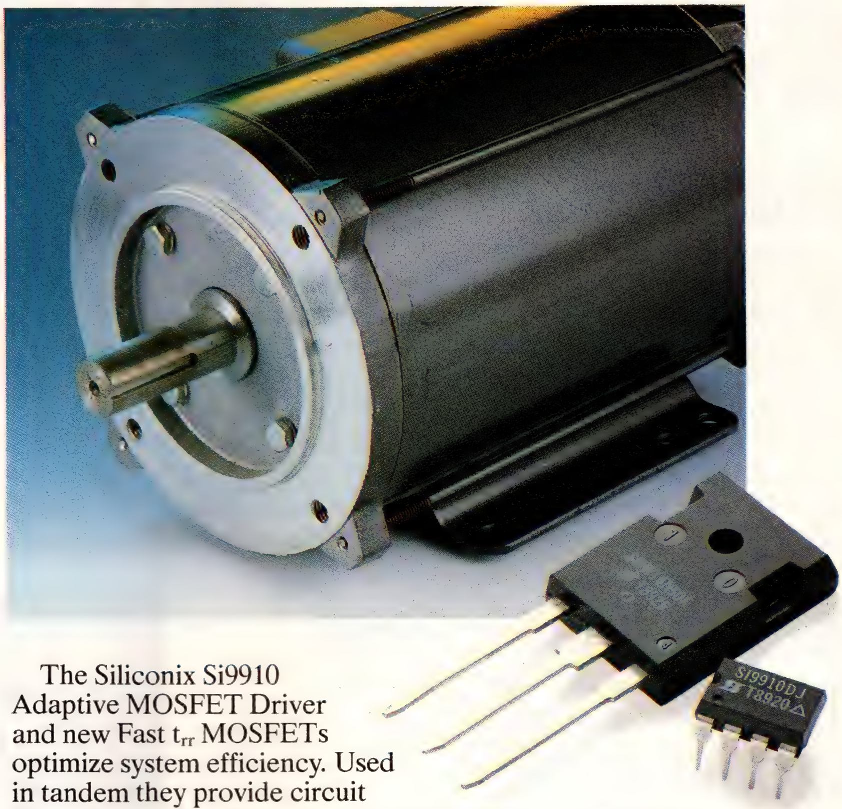
CIRCLE NO 112

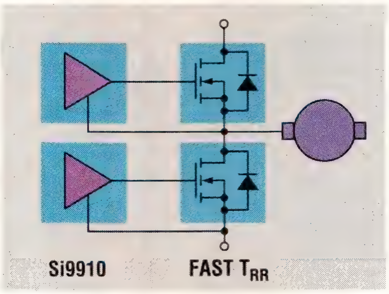
Improve your motor skills.

Siliconix' new system solution for more efficient motor control. Combine an Adaptive MOSFET Driver with Fast t_{rr} MOSFETs.



The Siliconix Si9910 Adaptive MOSFET Driver and new Fast t_{rr} MOSFETs optimize system efficiency. Used in tandem they provide circuit protection and logic interface in off-line motor applications.

This unique CMOS-compatible solution for variable-speed motor control significantly improves system performance. With five circuit protection features and lower power losses, the combined system results in higher reliability, smaller size, lower cost and reduced design time.



The Si9910 and Fast t_{rr} MOSFET family: system solutions for more efficient off-line control in motor drive and power supply applications such as major appliances, fans and blowers, industrial controllers, automobiles, power hand tools and UPS.

Improve your motor skills! Ask for your Si9910 and Fast t_{rr} Motor Control Design Kit. Call our toll-free hot line now! **1-800-554-5565, Ext. 946.**

Siliconix
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2201 Laurelwood Road, Santa Clara, CA 95054

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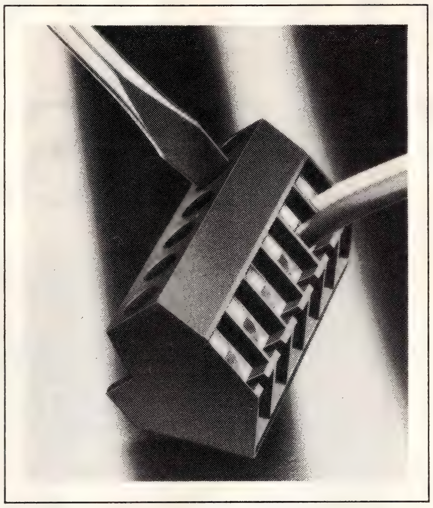
options include a 28-pin ceramic LCC and a 28-pin ceramic DIP. Depending on speed selection and package option, $30 to $110 (OEM qty). Delivery, stock to eight weeks ARO.

Micron Technology Inc, 2805 E Columbia Rd, Boise, ID 83706. Phone (208) 383-4000. FAX 208-343-2536. TWX 910-970-5973. Booth No. 5832. **Circle No. 443**

Terminal Strips For Printed-Circuit Boards



Featuring a 45° entry angle, Eurostyle terminal strips save space and provide safe access for wiring on crowded pc boards. They feature a 0.197-in. contact spacing that provides five terminations in less than an inch.

Eurostyle terminals have touch-proof recessed terminals and wire-ready captive screws that will not fall out and cause shorts. Captive wire protectors hold wires securely in place. The UL-recognized current rating is 15A, and the voltage rating ranges to 300V.

Other features include large wire entries, which will accept wire sizes to 14 AWG; a closed side that acts as a wire stop; and thermoplastic insulator material, which has a 94V-0 UL rating and a UL temperature index of 130°C. $0.18 per circuit (500).

Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. Booth Nos. 2551, 2553, 2555, and 2557.

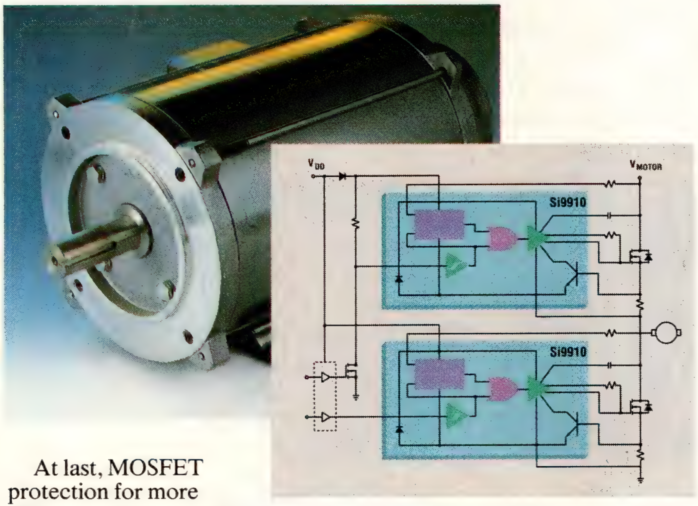
Circle No. 444

GaAs LED Indicators

Featuring a 2-mA forward-current requirement, Series 550 GaAs LED indicators are specifically designed for low-power pc-board applications. The indicators employ a T-1¾ LED light source and are available in a variety of package styles.

They are available in four board-mounting styles. One style mounts perpendicularly (LED and wire leads along the same axis). There are three right-angle packages and two with right-angle mounts (LED

MOSFET protection improves your motor skills.



At last, MOSFET protection for more efficient motor control!
The Si9910 Adaptive MOSFET Driver provides dv/dt and di/dt control, shoot-through current limiting, undervoltage protection and short-circuit protection. In addition, it drives the high or low side of an n-channel half-bridge.

Improve your motor skills! Ask for your Si9910 Motor Control Design Kit. Call our toll-free hot line now! **1-800-554-5565, Ext. 946.**

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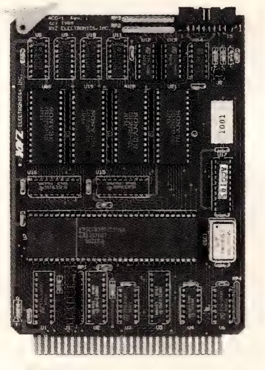
A Breakthrough in STD Bus Computer Graphics . . .

. . . the new XYZ ACG-1 (Advanced Color Graphics) card for the STD Bus features the Hitachi 63484 ACRTC (Advanced Cathode Ray Tube Controller) chip to minimize the software burden on the host processor. Designed for inclusion in real time and multi-tasking systems, full memory management is included for up to 256K of graphics memory (128K installed). This memory does not use, replace or interfere with normal system memory, making this board ideal for even the smallest system. Resolution is up to 640 x 400 (128K memory). Programmable resolution and sync rates can be tailored to almost any application including CGA and EGA monitors.

Call or write for information!



XYZ A NAME YOU'LL REMEMBER
ELECTRONICS INC.
Rural Route 12, Box 322
Indianapolis, IN 46236
Tel. Indiana 317-335-2128
Toll Free 800-852-6822
(except Indiana)

CIRCLE NO 116

and leads 90° apart), with one having a 45° slanted back. The fourth style also has a slanted back, but it is designed with small standoff feet molded into the bottom of the package to facilitate cleaning after wave soldering. All Series 550 indicators are housed in a black Valox package, which carries a 94V-0 UL rating. $0.54 (1000).

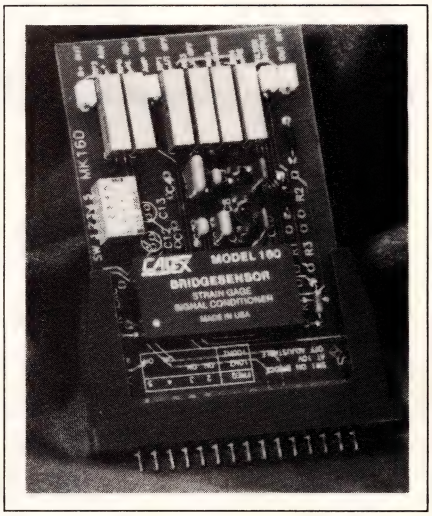
Dialight Corp, 1913 Atlantic Ave, Manasquan, NJ 08736. Phone (201) 223-9400. Booth No. 1918.

Circle No. 445

Signal Conditioner

Model 160MK Bridgesensor includes everything necessary for a strain-gauge-based, data-acquisition system. It features a bridge power-supply regulator, a differential amplifier, and an active filter with all the adjustments needed to calibrate and operate the device.

Filter corner frequency is switch selectable. The 160MK employs remote sensing to eliminate errors due to voltage drops on long lines. The bridge excitation is adjustable over a 4 to 12V dc range; the regulator delivers 100 mA for bridge excitation. You can optimize amplifier operation by setting coarse and fine gain, input offset, and output offset, using trimmers located on the board.



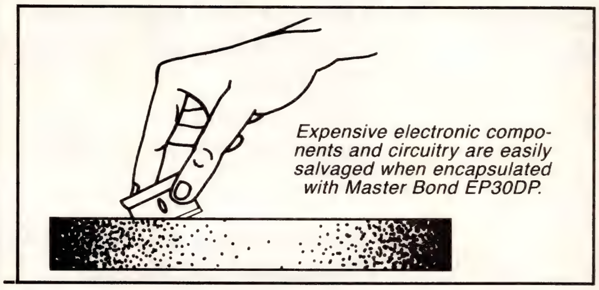
A bridge balance pot and bridge completion resistors located on the Model 160MK simplify operation even further. All you need to do to get the sensor system up and running is to connect it to a ±15V supply. $215.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (800) 542-3355; in CA, (415) 932-3911. FAX 415-932-6017. Booth No. 2019.

Circle No. 446

Text continued on pg 158

Encapsulant Provides Retrievability for Costly Electronic Components!



Expensive electronic components and circuitry are easily salvaged when encapsulated with Master Bond EP30DP.

Master Bond Polymer System EP30DP is that long sought after potting and encapsulation compound which features both superior environmental protection and retrievability upon demand for costly electronic components in case of malfunctions etc. It is a low viscosity, clear two component epoxy compound which can be readily mixed in a 4/1 mix ratio by weight and casts easily without creation of air bubbles, voids etc. Master Bond Polymer System EP30DP cures fully at ambient temperatures with minimal shrinkage to produce a tough semi-rigid thermoset plastic which can encapsulate even the most delicate electronic parts without damage. Components can be retrieved when desired by cutting away the encapsulant with a knife etc. or other mehanical means. It is available clear for visual inspection of the encapsulated components or in a number of colors as desired.

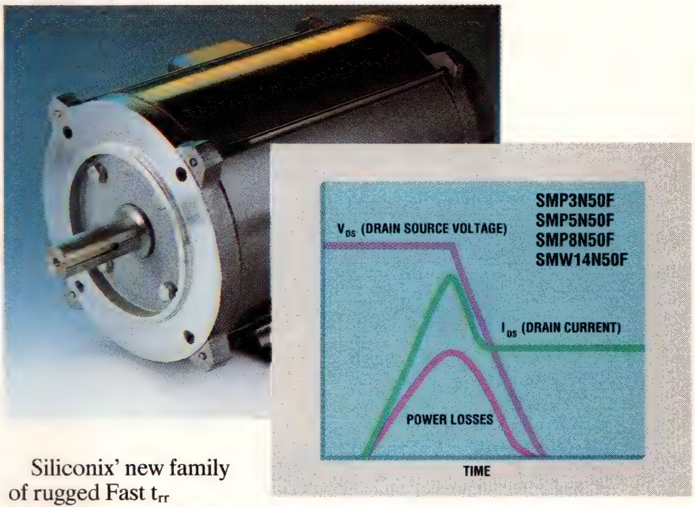
For information, call or write:

MASTER BOND, INC.

154 Hobart Street, Hackensack, N.J. 07601 • (201) 343-8983

CIRCLE NO 117

More efficient Power MOSFETs improve your motor skills.



Siliconix' new family of rugged Fast t_{rr} MOSFETs improves the efficiency, reduces the size and lowers the cost of motor control systems. And their low $R_{DS(ON)}$, solid dv/dt rating and fully characterized diodes make it easier to achieve high system reliability.

Improve your motor skills! Ask for your Fast t_{rr} Motor Control Design Kit. Call our toll-free hot line now! **1-800-554-5565, Ext. 946.**

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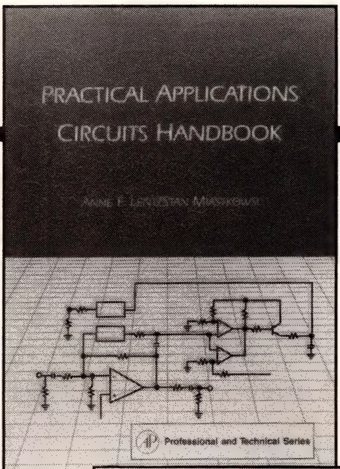

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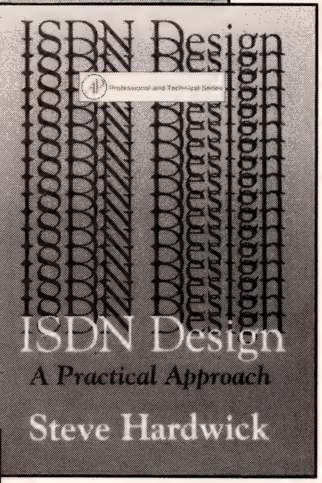

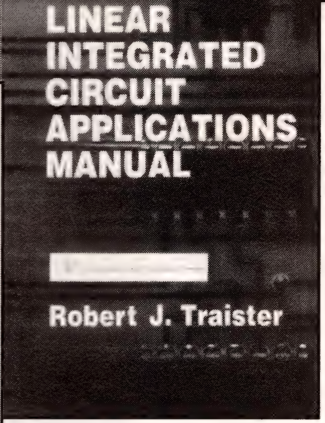

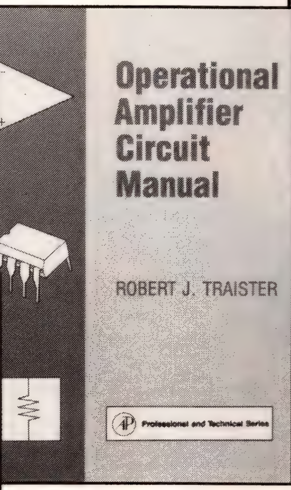
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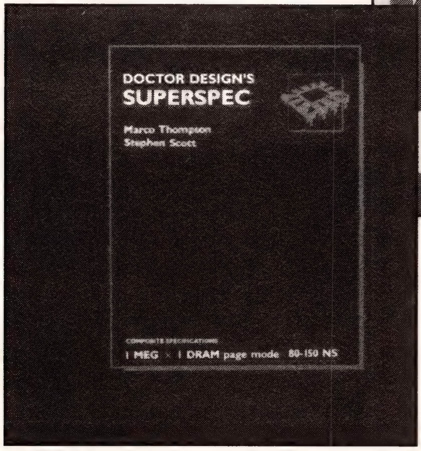

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Complete 50-MHz A/D Converter

The SP1078, a complete A/D converter in hybrid form, includes a 50-MHz flash converter with 3-state outputs, an onboard voltage reference, and a 50-MHz full-power-bandwidth buffer amplifier. The hybrid, which comes in a 24-pin double DIP hermetic package, consumes only 560 mW of power. The SP1078 is available in commercial (0 to 70°C) and military (−55 to +125°C) temperature ranges.

Key specifications include a sampling rate of 50M samples/sec for sampling signals as high as 25 MHz, a minimum S/N ratio plus distortion of 40 dB, a maximum differential nonlinearity of ±0.6 LSB, and a maximum integral nonlinearity of ±1 LSB. Other specs include aperture jitter of 50 psec, digital delay of 15 nsec, and a full-power amplifier bandwidth of 50 MHz.

The SP1078 has a 1V input range, which is usable in either bipolar or unipolar modes for binary or 2's complement coding. A summing node is available for external offset and gain adjustments; the reference is also available for external use. The converter operates from 5 and −5.2V supplies. Commercial version, $183; military version, $306 (100). Delivery, stock to 10 weeks ARO.

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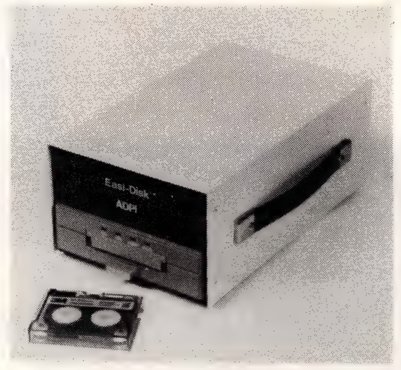

Cartridge System

The Easi Tape cartridge-tape system connects to a host that runs MS-DOS via an RS-232C port. When used with the company's MS-DOS software driver, the system can handle standard MS-DOS com-

Text continued on pg 162

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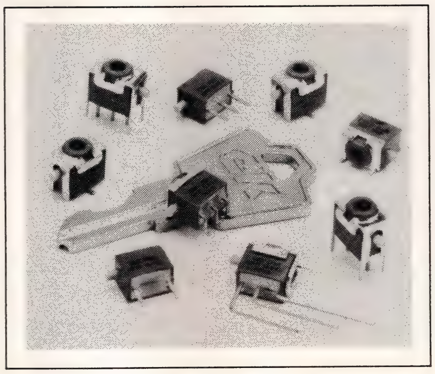
CIRCLE NO 121

mands such as "COPY" and "XCOPY." It provides 32M bytes of storage for 2.X and 3.X versions of MS-DOS and 40M bytes of storage for 4.X versions. Using a Reed Soloman error-checking code, the system provides an error rate of less than 1 error in 10^{14}. The host can communicate with the system at a baud rate ranging from 150 to 38.4k baud. In addition to an RS-232C interface, the device includes an IEEE-488 interface, an RS-422 interface, an RS-485 interface, a 20-mA current-loop interface, and an 8-bit parallel interface. The standalone unit measures 4×6×10 in. and weighs 6 lbs. It uses either 110 or 220V ac or 12 or 24V dc as a power source. $1295.

Analog & Digital Peripherals Inc, Box 499, Troy, OH 45373. Phone (513) 339-2241. FAX 513-339-0070. TWX 810-450-2685. Booth No. 1558. **Circle No. 448**



Pushbutton Switches

GP Series ultraminiature pushbutton switches are available for both through-hole and surface-mount applications. They are designed to withstand vapor-phase, infrared-reflow, and wave-soldering processes and are sealed to eliminate the intrusion of flux, solvents, or other contaminants during cleaning processes.

Switch features include high-temperature thermoplastic housings (UL 94V-0 rating), epoxy base and terminal sealing, and internal O-ring actuator seals. GP switches are available in spst and spdt momentary-action configurations. They come in straight, right-angle, and support bracket terminal styles with pin spacings of 0.100 or 0.050 in. Tin-lead terminal plating is standard. From $1.90 (1000).

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400. Booth Nos. 2318, 2320, and 2322.

Circle No. 449

Heat Sinks For DC/DC Converters

Two heat sinks are specifically designed for cooling 2.4×4.6-in. dc/dc converters. The models accommodate different air-flow directions: Model 410011 has lengthwise fins, and Model 410111 has crosswise

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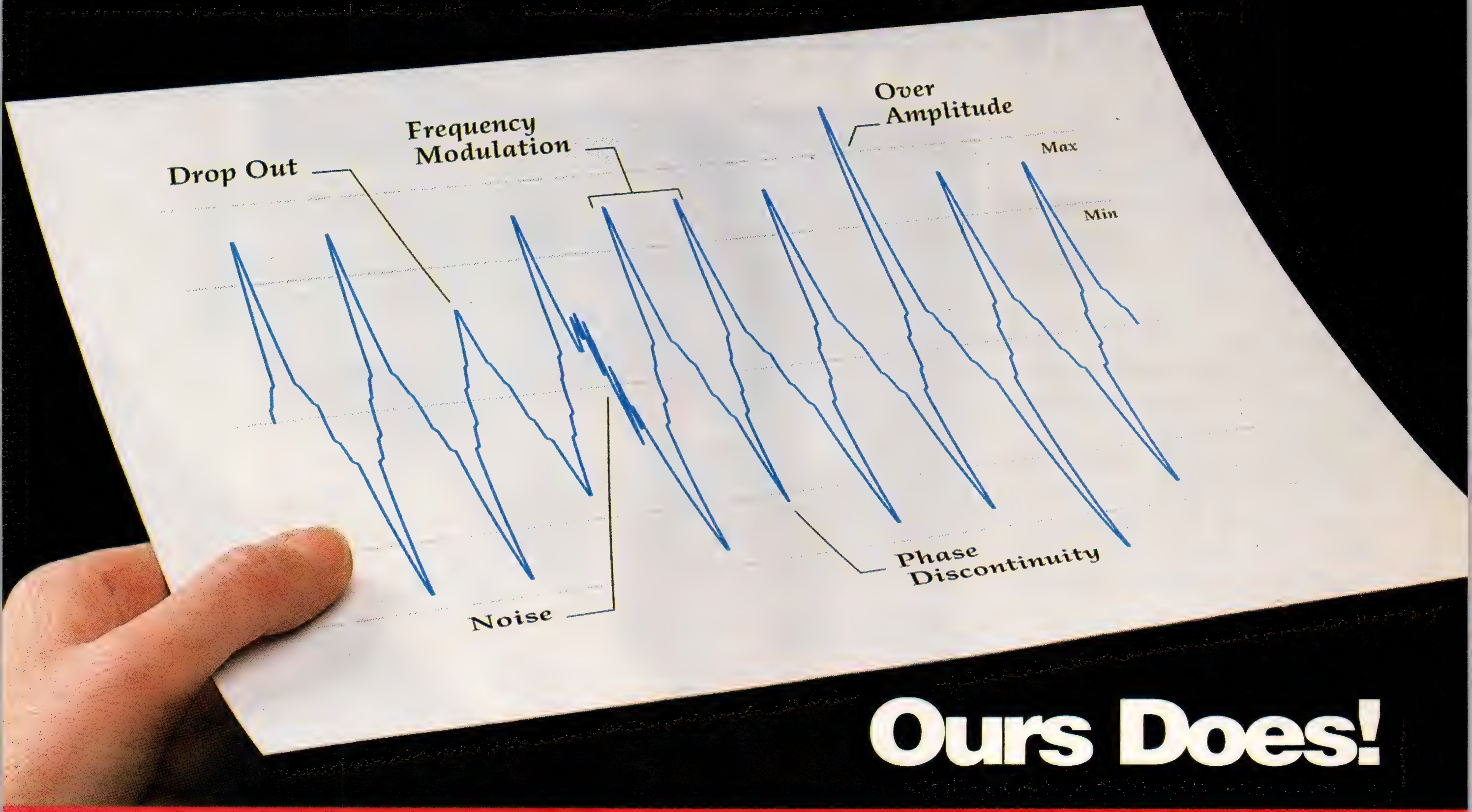
CIRCLE NO 122

Does Your Signal Generator Simulate The Real World?



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The LeCroy Arbitrary Function Generators

The ideal signal source for testing duplicates any worst case signal that a DUT can encounter including variations in shape, frequency, duty cycle, amplitude, phase, and even noise.

Now there is such a source, the LeCroy Arbitrary Function Generator. You can create signals of any shape and vary all the parameters singly or simultaneously, separately or interactively. And the generation of test waveforms is not a problem. LeCroy's EASYWAVE® software is a complete toolkit for making test waveforms from scratch. Whether you choose to create waveforms by using equations, select elements from our library of simple elements, or even by acquiring real world signals with a digital oscilloscope! In minutes you will be building your signal; in an hour you'll be an expert.

Three models offer a choice of single, dual, or both analog and digital outputs. All have 100 MHz bandwidth (200 MHz clock), ± 10 V p-p swing, 5 ns risetime, and other characteristics optimized for high speed, high fidelity applications.

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Circle 8 for Information **Circle 9 for Demonstration**

700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977-6499 USA

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- *Leading Supplier of DC DC converters.*
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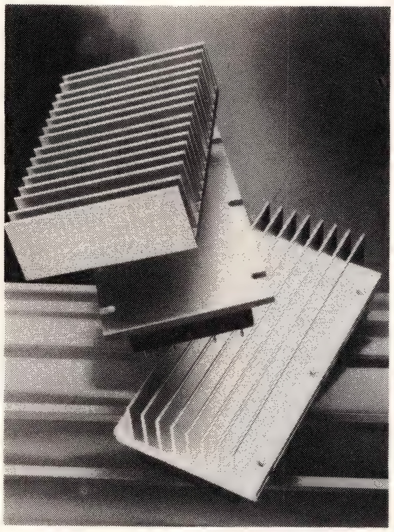
CIRCLE NO 123



fins.

The mounting surface is machined flat to provide maximum metal-to-metal contact for minimum interface resistance. Under natural convection, thermal resistance is 3.5 and 3.0°C/W for the 410011 and 410111, respectively. Thermal resistance under forced-air convection ranges from 0.6°C/W at 1000 linear ft/minute to 2.0°C/W at 100 linear ft/minute for the 410011. Respective figures for the 410111 range from 0.5°C/W at 1000 linear ft/minute to 1.5°C/W at 100 linear ft/minute.

The 2.4×4.6×0.9-in. heat sinks are made of aluminum alloy and come in gold chromate or black anodize finishes. Model 410011, $4.21; Model 410111, $4.23 (1000). Delivery, stock to six weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400. Booth No. 2730.
Circle No. 450

Data-Acquisition Card For IBM PCs

The Lab-PC data-acquisition board for the IBM PC, PC/XT, PC/AT, and compatible computers can digitize data having 12-bit resolution at rates as high as 60 kHz. It has eight analog-input channels that are multiplexed into a single channel. The

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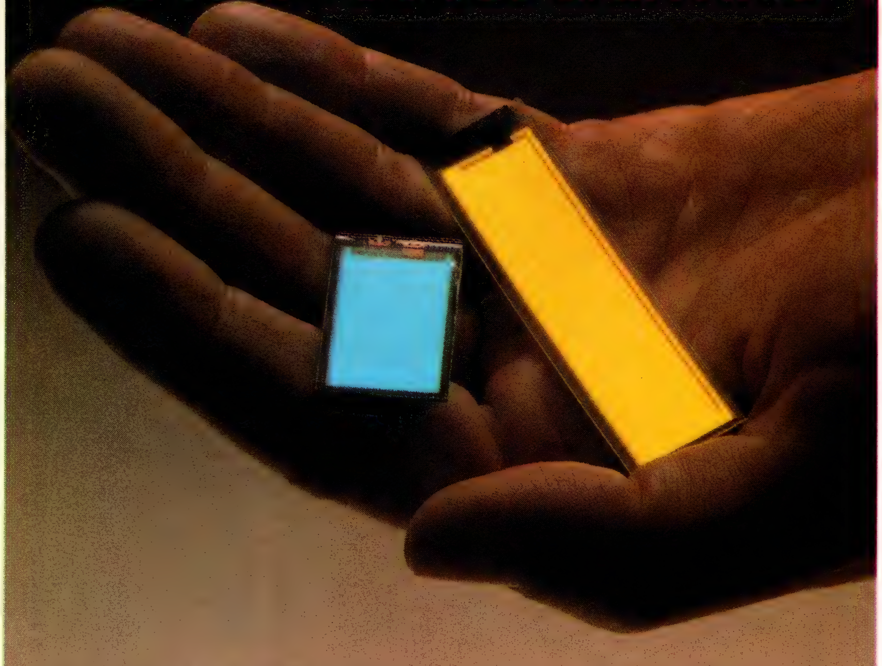
- *Reverse polarity protected*
- *No-load protected*

A self-adjusting DC-AC inverter that matches performance to EL lamp capacitance changes, to extend lamp-life and optimize brightness. (For more information, see Loctite ad, below.)

Nothing Turns On EL Lamps Like Our Inverters.
LOCTITE LUMINESCENT SYSTEMS INC



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WE'D LIKE TO SEND YOU ONE OF OUR EL LAMPS–
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Only our electroluminescent (EL) lamps can take it. Because only our EL lamps combine solid-state technology with Loctite quality and reliability.

These lamps, available in a wide range of sizes, shapes and colors, will survive under conditions that destroy incandescents and even other ELs. Our DC-AC inverter line, designed to match any lamp size and desired output, assures maximum lamp performance–uniform surface illumination and useful life exceeding 10,000 hours.

HERE'S HOW TO GET ONE, SO YOU CAN SEE FOR YOURSELF.
Just send this ad, along with your business card, to Mike Hartman, our Marketing Manager. Along with our DESIGN GUIDE, he'll send you a sample EL lamp–both free. After you kick it around for a while, you'll understand why we say–no other light can hold a candela to ours.

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FAX (603) 448-3452, TWX 710-366-0607
Etna Rd., Lebanon, NH 03766

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CIRCLE NO 124

Some designers already take enclosures very seriously.

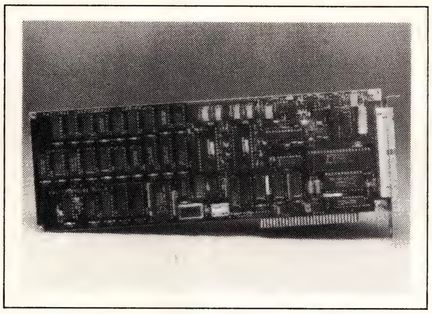
Successful designers call it their "how-to book" for perfection. It's filled with the most advanced, aesthetically beautiful packaging solutions in the world.

The comprehensive Rittal Handbook. It's easy to get, and it's free. Just give us a call and we'll tell you how you can take your designs all the way to perfection…with enclosure systems from Rittal.

1-800-637-4425

RITTAL Corporation, 3100 Upper Valley Pike, P.O. Box 1284, Springfield, Ohio 45504, Tel: (513) 399-0500, Fax: (513) 390-5599
CANADA, RITTAL LTD., P.O. Box 986, Oakville, Ontario L6J5E8, Tel: (416) 338-2440, Fax: (416) 845-5901, Telex: 6968914

CIRCLE NO 307



board provides two 12-bit analog-output channels and 24 digital I/O lines. Three counter/timers can measure time-critical signals. The company offers three software packages for programming the board. The LabDriver software has ready-to-go routines for data acquisition, using DMA and waveform generation. The libraries run with Microsoft C and QuickBasic languages. The board also works with MS-DOS version 2.0 and the company's LabWindows instrumentation software. Board, $695; LabDriver, $95; MS-DOS 2.0 drivers, $295.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488; in TX, (512) 794-0100. TLX 756737. Booth No. 959. **Circle No. 451**

Military-Rated Isolation Amplifier

According to the company, the AD203SN is the first isolation amplifier tested and specified over the full −55 to +125°C temperature range. The amplifier is also evaluated using MIL-STD-883 tests. Specific testing includes Class 2 ESD sensitivity, 1500g of mechanical shock, and 20g vibration tolerance. The AD203SN can also tolerate 1500V rms of common-mode voltage.

The amplifier's full-power input bandwidth of 10 kHz accommodates high-frequency signals from ac-excited bridge transducers, and its typical 0.012% nonlinearity allows the device to work in 12-bit accurate systems. Other key specifications include a maximum offset voltage of $\pm(5+25/G)$ mV (G = gain) and a typical offset-voltage drift of $\pm(6+100/G)$ μV/°C.

Based on a 2-port, transformer-coupled design, the AD203SN eliminates the need to use an expensive military-specified dc/dc converter to power the front-end circuitry. The amplifier operates from a single 15V supply and transfers both power and signals across the isolation barrier. Isolated power, rated at ±15V at 15 mA, is also available to power three or four external op amps.

On the input (isolated) side of the

Text continued on pg 170

WE CAN GET YOU AROUND YOUR LIGHTING PROBLEMS.

Our electroluminescent (EL) lamps give you light that's easy to work with.

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We can also provide a DC-AC inverter that is carefully matched to your lamp, insuring optimum performance over its life.

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And with our lamps, we give you solid-state-of-the-art construction backed with our Loctite applications know-how. So for solutions to any problem, we're here. To learn more, send for our DESIGN GUIDE, the definitive reference on electroluminescence. Because the solution to your lighting problem may be as simple as seeing it in a new light.

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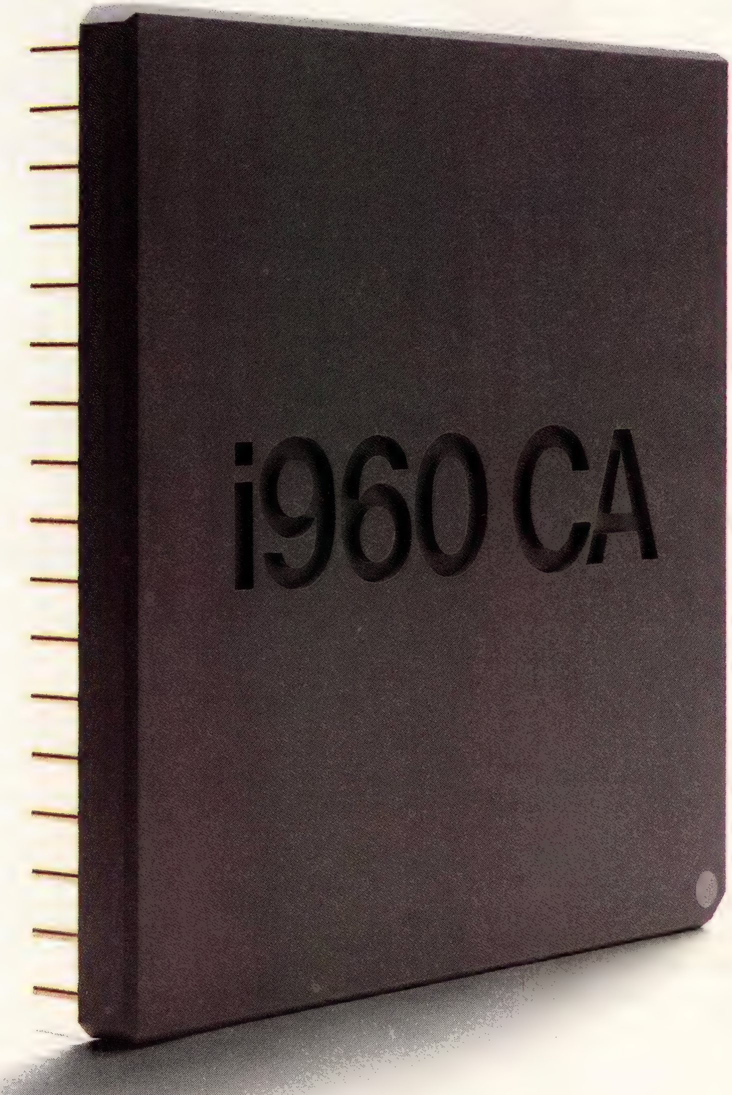
CIRCLE NO 125

Multiple instructions per clock is not a barrier.



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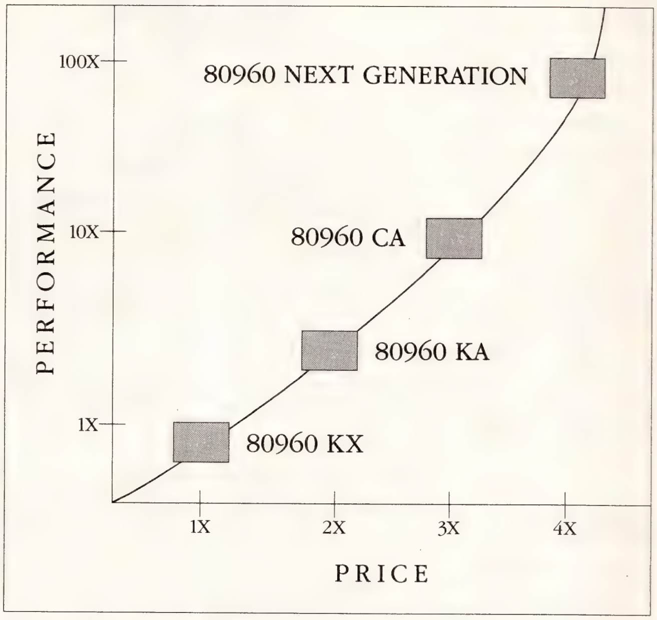
It's a milestone.

Multiple instructions per clock is now a reality. Intel's new i960 CA is the first 32-bit embedded processor to execute multiple integer and control instructions per clock.

The i960 CA is the first processor to implement SuperScalar architecture on a single chip. It consistently breaks the multiple instructions per clock barrier because it looks ahead in the data stream and selects groups of instructions to safely begin executing at the same time.

Thus the i960 CA allows you to reduce design costs by using less expensive memory and peripherals, at the same time you enjoy its unprecedented performance. In its 33-MHz version, the i960 CA can sustain 66 native MIPS.



For 32-bit embedded control, i960 architecture offers a broad and growing range of price-performance options.

But as pleased as we are with its performance, we're also proud of the i960 CA as an Intel milestone. It's part of the i960 family of products that will remain software-compatible for generations.

The world's most highly
integrated 32-bit embedded processor:

☐ Instruction cache: 1-kb, two-way, set-associative
☐ SRAM: 1.5 kb one-clock access (15 frames 16 × 32 bit registers)
☐ General purpose registers: 32 × 32 bit
☐ I/O channel processor: data chaining, 4-channel DMA's
☐ Interrupt processor: 248 possible vectors
☐ Programmable bus controller: 8/16/32-bit environments

Intel gives you the support components and tools you need to get up to speed, including memories and peripherals specifically designed to work with the i960. Plus, we offer compilers, software debuggers, performance simulators, and macro assemblers to provide easy access to the full capabilities of the i960 CA.

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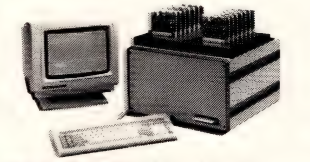

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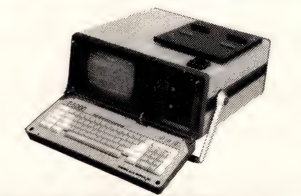
- 660 Watts of programming power
- MS-DOS compatible

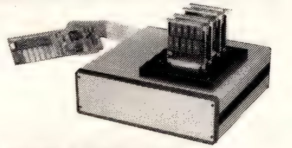
T-6000 BRIEF CASE PORTABLE IN-CIRCUIT PROGRAMMER

- Optional lift out UV board size eraser
- Program several boards in one pass
- 3.5 inch, 1.2 MB floppy
- Rugged, shock mounted case, water tight



T-5000 TRANSPORTABLE MS-DOS BASED IN-CIRCUIT PROGRAMMER

- Program several boards in one pass
- 20 MB hard disk, 3.5 inch floppy
- Rugged, shock mounted construction



T-4000 LOW COST IN-CIRCUIT PROGRAMMER

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- Program whole circuit cards in one pass
- Supplied turnkey or develop your own interface using built-in self guided, menu driven software

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CIRCLE NO 127

amplifier, users can program the gain from 1 to 100V/V with two external resistors, which set input voltage ranges from ±10 to ±0.1V. The amplifier's output side has an internal buffer amplifier that can drive low-impedance loads to a full-scale output of ±10V. The AD203SN is packaged in a plastic 2.23×0.83×0.6-in. DIP. $58 (100).

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-4065. Booth No. 2618. **Circle No. 452**

80486 In-Circuit Emulator

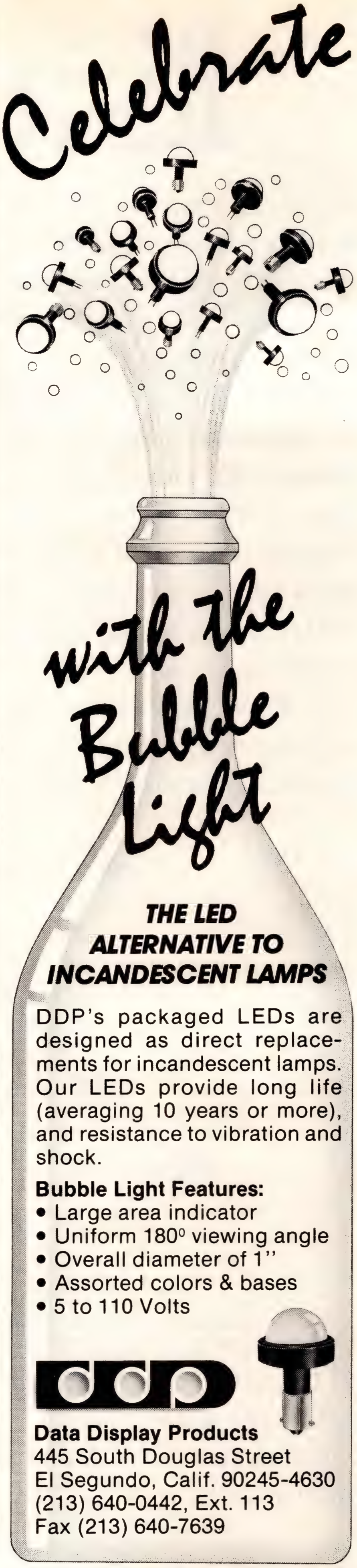
The HyperICE-486 is a true real-time in-circuit emulator for Intel Corp's 80486. The unit, whose trace buffer is 8k frames deep, supports the 32-bit µP in its current 25-MHz version and will support the 33-MHz version when it becomes available. The HyperICE-486's features are a superset of those of the vendor's HyperICE-386, which supports the 80386. You can use the emulator with a PC, a mainframe, a workstation, or a terminal. HyperSource, a high-level-language debugger with support for C, Ada, and PL/M, operates on a PC and utilizes a windowed interface. $24,990; delivery, 45 days ARO.

Microcosm Inc, 15275-E SW Koll Pkwy, Beaverton, OR 97006. Phone (503) 626-6100. FAX 503-644-9906. TLX 759527. Booth Nos. 1144 and 1146. **Circle No. 453**

Process Meter/Controller

You can program the Model P6004, a µP-based, 6-digit ⅛-DIN panel instrument, to operate as a flow-rate indicator/controller or an accumulating flow indicator/controller. The P6004 has an integral V/F converter, which accepts 4- to 20-mA, 0 to 10V, or 0 to 2V analog inputs; the P6000 accepts pulse inputs.

Programmable features include a 6-digit scale factor for display in en-



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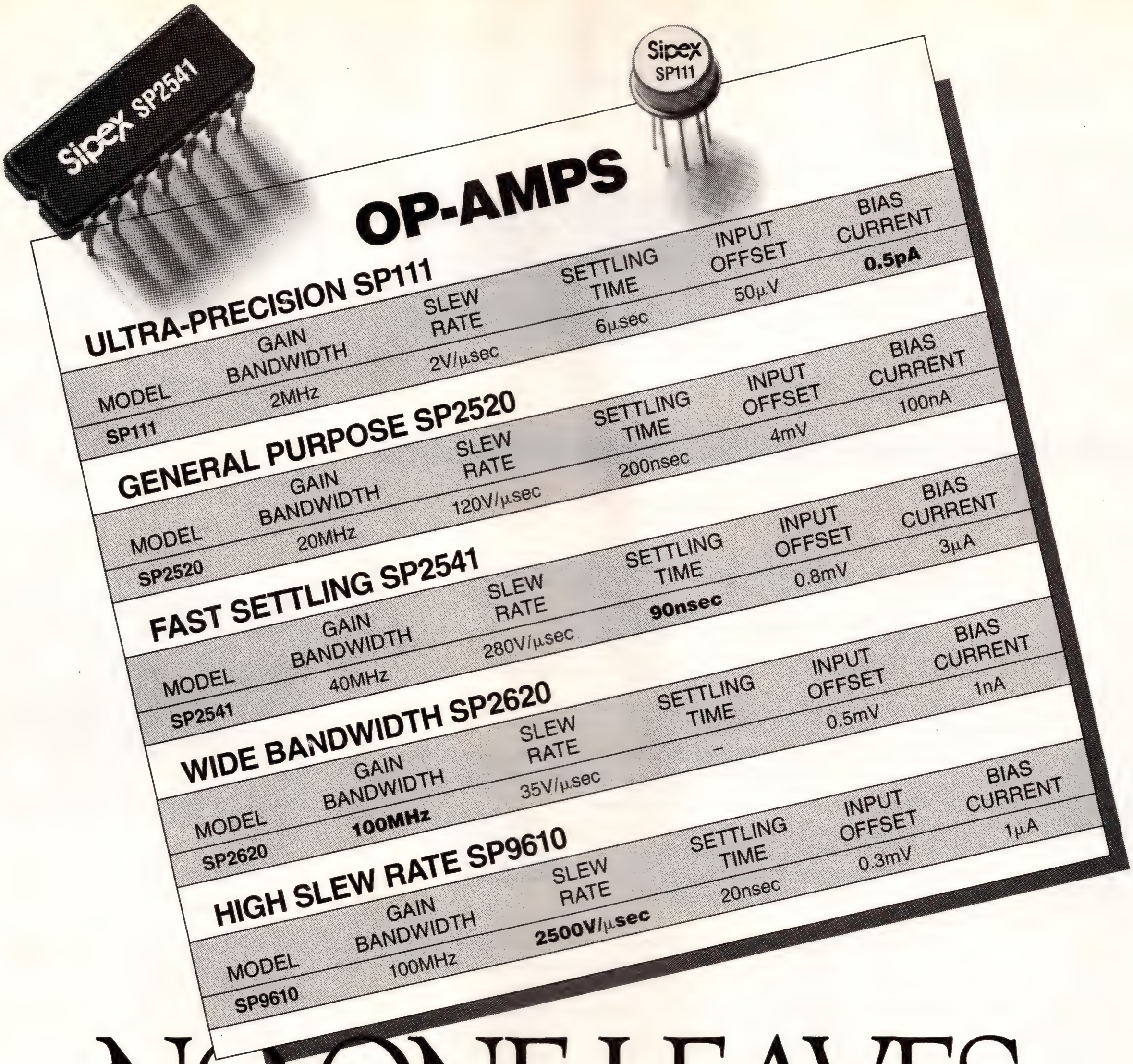
Sipex SP2541
Sipex SP111

OP-AMPS

ULTRA-PRECISION SP111

MODEL	GAIN BANDWIDTH	SLEW RATE	SETTLING TIME	INPUT OFFSET	BIAS CURRENT
SP111	2MHz	2V/µsec	6µsec	50µV	**0.5pA**

GENERAL PURPOSE SP2520

MODEL	GAIN BANDWIDTH	SLEW RATE	SETTLING TIME	INPUT OFFSET	BIAS CURRENT
SP2520	20MHz	120V/µsec	200nsec	4mV	100nA

FAST SETTLING SP2541

MODEL	GAIN BANDWIDTH	SLEW RATE	SETTLING TIME	INPUT OFFSET	BIAS CURRENT
SP2541	40MHz	280V/µsec	**90nsec**	0.8mV	3µA

WIDE BANDWIDTH SP2620

MODEL	GAIN BANDWIDTH	SLEW RATE	SETTLING TIME	INPUT OFFSET	BIAS CURRENT
SP2620	**100MHz**	35V/µsec	–	0.5mV	1nA

HIGH SLEW RATE SP9610

MODEL	GAIN BANDWIDTH	SLEW RATE	SETTLING TIME	INPUT OFFSET	BIAS CURRENT
SP9610	100MHz	**2500V/µsec**	20nsec	0.3mV	1µA

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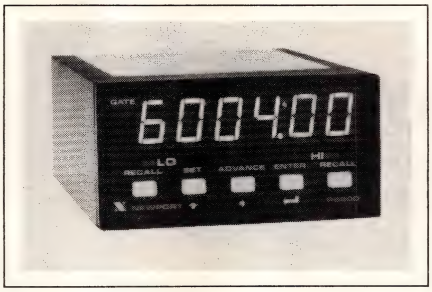
CIRCLE NO 129

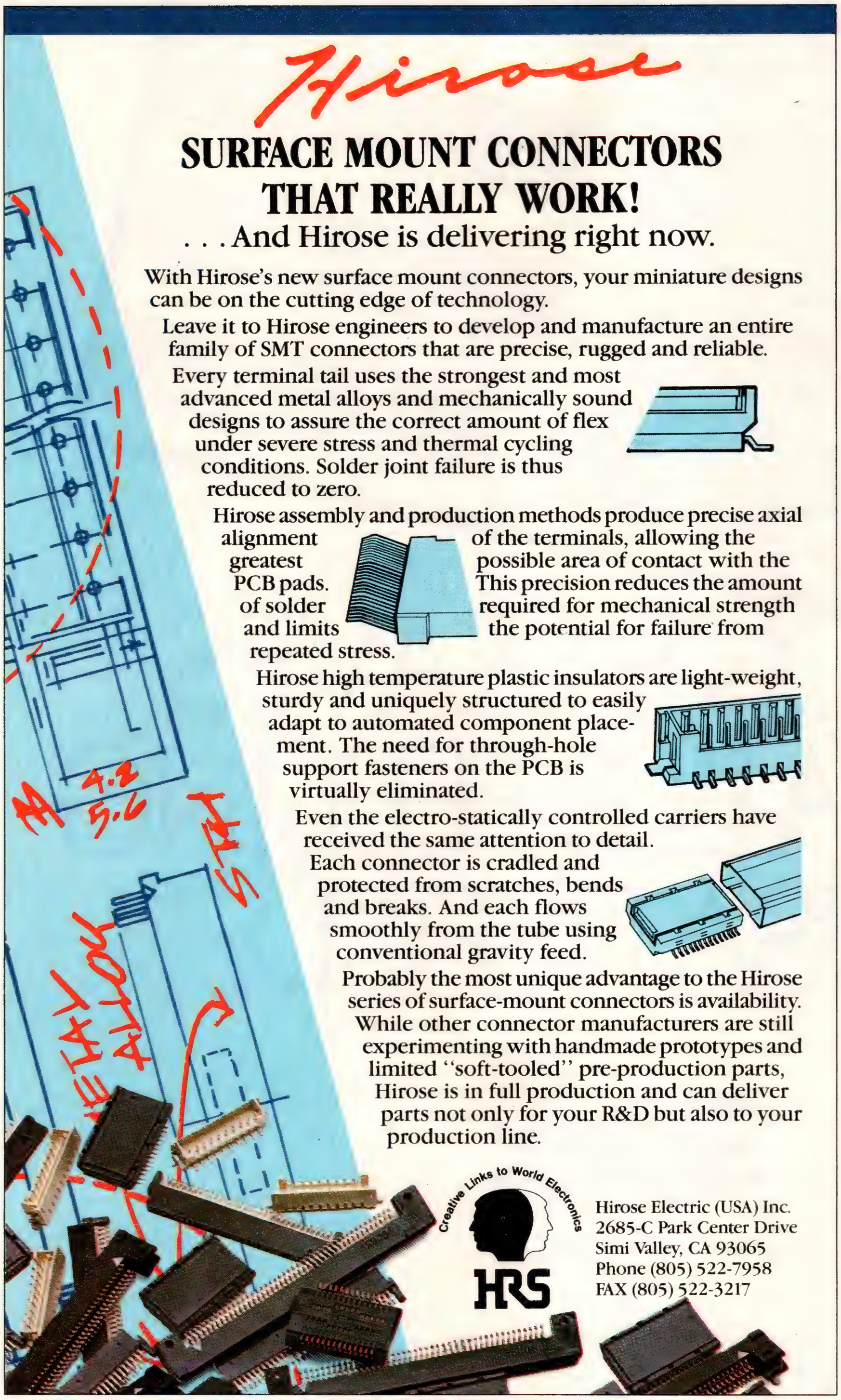
gineering units, a 6-digit offset or preset (any decimal point), and two on/off setpoints with open-collector outputs for control or alarm applications. All setup information is stored in nonvolatile RAM, which requires no battery backup.

The P6004 provides four levels of lockout for program security. You can use the RS-232C interface with modem support, which is standard, for remote programming and measurements. Options include dual 8A Form C relays, isolated 3-state parallel BCD output, and isolated 4-to 20-mA or 0 to 10V analog outputs. P6004, $374; P6000, $275.



Newport Electronics Inc, 2229 S Yale St, Santa Ana, CA 92705. Phone (714) 540-4914. FAX 714-546-3022. Booth No. 1153.

Circle No. 454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Hirose high temperature plastic insulators are light-weight, sturdy and uniquely structured to easily adapt to automated component placement. The need for through-hole support fasteners on the PCB is virtually eliminated.

Even the electro-statically controlled carriers have received the same attention to detail. Each connector is cradled and protected from scratches, bends and breaks. And each flows smoothly from the tube using conventional gravity feed.

Probably the most unique advantage to the Hirose series of surface-mount connectors is availability. While other connector manufacturers are still experimenting with handmade prototypes and limited "soft-tooled" pre-production parts, Hirose is in full production and can deliver parts not only for your R&D but also to your production line.

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See us at Wescon '89, Booths 4216-4218,
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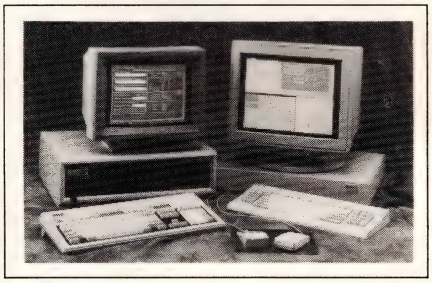
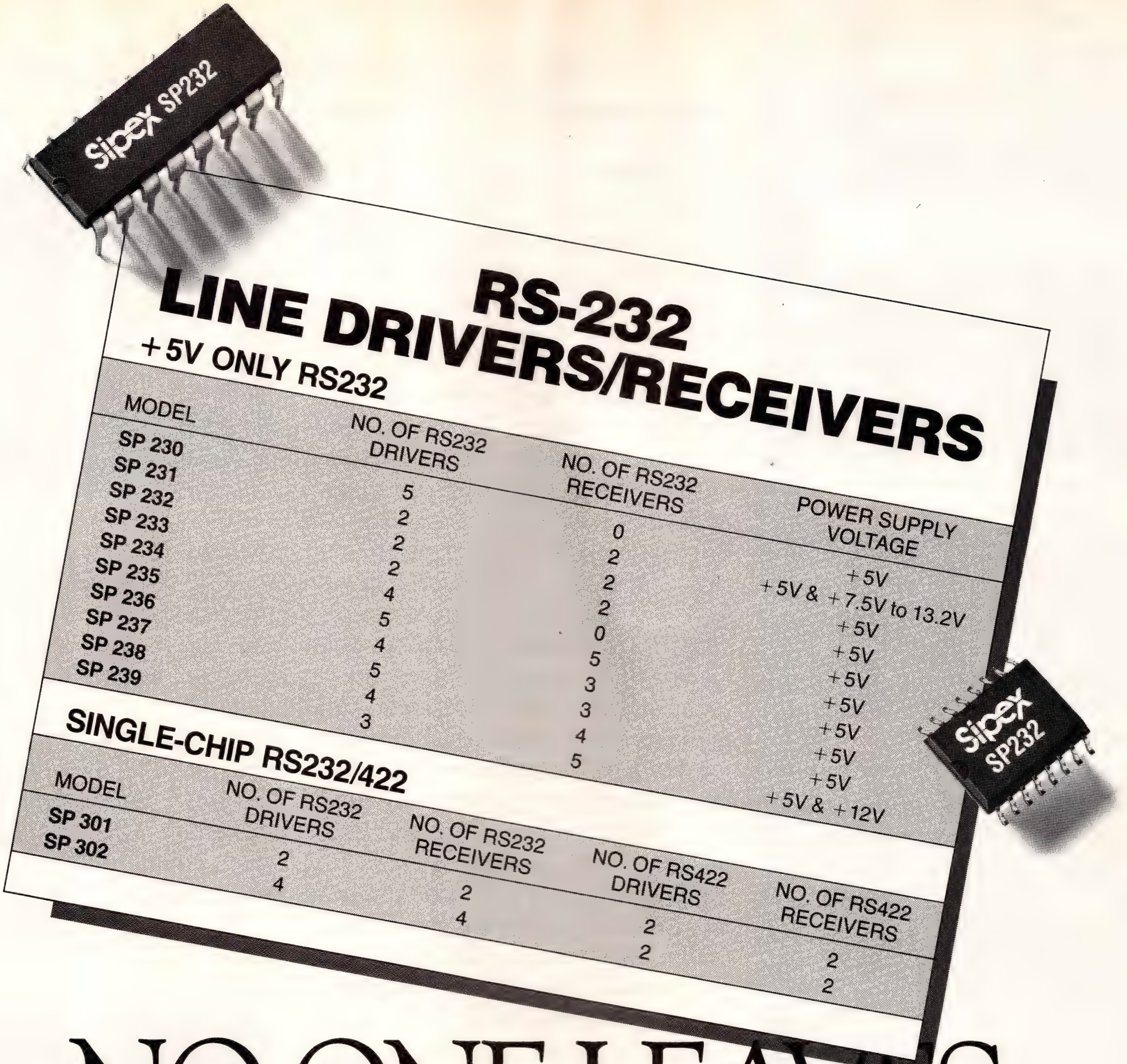


Automatic Test-Vector Generator For PLDs

The PLDtest Plus software package generates test vectors For PLDs. It accepts input in JEDEC standard 3A format or in Abel intermediate file format. Outputs include JEDEC standard 3A format, Abel "include" format, and generic test-vector format. The program can supplement user-supplied test vectors or can generate a complete new set of test vectors, whichever will achieve the maximum fault coverage for the targeted device in your design. The program provides separate lists of faults detected by the user-supplied test vectors and of faults detected by program-generated test vectors. In addition, the program provides performance statistics that help you analyze the testability of your design. Version for IBM PCs, PS/2s, and 80386-based computers, $5995; version for Sun-3 workstations, $9600.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX 206-882-1043. TLX 152167. Booth No. 1437.

Circle No. 455



RS-232 LINE DRIVERS/RECEIVERS

+5V ONLY RS232

MODEL	NO. OF RS232 DRIVERS	NO. OF RS232 RECEIVERS	POWER SUPPLY VOLTAGE
SP 230	5	0	+5V
SP 231	2	2	+5V & +7.5V to 13.2V
SP 232	2	2	+5V
SP 233	2	2	+5V
SP 234	4	0	+5V
SP 235	5	5	+5V
SP 236	4	3	+5V
SP 237	5	3	+5V
SP 238	4	4	+5V
SP 239	3	5	+5V & +12V

SINGLE-CHIP RS232/422

MODEL	NO. OF RS232 DRIVERS	NO. OF RS232 RECEIVERS	NO. OF RS422 DRIVERS	NO. OF RS422 RECEIVERS
SP 301	2	2	2	2
SP 302	4	4	2	2

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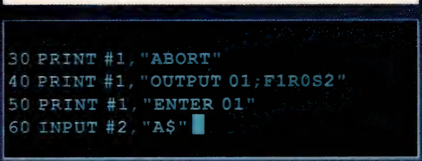
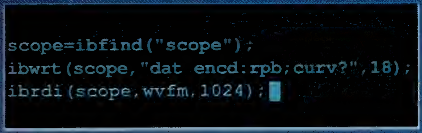


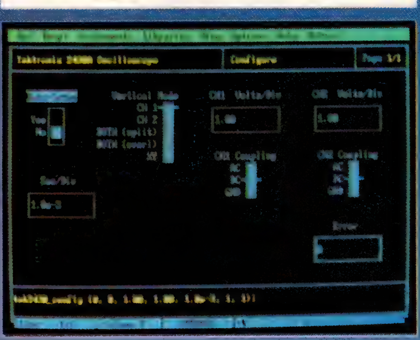
```
30 PRINT #1,"ABORT"
40 PRINT #1,"OUTPUT 01;F1R0S2"
50 PRINT #1,"ENTER 01"
60 INPUT #2,"A$"
```

High-speed compiled language users



```
scope=ibfind("scope");
ibwrt(scope,"dat encd:rpb;curv?",18);
ibrdi(scope,wvfm,1024);
```

Application Software



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CIRCLE NO 132

See us at WESCON booth #959

Wescon/89 Products

PC-Board Design System

AutoPCB release 5.3 has been greatly enhanced with features that facilitate the design of SMT (surface mount technology) boards. The program works with AutoCAD, release 9 or later, which provides the user interface and extensive documentation facilities. The layout provides the following features: It allows you to switch an SMT component interactively from one side of the board to the other; it allows you to use metric dimensions in conjunction with US dimensions; and it provides a parts library that lets you include your corporate part numbers as well as the vendor's part numbers. The logic symbols conform to ANSI standards. The autorouter can route to surface-only pads and can incorporate blind and buried vias. The package includes interfaces to Spice for analog simulation and to Susie for logic simulation. Any changes that you make to reference designators during layout are automatically back-annotated to the schematic. Prices start at $495 for a schematic-capture and parts-placement package that runs on IBM PCs and compatibles.

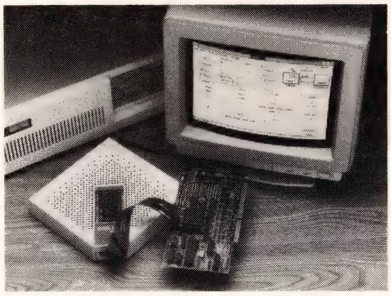
Cadisys Corp, 624 E Evelyn Ave, Sunnyvale, CA 94086. Phone (408) 732-1832. FAX 408-732-1832. Booth No. 1342. Circle No. 456

2-GHz Pattern Generator

The PG-2500 pattern generator produces 4-bit-wide pulse patterns to 2 GHz and 8-bit-wide patterns to 1 GHz. The unit can store 4-bit × 32k-frame or 8-bit × 16k-frame sequences. You can shift the outputs (individually in the 1-GHz mode and in pairs in the 2-GHz mode) over a range of ±2 nsec with 10-psec resolution and an error of <100 psec. You can control the internal clock's frequency in increments of 1% from 10 MHz to 2 GHz. You must use either an IBM PC/AT-compatible computer or an 80386-based PC with the industry-standard bus as the host. The computer must have an IBM EGA video controller, a high-resolution color monitor, a hard disk with at least 10M bytes available, and a National Instruments PC 2A IEEE-488 interface. Such a computer can control as many as eight units. $75,000.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479. Booth No. 856.

Circle No. 457



In-Circuit Verifier For Programmable Gate Arrays

The Mesa I is a multipurpose, hardware-based in-circuit verifier for troubleshooting field-programmable gate arrays. At present, the verifier supports logic-cell arrays (LCAs) from Xilinx and AMD. The unit lets you view the internal states of a device operating in a target system and, while you are doing so, lets you change stimuli to isolate problems. The verifier consists of a probe and cable assembly, an 8½×8×½-in. pod (which, itself, contains 12 LCAs), a Microsoft Windows-based software package,

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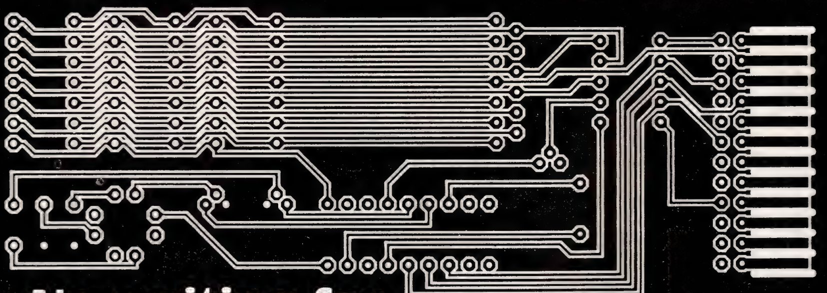
Introducing software that thinks. There has never been personal computer design and drafting software this powerful, this fast or this intuitive. Vellum thinks. Its radical new technology automatically pinpoints and aligns geometry as you draw. Built-in intelligence allows you to draw virtually freehand, yet set precise dimensions at any time. Finally, the days of complex commands and weeks of training are gone. Vellum has made industrial-strength design click on the Macintosh. For a demonstration see your Ashlar dealer or call (408) 746-3900.

ASHLAR
Software That Thinks™

CIRCLE NO 133

*Single-sided, actual size



No waiting for prototype boards from CAD...

BoardMaker™ made this ready-to-stuff board* in 22 minutes!

Whatever your CAD system, BoardMaker lets you get your hands on ready-to-stuff boards fast: in an hour or just several hours—depending on board size and complexity.

BoardMaker works with virtually all CAD systems, milling and drilling SMT, single- and double-sided boards in copper-clad from your Gerber files.

Low cost breakthrough.
You'll pay for a BoardMaker after making 12 to 20 boards. Which means you can't afford not to own one.

Free VHS demo.
Our videocassette demo shows all three BoardMaker models in action. Request on your letterhead or phone 415-883-1717. Or circle bingo card for more information. Instant Board Circuits, 20A Pamaron Way, Novato, CA 94949.

ibc
Instant Board Circuits

CIRCLE NO 137

See the IEEE, IEE & UMI experiment in *Distribution of Information on CD-ROM* at booth 1318

The Institute of Electrical and Electronics Engineers, Inc. (IEEE), the UK-based *Institution of Electrical Engineers (IEE)* and *University Microfilms International (UMI)* have created and are currently testing a CD-ROM image database system for IEEE and IEE publications issued from January 1988 onward. The aim of the program, called IEEE/IEE Publications Ondisc (IPO), is to serve the organizations' members better by making easily available a complete source of their publications. All 1988 IEEE and IEE journals, conference proceedings and magazines, plus a complete set of IEEE Standards will be stored on 25 to 30 discs — a total of 200,000 pages of text. 1989 material is being added as it is published.

Come to booth 1318 at WESCON '89 for a free demonstration of this exciting new experiment.

CIRCLE NO 135

and an IBM PC/AT-compatible plug-in board that can support four pods. The software is compatible with Xilinx's LCA design software. To use the verifier, you plug a probe into one of the target system's LCA sockets and insert an LCA like the one removed from the target into the pod. $9390. Delivery, four to six weeks ARO.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX 206-882-1043. TLX 152167. Booth No. 1437.

Circle No. 458

68030 ICE

The ERX in-circuit emulator for the 68030 μP also supports the 68882 coprocessor. In addition to emulation, the instrument performs real-time software performance analysis. The unit consists of an emulation module that plugs into the IBM PC/AT bus and a personality module that connects to the target system. Emulation memory is 256k-bytes deep and is expandable to 2M bytes. The trace buffer is 88 bits wide and 8k frames deep. You can set as many as 1M breakpoints. Supporting software permits both symbolic and high-level-language debugging. $15,995.

Zax Corp, 2572 White Rd, Irvine, CA 92714. Phone (800) 421-0982; in CA, (714) 474-1170. FAX 714-474-0159. Booth No. 1056.

Circle No. 459

C Cross-Compilers For NEC V25 And Intel 80386

InterTools, a well-established software cross-development system that runs on a wide variety of host computers, is now available for target systems based on Intel's 80386 μP or NEC's V25 μP. The package consists of an optimizing C cross-compiler; a manufacturer-compatible cross-assembler; the XDB 5.0 source-level cross-debugger; and a

Text continued on pg 180

National Semiconductor

Silence system noise with our new FACT Quiet Series.™

NATIONAL INTRODUCES THE FIRST INDUSTRY-STANDARD LOW-NOISE SOLUTION.

The ACMOS marketplace has been long seeking an industry-standard pin-out solution that comes with guaranteed noise specifications, as well as important characteristics designed to answer specific low-noise application requirements. FACT Quiet Series (QS) is precisely that solution. And just as you'd expect, it's available from the leader in ACMOS logic, National.

FACT QS addresses all components of system- and device-generated noise, and not merely V_{OLP}, or positive ground bounce. Those additional elements include V_{OLV} (undershoot) and ringing, dynamic noise margin, as well as crosstalk and EMI.

FACT QS 74ACTQ244 Specifications

	Typical	Max
V_{OLP}	1.0V	1.5V
V_{OLV}	−0.5V	−1.2V
V_{IHD^*}	1.8V	2.2V
V_{ILD^*}	1.4V	0.8V
Tskew	0.5ns	1.0ns
ESD	6,000V	4,000V min
Latchup	1.0A	300mA

*V_{IHD} – *Dynamic Input threshold high.*

*V_{ILD} – *Dynamic Input threshold low.*

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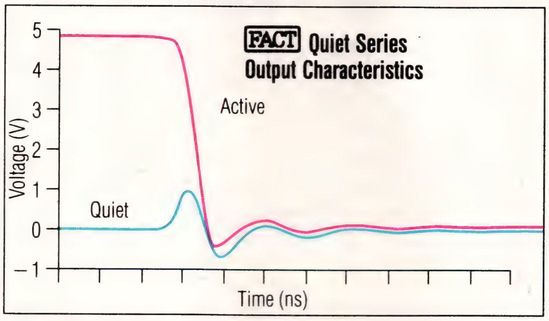
FACT (Fairchild Advanced CMOS Technology) Quiet Series (QS), FACT and GTO (graduated turn-on output) are trademarks of National Semiconductor Corporation.



Worst-case noise conditions, using industry-accepted test methodology.

QUIETER THAN ANYTHING ELSE.

FACT QS utilizes graduated turn-on circuitry (GTO™) to smooth the edges of the switching output. In addition, we've included an innovative undershoot corrector to prevent negative output excursions, which has the additional benefit of virtually eliminating device-generated ringing. The unique split-power bus design isolates the input from any output perturbations, which increases the input dynamic threshold and the resulting dynamic noise margin.

THE COMPLETE ASYNCHRONOUS SOLUTION.

For applications such as asynchronous line driving, FACT QS also provides performance benefits in addition to low noise, beginning with very tight output skew. With in-phase propagation delays used in clock distribution, typical skew is less than 500ps. In all cases, we guarantee that output skew will be less than 1ns. Furthermore, FACT QS also offers up to a 15% propagation delay improvement over standard FACT.

ALL IN THE FAMILY.

As the newest member of our growing FACT and FACT FCT family, FACT QS is available in all industry-standard packages, including PDIP and SO, as well as CDIP, Flatpak and LCC for military applications.

FACT QS vs. THE COMPETITION [Typical (+25°C, 5.0V)]

Parameter	1. National's FACT QS	2. Competitor A Center Pin ACL	3. Competitor B FCTA
V_{OLP}	1.0V	1.4V	3.0V
V_{OLV}	−0.5V	−1.5V	−1.6V
V_{IHD}	1.8V	2.3V	2.4V
V_{ILD}	1.4V	0.6V	0.4V

CALL AND FIND OUT MORE.

Give us a call today at **1-800-825-5805, ext. 108**, and arrange to get more information, plus a free sample. Or write: **National Semiconductor Corporation, P.O. Box 7643, Mount Prospect, IL 60056.** And discover how FACT QS can answer all your low-noise application needs.

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CIRCLE NO 136

Dry Desert to Wet World

Survival! That's what you can expect from OTTO precision snap-action pushbutton switches. Sealed to survive the rigors of industrial, commercial and military applications, these switches are available in momentary and alternate (push-on, push-off) action, miniature and subminiature sizes, choice of front panel appearance and button colors.

Sealed against dirt and water. Electrical ratings from computer level to 10 Amperes. Contact resistance <.025 ohms.

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CONTROLS Division, OTTO ENGINEERING, INC.
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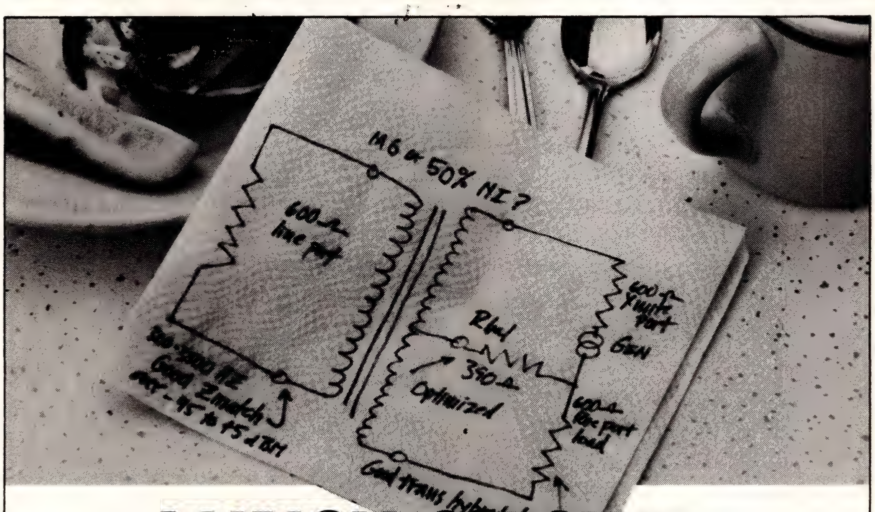
CIRCLE NO 134



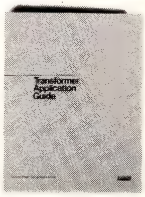
LUNCH CIRCUIT.

We know there's no special time for ideas. We also know that if your design involves transformers and/or inductors, we can help you make sure it's right. *Before* it gets to breadboard.

Meanwhile, you may want to read our free *Transformer Application Guide.* It's loaded with food for thought. Like how to determine VA rating. How to size rectifier circuits. How to estimate secondary RMS voltage. How to determine capacitor factors. And much more.

Simply write us at East Bridgewater, MA 02333. Or call 1-800-422-1107. In Massachusetts, call (508) 378-5260.

Bon Appetit!



Foxboro/Power Components Group

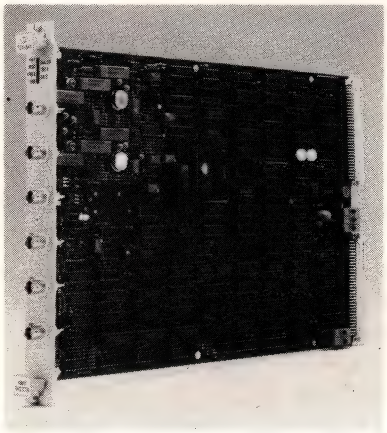
FOXBORO

CIRCLE NO 138

standard set of utility programs such as linker, librarian, locator, formatter, and ROM processor. The 80386 tools support that chip's protected mode, produce output in COFF format, and let you write interrupt handlers in C.

The global-optimizing phase of the compiler has been enhanced by strength reduction, a new type of optimization. The NEC V25 tools include many features (such as enhancements to the runtime libraries) that take specific advantage of on-chip peripherals and make it easy to write interrupt handlers. PC version of the compiler/assembler/utility package, from \$1800; PC version of XDB 5.0, from \$1500.

Intermetrics Inc, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-0072. FAX 617-868-2843. TWX 710-320-7523. Booth Nos. 849 and 851. **Circle No. 460**



VXIbus Counter

The 73A-541 single-width C-size VXIbus card performs measurements normally made by standalone universal counters. The unit can measure frequency, pulse width, period, time interval, and duty cycle. It can do so for single events, or it can compute averages over multiple-event occurrences. It can also count events. The board operates in an unconventional manner: It stores the absolute time of occurrences in a 28-bit × 2048-word

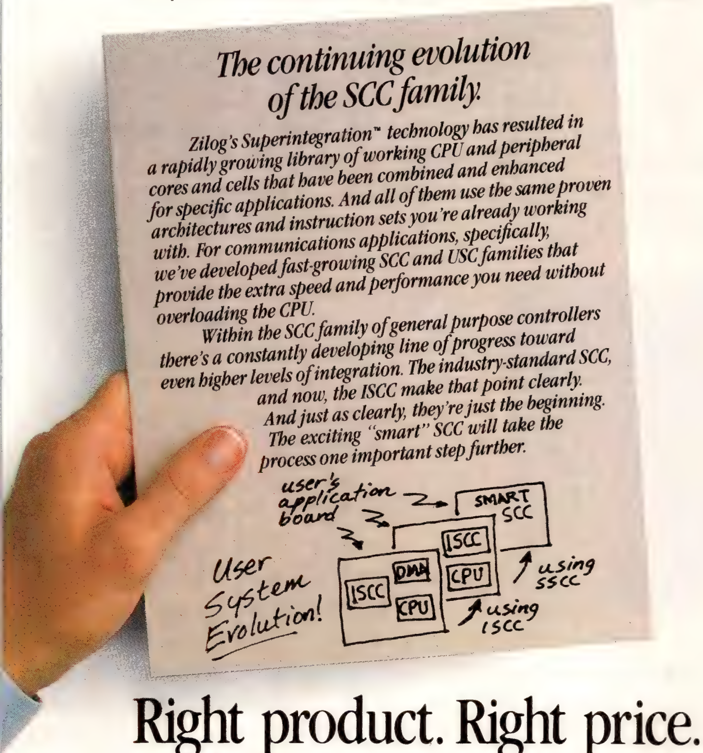
ZILOG

The integrated SCC that increases system performance and cuts CPU overhead in half. *Any* CPU.

The CMOS Integrated Serial Communications Controller (Z16C35™) adds another level of performance and integration to Zilog's industry-standard SCC. And it'll work with whatever CPU you're using.

You cut real estate dramatically.

The ISCC's four DMA controllers (two per SCC channel) can cut your bus overhead by 50%, compared to industry-standard controllers. The maximum bus bandwidth of 3.1 Mbytes/second reduces both bus utilization and CPU overhead.



The continuing evolution of the SCC family.

Zilog's Superintegration™ technology has resulted in a rapidly growing library of working CPU and peripheral cores and cells that have been combined and enhanced for specific applications. And all of them use the same proven architectures and instruction sets you're already working with. For communications applications, specifically, we've developed fast-growing SCC and USC families that provide the extra speed and performance you need without overloading the CPU.

Within the SCC family of general purpose controllers there's a constantly developing line of progress toward even higher levels of integration. The industry-standard SCC, and now, the ISCC make that point clearly. And just as clearly, they're just the beginning. The exciting "smart" SCC will take the process one important step further.

Since you've got a programmable bus interface, there's no need for programmable array logic on board. Plus you've got a more compact code to work with.

You pick the CPU.

The new streamlined, general purpose bus architecture is programmable in 8- or 16-bit data widths and 8-, 16- and 32-bit address bus widths. The ISCC's bus architecture is programmable to accept multiplexed or non-multiplexed formats.

You improve system performance.

Available in 10, 12.5 and 16 MHz versions, the ISCC will give you a data transfer rate of up to 4 Mbit/sec. You've also got a 10 x 19 bit status FIFO and a 14-bit byte counter for high speed SDLC transfer, using on-chip DMA controllers. Besides the low power CMOS and Superintegration™ advantages, you have performance enhancers like on-chip baud-rate generators, digital phased locked loops and crystal oscillators. And the ISCC supports all the current SCC features, including multiprotocol operation.

You choose.

The ISCC is designed for applications that don't require the higher bit rates of the USC, but do require DMA interface to larger memory systems as found in networked small computers, for example. In fact, it's the only integrated general purpose alternative available. It's also off the shelf. And backed by Zilog's proven quality and reliability. To find out more about the ISCC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.

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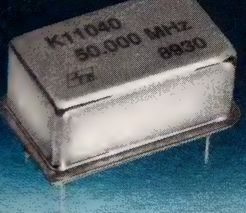
ZILOG SALES OFFICES: CA (408) 370-8120, (714) 838-7800, (818) 707-2160, **CO** (303) 494-2905, **FL** (813) 585-2533, **GA** (404) 923-8500, **IL** (312) 517-8080, **NH** (603) 888-8590, **MN** (612) 831-7611, **NJ** (201) 382-5700, **OH** (216) 447-1480, **PA** (215) 653-0230, **TX** (214) 987-9987, **CANADA** Toronto (416) 673-0634, **ENGLAND** Maidenhead (44) (628) 39200, **W. GERMANY** Munich (49) (89) 672045, **JAPAN** Tokyo (81) (3) 587-0528, **HONG KONG** Kowloon (852) (3) 723-8979, **KOREA** (82) (2) 552-5401, **TAIWAN** (886) (2) 741-3125, **SINGAPORE** 65-235 7155, **DISTRIBUTORS: U.S.** Anthem Electronics, Hall-Mark Electronics, JAN Devices, Inc., Schweber Electronics, Vargas Electronics, Western Microtechnology, **CANADA** Future Electronics, SEMAD, **LATIN AMERICA** Argentina—Yel.-(1) 46-2211, Brazil—Digibyte (011) 581-1945.

CIRCLE NO 139

Drives MC68040, MC68030 at 50 MHz



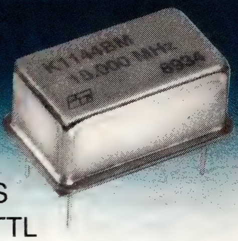
K11040 Series

- 40 MHz to 70 MHz
- TTL Compatible; CMOS Compatible with 50 pF Load Capability
- Min/Max Symmetry 47.5/52.5% for Tightly Controlled Duty Cycle
- Rise Time 1.7 ns, Fall Time 1.6 ns Max

Cooperatively designed to drive the Motorola MC68030 and MC68040 families of 32-bit microprocessors, the K11040 Clock Driver is also ideal for other applications requiring tightly controlled duty cycle and very fast rise and fall times with 50 pF load capability. Consult factory for additional frequencies.

CIRCLE NO 143

±20 PPM Clock For Telecom Applications



K1144 Series

- 1.5 - 35 MHz TTL or CMOS
- 35 - 60 MHz TTL
- +5V dc Input

For telecommunications, modems, and other applications requiring tight stability, the K1144BM provides ±20 ppm stability, uses standard +5V dc input, drives standard TTL and CMOS logic, fan out of 10 from 1.5 to 35 MHz. Model K1144AM drives up to 5 TTL logic gates from 35 to 60 MHz. Tighter stabilities available.

CIRCLE NO 144

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Champion
Technologies, Inc.

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Franklin Park, IL 60131 U.S.A.
708/451-1000 FAX: 708/451-7585
EasyLink: 62931824 Telex: 499-0104 CTI UD

memory and processes this data to obtain the needed results. Many types of results are available in real-time while the unit is making additional measurements. The unit can accept inputs from front-panel connectors or from the VXIbus's TTLTRG lines. There are several built-in self-test functions. $2295. Delivery, 12 to 16 weeks ARO.

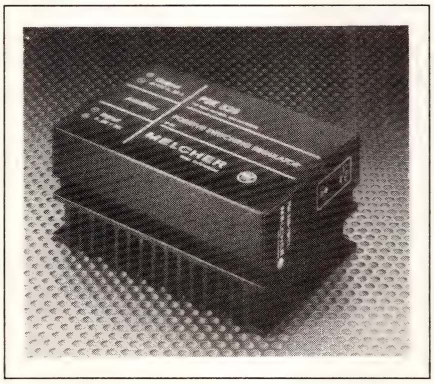
Colorado Data Systems Inc, 3301 W Hampden, Englewood, CO 80110. Phone (800) 237-2831; in CO, (303) 762-1640. TWX 910-933-0193. Booth No. 932.

Circle No. 461

Switching Regulators

Units in the PSK Series of dc/dc switching regulators provide single outputs of 5, 12, 24, and 36V in 16 and 20A (25A for 5V models) versions. The devices have input ranges as wide as 8 to 80V dc and efficiencies ranging from 82 to 94%.

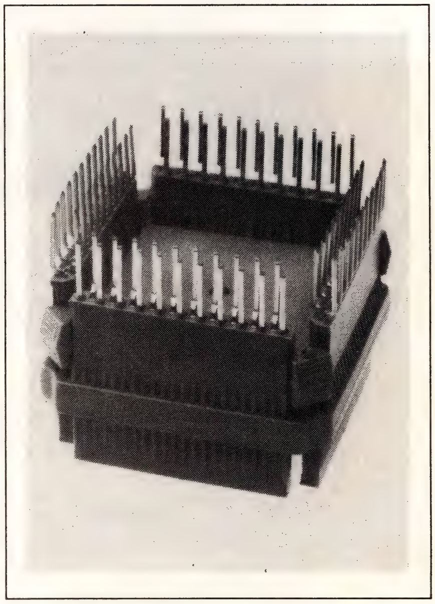
PSK regulators operate over a −25 to +71°C range. Line and load regulation equals ±0.3%; output ripple is 100 mV p-p max. Standard features include remote on/off, output voltage adjustability (0 to 100%), input filtering, remote sense, load-current sharing, and temperature surveillance. Available options include in-rush current limiting and output crowbar.



Mechanically, PSK regulators are suitable for single-height-Eurocard or chassis mounting. Electrical connections are made via a standard H15 pin connector for 16A units and an H15/4H connector with 4 high-current pins for 20 and 25A modules. $300 (100). Delivery, eight to 10 weeks ARO.

Melcher Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-4715. FAX 508-879-8669. Booth No. 5618.

Circle No. 462



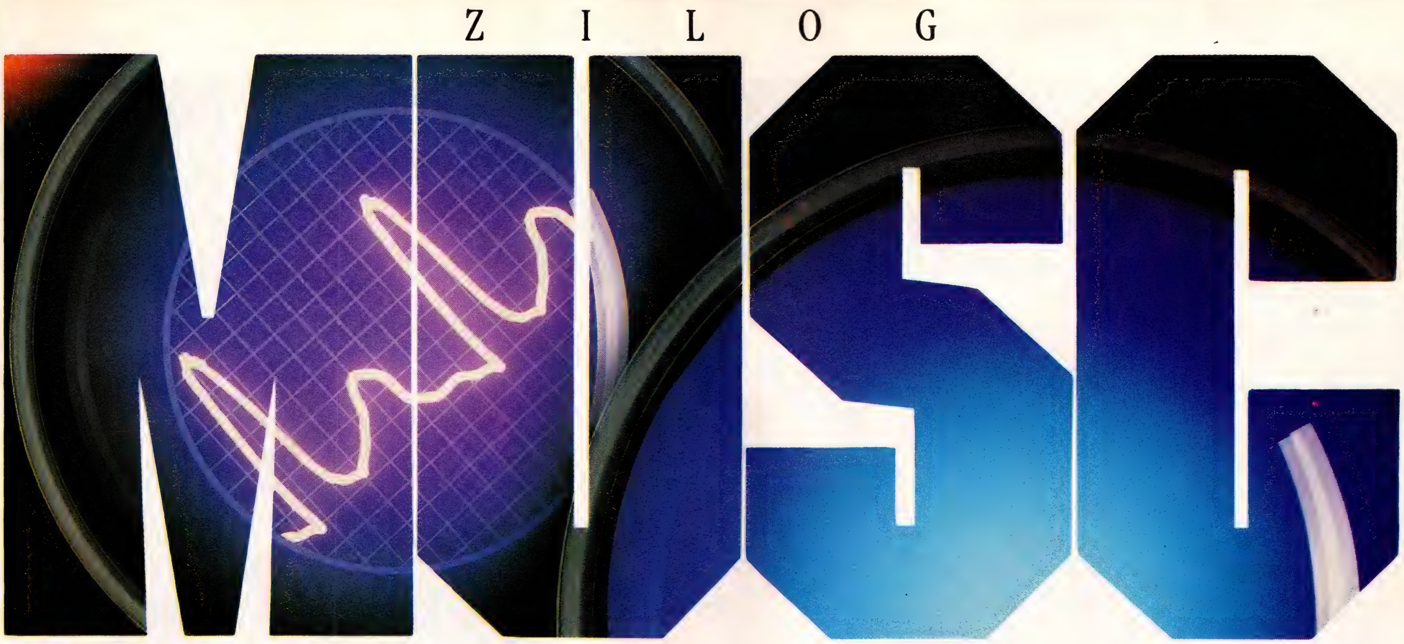
Test Adapter

Model 5402 is designed to test 84-lead chip carriers (LCC or PLCC) with J-lead contacts. The adapter design features a patented snap-ring design, which provides springless actuation. In use, the adapter mounts directly onto the IC under test and locks securely into position to provide hands-free testing. Output signals are delivered by 0.025-in. square, gold-plated phosphor bronze pins, which are staggered to maximize test-lead access. Model 5402 has a 500V rms rating and will carry current level ranging to 1A. Operating temperature rating measures 102°C. The Model 5402 adapter features beryllium copper interface contacts and glass-filled nylon insulation. $44.50.

ITT Pomona Electronics, Box 2767, Pomona, CA 91769. Phone (714) 623-3463. Booth Nos. 1742 and 1744.

Circle No. 463

Text continued on pg 186



Now you can build 10 Mbit high-performance into your single-channel designs.

Zilog's MUSC, mono-channel universal serial communications controller (Z16C33™), has been designed specifically for high-performance applications that require only one high-speed channel. And it costs you about 40% less than the dual-channel USC.

All the performance you want.

The MUSC's 10 Mbit/sec data transfer rate makes it the fastest single-channel general purpose controller available. CMOS and Superintegration™ give you higher throughput, while helping reduce the CPU workload. And the 32-byte FIFO transmit-and-receive buffers help reduce CPU overhead. So does the fact that the MUSC integrates two time slot assignment cells—one for receive and one for transmit. So data is automatically inserted into programmed time slots, reducing CPU overhead and external logic even more. And all of that frees up more CPU power for the system. The final touch is a separate 8-bit parallel I/O port, ideal for status or displays, that adds flexibility in local control or data presentation.

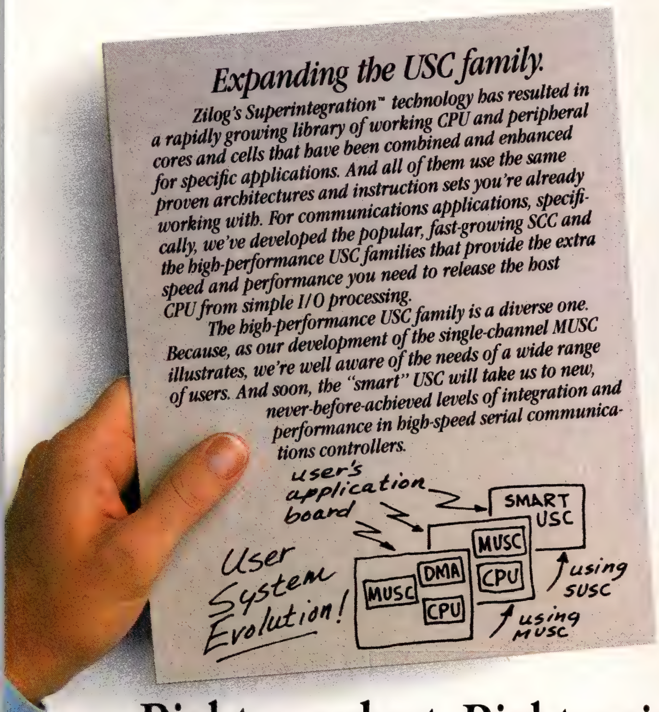
All the flexibility you need.

The MUSC's multiprotocol design lets you adapt your system to a variety of networks. But not only do you get 10 protocols, you get 8 encoding formats—including asynchronous, bit and byte synchronous, isochronous, Ethernet, and MIL-STD 1553B. And the Open Systems Interconnect (OSI) model features Time Slot Assignment that allows transmission of time multiplexed Synchronous Data Link Control (SDLC) protocol to the ISDN link level.

All the reliability you've come to expect.

Of course, the MUSC comes to you off the shelf, with Zilog's proven quality and reliability. And you have the advantage of CMOS and Superintegration. But you also have the MUSC's unique built-in bus-oriented testability, which allows access to nodes and registers for testing program functionality in real time. And, since dedicated pointer registers provide a window to serial flow during on-line testing, you can test transmission reliability of the controller during system operation.

To find out more about the MUSC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.



Expanding the USC family.

Zilog's Superintegration™ technology has resulted in a rapidly growing library of working CPU and peripheral cores and cells that have been combined and enhanced for specific applications. And all of them use the same proven architectures and instruction sets you're already working with. For communications applications, specifically, we've developed the popular, fast-growing SCC and the high-performance USC families that provide the extra speed and performance you need to release the host CPU from simple I/O processing.

The high-performance USC family is a diverse one. Because, as our development of the single-channel MUSC illustrates, we're well aware of the needs of a wide range of users. And soon, the "smart" USC will take us to new, never-before-achieved levels of integration and performance in high-speed serial communications controllers.

Right product. Right price. Right away.

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ZILOG SALES OFFICES: CA (408) 370-8120, (714) 838-7800, (818) 707-2160, **CO** (303) 494-2905, **FL** (813) 585-2533, **GA** (404) 923-8500, **IL** (312) 517-8080, **NH** (603) 888-8590, **MN** (612) 831-7611, **NJ** (201) 382-5700, **OH** (216) 447-1480, **PA** (215) 653-0230, **TX** (214) 987-9987, **CANADA** Toronto (416) 673-0634, **ENGLAND** Maidenhead (44) (628) 39200, **W. GERMANY** Munich (49) (89) 672045, **JAPAN** Tokyo (81) (3) 587-0528, **HONG KONG** Kowloon (852) (3) 723-8979, **KOREA** (82) (2) 552-5401, **TAIWAN** (886) (2) 741-3125, **SINGAPORE** 65-235 7155, **DISTRIBUTORS: U.S.** Anthem Electronics, Hall-Mark Electronics, JAN Devices, Inc., Schweber Electronics, Vargas Electronics, Western Microtechnology, **CANADA** Future Electronics, SEMAD, **LATIN AMERICA** Argentina—Yel.-(1) 46-2211, Brazil—Digibyte (011) 581-1945.

CIRCLE NO 140

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Look who's talking to IBM now– with a single chip.

THE DP8344 BCP OPENS UP THE IBM WORLD.

Because of this one little device, a lot of players have found effective new ways of getting into the Big Blue game. Among them are Apple, Digital Equipment Corporation, and many others emerging as winners in IBM protocol design and development.

The DP8344 Biphase Communications Processor (BCP) is the key component in Apple's new adapter card for the Macintosh II—a landmark beginning in Apple's strategy of integration into the IBM mainframe environment.

The BCP is also a key component in Digital's new 3270 Terminal Option Card for the DECserver 550, which gives IBM 3270 displays full-screen VT220 access to VAX applications. Users can simply "hot-key" from their IBM system to Digital's program development environment, industry-leading ALL-IN-1, and world-class UNIX.

Besides putting new players in the game, the BCP gives existing plug-compatible players—like Memorex Telex—big competitive advantages.

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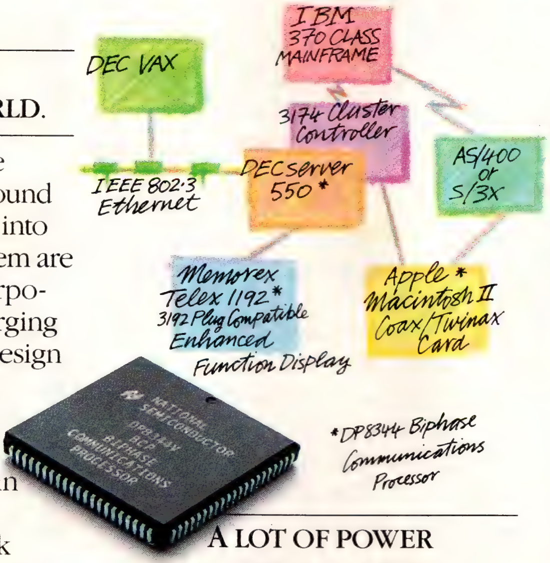

A LOT OF POWER IN A VERY SMALL SPACE.

An intelligent transceiver and high-performance CPU are integrated on the same low-power CMOS chip. So a full system supporting all three IBM protocols—3270, 3299 and 5250—can be implemented in an area the size of a credit card.

Yet the DP8344 BCP's RISC architecture is so powerful that it's the only processor needed in the new Memorex Telex 1192 Enhanced Function Display Terminal Series. Memorex Telex was able to cut both power consumption and board space—while adding a lot of new features, like an on-screen calculator and adjustable cursor-movement rates.

The BCP also enables Digital to maintain both its own and IBM sessions for four terminals with a single chip. And Apple can implement IBM coax and twinax protocols with the same hardware platform and two-line interfaces.

WE'LL GIVE YOU ALL THE SUPPORT YOU NEED.

Our system solution includes a Multi-Protocol Adapter Demonstration System for 3270/3299/5250 connectivity. It supports all popular terminal-emulation and file-transfer software.

We also offer the BCP PocketLink, a credit-card-size terminal emulator; a demonstration/development system with monitor debugger; and the DP8344 assembler/linker/librarian system.

LET'S TALK.

If you want your system to talk to IBM, you should first talk to National. Give us a call today at (800) 825-5805, ext. 103.

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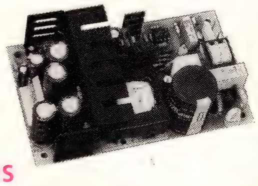
40 WATT
SWITCHERS



FEATURES
- Universal input voltage range 85-265 VAC
- 0% Minimum load on all outputs
- Approved UL, CSA and TUV standards
- Onboard VDE Class "B" line filter which exceeds the requirement by 10dB margin
- Indefinite short circuit protection
- Overvoltage protection
- Minimum 205,000 hours M.T.B.F.
- 3″ × 5″ × 1.5″

MODEL NUMBER	OUTPUT VOLTAGE/CURRENT
FLU3-40-1AD	5V@5A, +12V@3A (5A Pk), −12V@0.7A

Eight models are available with voltage combinations of +5, −5, +12, −12, +15, −15, +24 & +28 VDC.

PRICE & DELIVERY
- $79 for singles and $63.50 each for 100 quantity, (For FLU3-40 Series)
- Delivery-Stock to 2 weeks

POWER GENERAL'S FLU2-40 and FLU3-40 series are families of dual and triple output 40 watt switching power supplies for Disk drive subsystems, Data communications, CRT terminals, Industrial equipment and Instrumentations.

These products are machine inserted, auto-tested and monitored under statistical process control on our JIT production line.

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CIRCLE NO 142

Products

LCD Switch Module

The Pixie module integrates a low-power LCD and a custom IC driver into the keycap of an spst momentary-contact switch to provide a user-friendly method for machine control and display applications. The LCD employs super-twist technology and features LED-type backlighting to accommodate low-ambient lighting conditions.

The LCD consists of 864 pixels in a 24×36-pixel matrix that provides full-screen graphics displays. You can also configure the Pixie's display in a 5×7 dot matrix to obtain a 3-line×6-character alphanumeric presentation.

The spst switch contacts have a nominal rating of 12V at 50 mA. Contact withstanding voltage rating is 250V ac for 1 minute. Contact and isolation resistance are 1Ω max and $50\times10^6\Omega$ min, respectively. Switch bounce measures 5 msec max. $40.72 (100).

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. FAX 818-376-1075. Booth No. 2331. **Circle No. 464**

Clock Oscillators

MX055L Series TTL-compatible clock oscillators are available in 26 standard versions covering a frequency range of 2.4576 to 64 MHz. Custom frequencies within this range are also available. All oscillators will drive 10 standard TTL loads.

Housed in a hermetically sealed metal package that's compatible with 14-pin DIPs, MX055L oscillators employ a 3-point/120° crystal mount, which maximizes shock and vibration performance. They feature a +100-ppm frequency stability over an operating range of 0 to 70°C. Optional stabilities of ±25 to ±1000 ppm are also available.

MX055L oscillators also feature enable/disable and complementary output options. They operate from 5V supplies and draw currents

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CIRCLE NO 290

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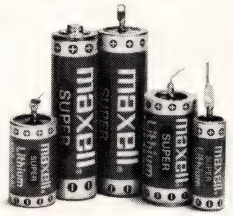
*Recognized under the Component Program of Underwriters Laboratories.

See us at WESCON, Booth #5303

CIRCLE NO 145



ranging from 20 to 35 mA. Rise and fall times for the 50% duty-cycle output range from 2 to 4 nsec typ. $2.25 (1000).

CTS Corp, 400 Reimann Ave, Sandwich, IL 60548. Phone (815) 786-8411. FAX 815-786-9743. Booth No. 2104. **Circle No. 465**

Binary-Coded Rotary Switches

Measuring only 0.5 in. in diameter, Series 26 binary-coded rotary switches have 16 positions and are rated for 25,000 cycles of operation when switching logic-level loads. They do, however, have an adjustable stop feature that allows users to create a 10-position BCD-code output or an 8-position octal-code output.

By adjusting the location of the stops on the Series 26 switches, you can isolate any portion of the standard binary code and use that portion as the output. All switches are supplied with seals at the front of their housings.

At end of life, contact resistance for Series 26 switches will equal 500 mΩ. Dielectric strength equals 250V ac min, and minimum insulation resistance measures $10^9\Omega$. All switches are supplied with five terminals regardless of the number of active positions. $6.52 (100). Delivery, four to six weeks ARO.

Grayhill Inc, Box 10373, La Grange, IL 60525. Phone (312) 354-1040. FAX 312-354-2820. TLX 6871375. Booth No. 1731.

Circle No. 466

Chip Carriers

The SPC family of PLCC sockets conforms to EIA specifications for JEDEC PLCC Type A devices with J-style leads. They change 0.05-in. contact centers on the chip carriers to standard pc-board 0.100-in. spacings.

The sockets feature a closed bottom that prevents solder wicking or bridging. Built-in dual polarization prevents incorrect chip-carrier orientation during insertion. SPC2 devices can operate to 220°C. Both SPC and SPC2 units are available in 20-, 28-, 32-, 44-, 52-, 68-, 84-, and 100-contact sizes.

The SPC sockets also provide glass-filled polyester insulators and phosphor bronze contacts with tin over nickel plating. SPC2 units operate over a −55 to +220°C range and are constructed with 94V-0 UL-rated polyphenylene sulfide insulators. All devices are recognized by the UL listing program. SPC Series, $0.048/contact position; SPC2

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- Alpha-numeric displays for numbers and letters
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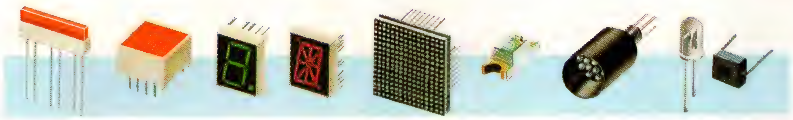
- Chip type LEDs for ultracompact, high-density mounting
- LOD series for signboard application
- Infrared LEDs for ultra high power



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CIRCLE NO 146

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105° C Rated Storage Capacitors

EMI Tested to FCC 20780 Class B & VDE 0871 Class B

Less Than 500 μA Leakage Current

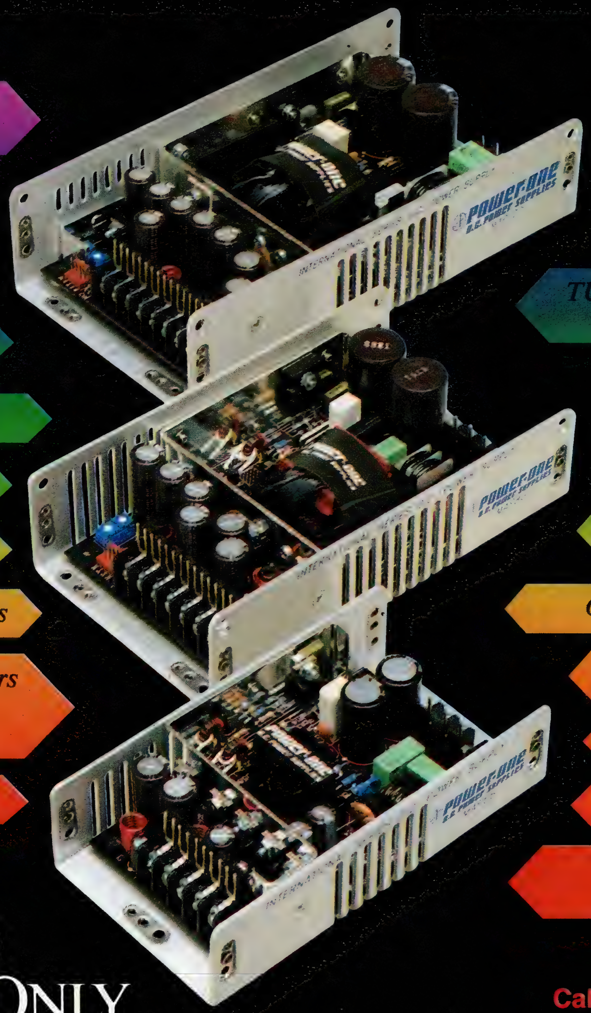
Rugged Wrap-Around Chassis

Thermal Shutdown with Warning

Platinum Barrier Schottky Rectifiers

Universal Terminal Block Connectors Include Both Locking Wafer Style Connectors & 6-32 Wire Clamps

75% Typical Efficiency



Universal Mounting System Provides .170 thru Holes, 6-32 Threads & M4 Metric Threads

30 Msec Typical Hold-Up Time

TÜV Certified to VDE 0806, IEC 380, IEC 950 & EN60950

All DC Outputs Fully Regulated

UL Recognized, CSA Certified

High Power Density, Up to 2.2 Watts/Cubic Inch

Outstanding Application Flexibility

100% Test, Inspection & Burn-In

Power-Fail Warning Signal

MOSFET Switching Technology

3750 VRMS Isolation Plus VDE Safety Spacings

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MODEL	POWER	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4
MAP55-4000	55W/65W PK	5V @ 6A	12V @ 3A/4A PK	– 12V @ 1A	– 5V @ 1A
MAP55-4001		5V @ 6A	12V @ 1A	– 12V @ 1A	24V @ 1.5A
MAP55-4002		5V @ 6A	12V @ 3A/4A PK	12V @ 1A	– 12V @ 1A
MAP80-4000	80W/110W PK	5V @ 14A	12V @ 4A/7A PK	– 12V @ 1A	– 5V @ 1A
MAP80-4001		5V @ 14A	12V @ 1A	– 12V @ 1A	24V @ 2A
MAP80-4002		5V @ 14A	12V @ 4A/7A PK	12V @ 1A	– 12V @ 1A
MAP130-4000	130W/165W PK	5V @ 20A	12V @ 5A/8A PK	– 12V @ 1A	– 5V @ 1A
MAP130-4001		5V @ 20A	12V @ 1A	– 12V @ 1A	24V @ 3.5A
MAP130-4002		5V @ 20A	12V @ 5A/8A PK	12V @ 1A	– 12V @ 1A

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CIRCLE NO 147

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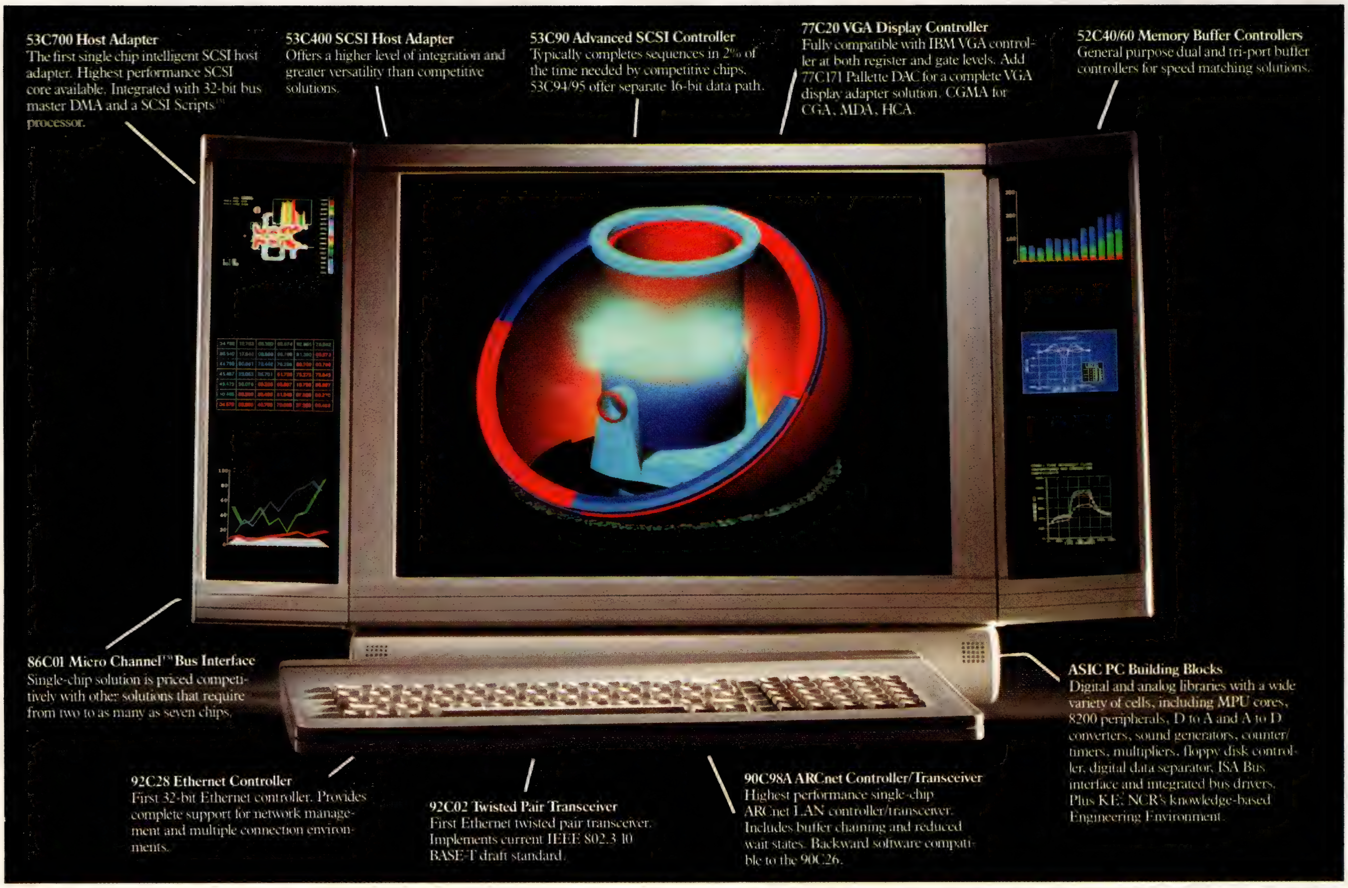

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53C400 SCSI Host Adapter
Offers a higher level of integration and greater versatility than competitive solutions.

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Typically completes sequences in 2% of the time needed by competitive chips. 53C94/95 offer separate 16-bit data path.

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Fully compatible with IBM VGA controller at both register and gate levels. Add 77C171 Pallette DAC for a complete VGA display adapter solution. CGMA for CGA, MDA, HCA.

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Single-chip solution is priced competitively with other solutions that require from two to as many as seven chips.

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Creating value

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CIRCLE NO 148

Series, $0.052/contact position (1000).

Circuit Assembly Corp, 18 Thomas St, Irvine, CA 92718. Phone (714) 855-7887. Booth No. 2433.
Circle No. 467

TO-5-Style Thermostats

The SD Series includes 30 snap-action thermostats, which are designed for use on pc boards. The hermetically sealed devices can withstand wave soldering and all board-cleaning operations. The alloy crosspoint switch contacts, designed to switch logic-level circuitry, are operated by a snap-action bimetallic disk. The SD line includes both open-on-temperature-rise and close-on-temperature-rise versions. Both groups operate to a ±5° tolerance in 5° increments over 40 to 120°C.

Operational life for the SD Series thermostats is 10,000 cycles at 1A or 100,000 cycles at 100 mA. Dielectric strength measures 500V ac rms at 60 Hz for 1 second. Contact resistance equals 100 mΩ max and operating range spans −50 to +150°C. The thermostats require no external power source. $5 (500).

Warren G-V, 1 Apollo Dr, Whippany, NJ 07981. Phone (201) 368-1200. Booth No. 1125.
Circle No. 468

Pin-Grid-Array Sockets

These low-insertion-force (LIF) pin-grid-array (PGA) sockets are available in sizes ranging from 10×10 through 16×16 positions. The insulators come in three versions—fully populated, custom populated, and center relieved.

These PGA sockets feature top-side standoffs, which prevent IC overinsertion and maximize air flow and power dissipation. Tapered entry holes make pin alignment easy and virtually error free. Staggered contact mating points, combined with a special plastic preload design, ensures consistent insertion and normal forces. The closed bottom contact design acts as an antiwicking solder ledge.

The devices feature beryllium copper contacts with selective 30-µin. gold plating in the contact area and tin plating on the solder tail. The insulator is molded from a high-temperature thermoplastic, which will withstand vapor phase and IR soldering process temperatures. From $3.50 (1000).

Thomas & Betts Corp, 1001 Frontier Rd, Bridgewater, NJ 08807. Phone (201) 685-1600. Booth No. 1848. **Circle No. 469**

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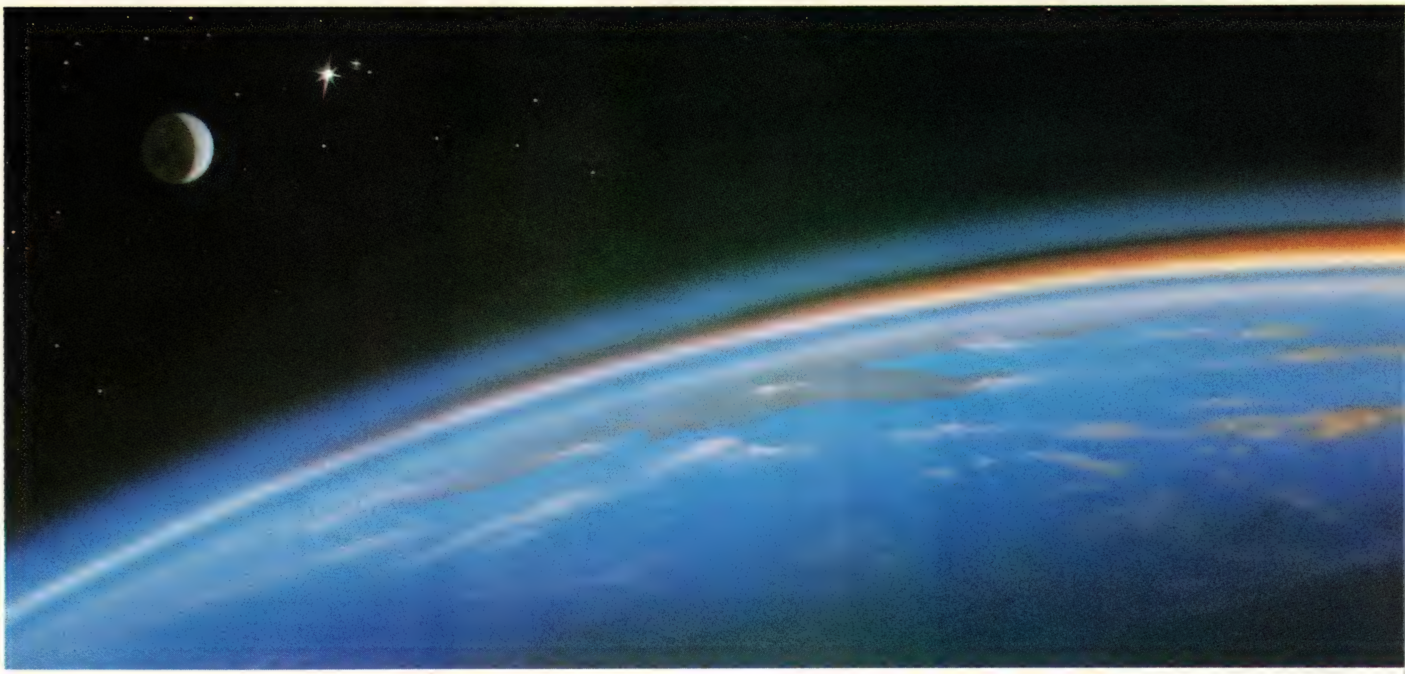
CIRCLE NO 149

SIEMENS



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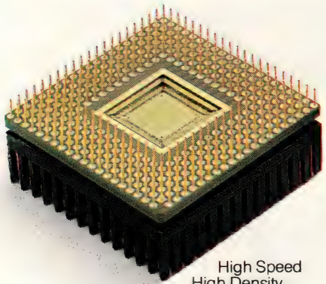

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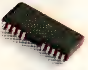

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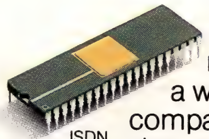
DRAM



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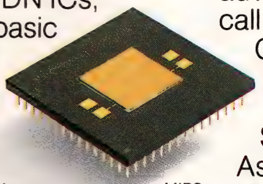

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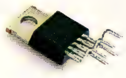

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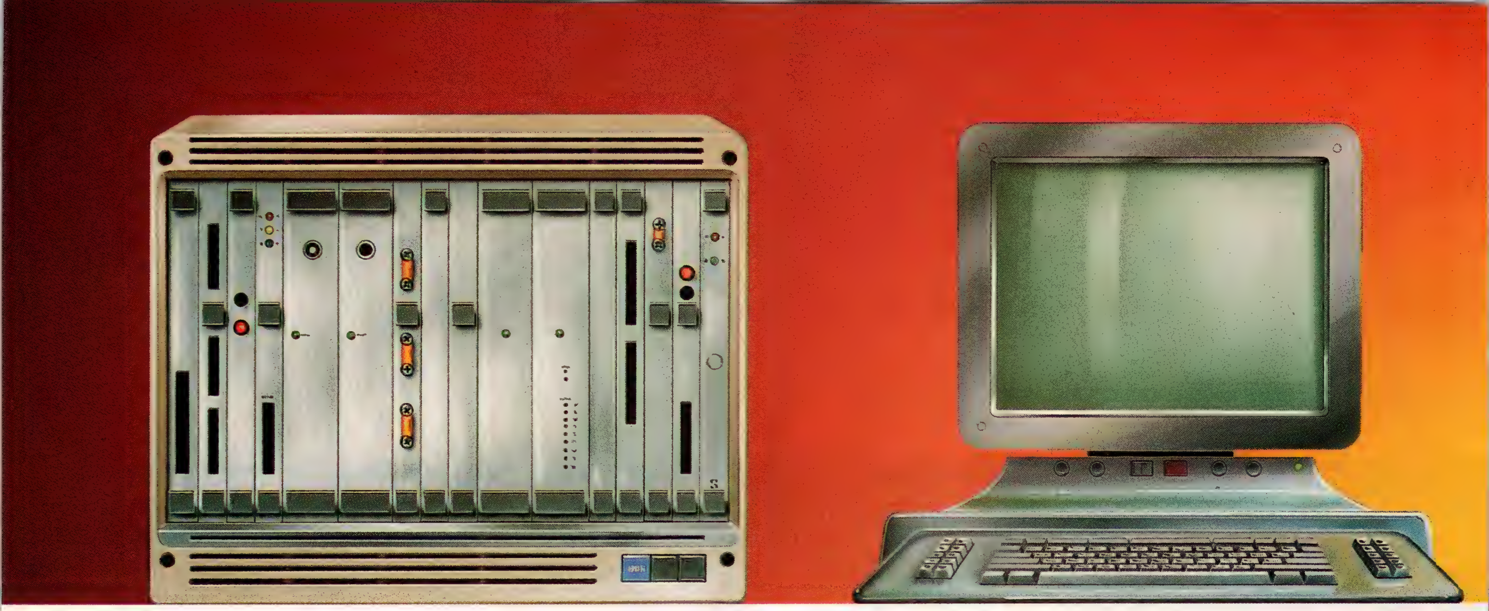

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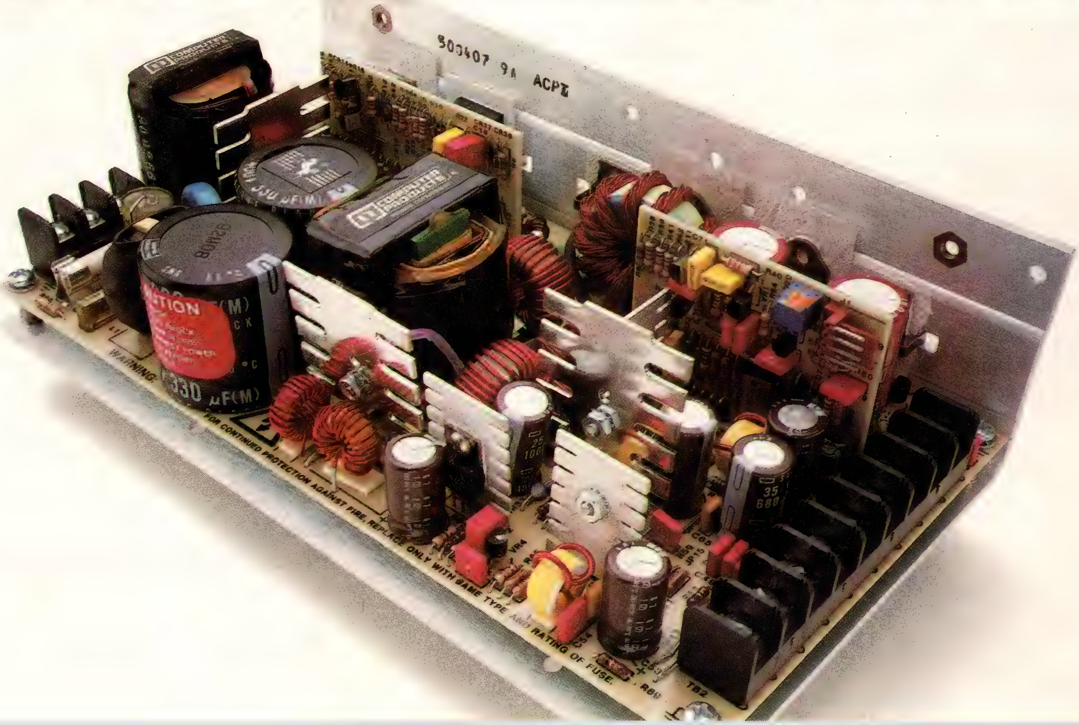

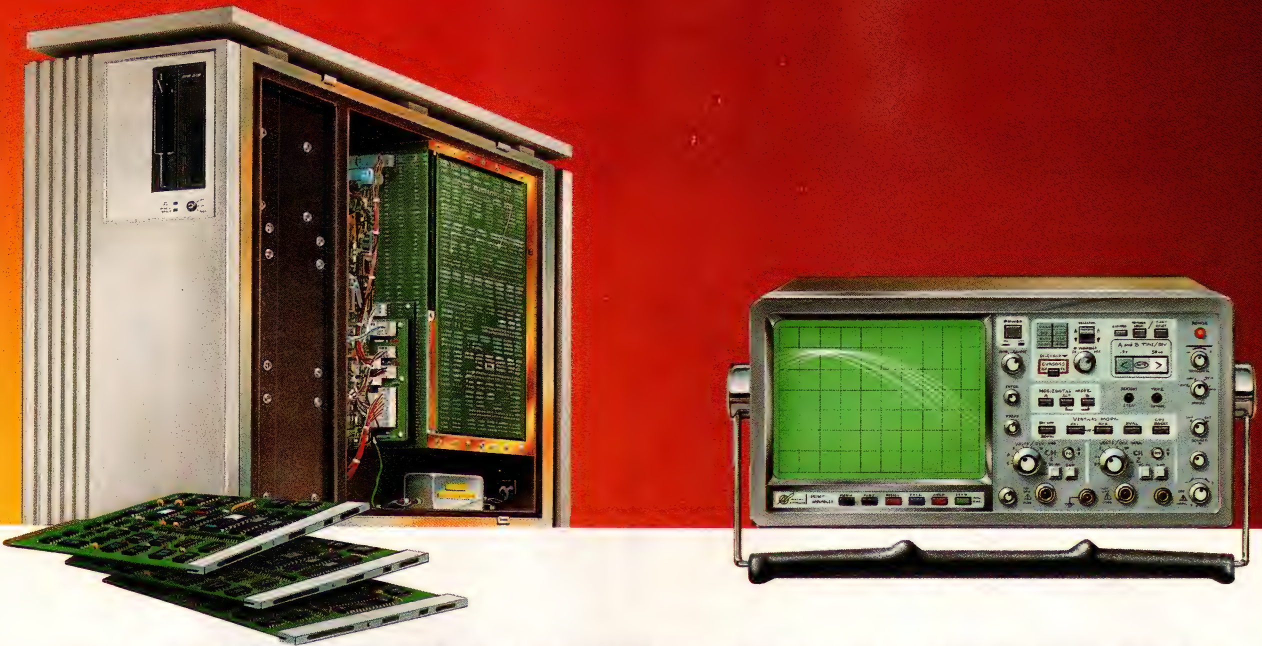

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NFS200 is the newest in our extensive line of universal input switchers, ranging from 25 to 600 watts. It's a natural addition to our growing family of both AC/DC and DC/DC power supplies. Computer Products. Now, more than ever *the power behind the products.*

MODEL	WATTS	W/AIR	NUMBER OF OUTPUTS
NFS25	25	25	1 Dual, 2 Triples
NFS40	40	50	4 Singles, 4 Triples
NFS42	40	40	3 Triples
NFS50	50	60	1 Triple
NFS110	80	110	4 Singles, 3 Quads
NFS200	—	200	1 Triple, 3 Quads
NFS350	—	350	1 Triple, 2 Quads
*NFS600	—	600	1 Triple, 3 Quads

*To Be Announced

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CIRCLE NO 151

SOLUTIONS IN PERFECT PROPORTION

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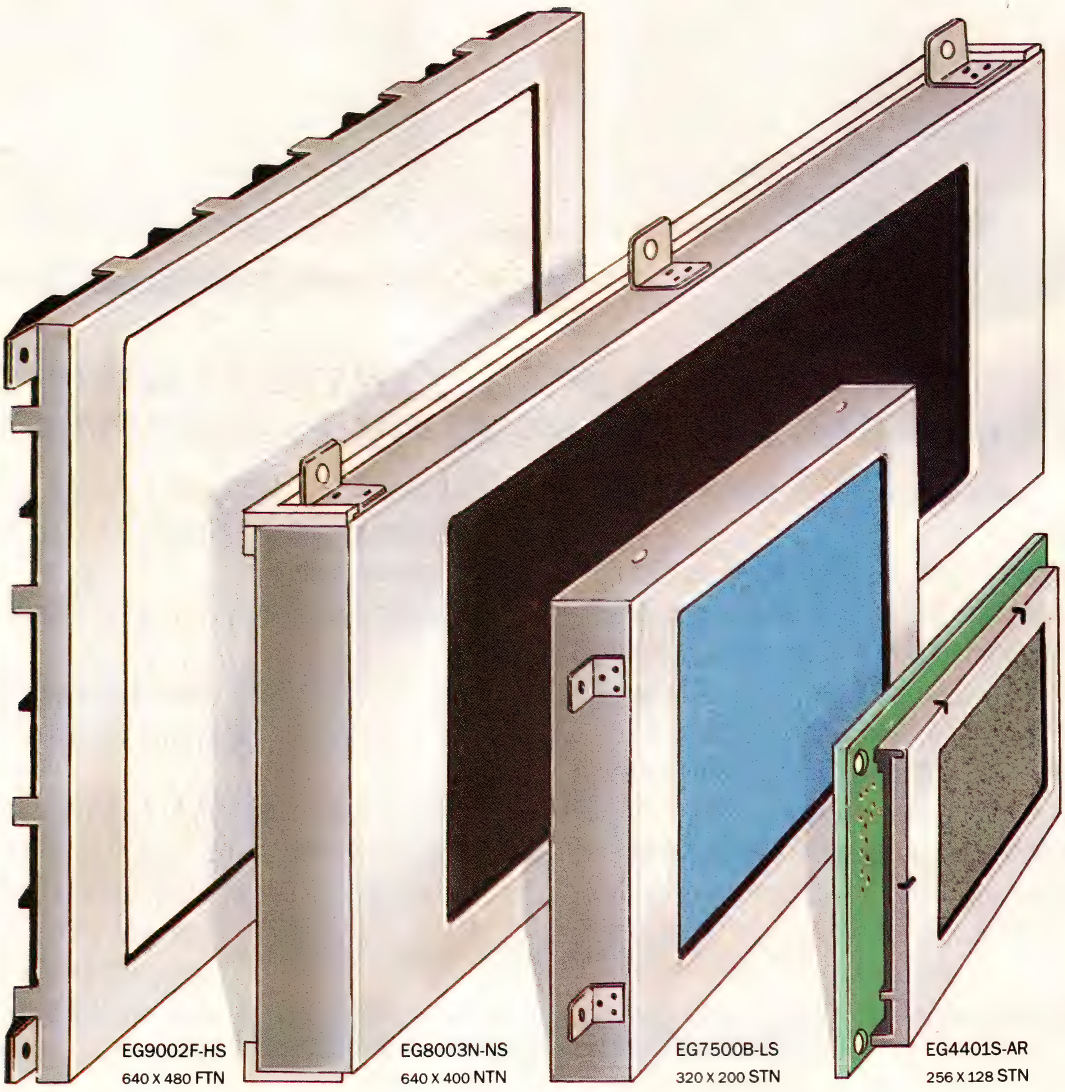

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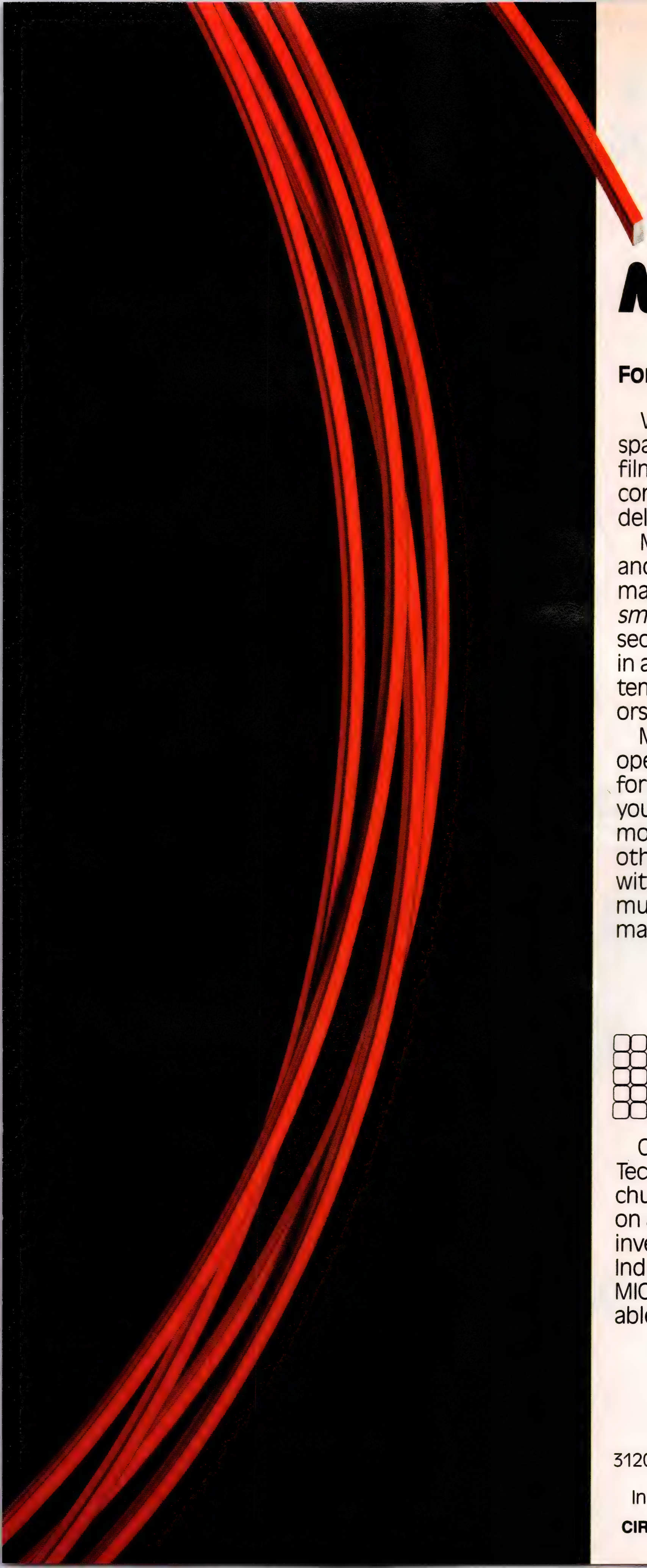

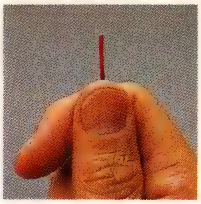

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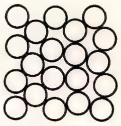

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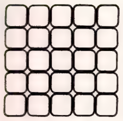

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DESIGNER'S GUIDE

Resonant-Mode Power Supplies Part 1

Resonant-mode design techniques improve switcher performance

Resonant-mode design techniques are becoming increasingly attractive to power-supply designers because they lead to fewer switching losses and allow you to use smaller components. Part 1 of this 2-part article reviews the classifications and circuits of the various resonant-mode topologies. Then, a 5V-power-supply design example illustrates the waveforms and control requirements of a typical resonant-mode design. Part 2 will detail the design of the control loop, resonant tank, and transformer.

Frederick E Sykes, *Gennum Corp*

One of the advantages of resonant-mode power supplies is that they can operate at higher switching frequencies than PWM designs, allowing you to use smaller transformer and output-filter components. In addition, resonant mode's use of sine-wave current and voltages reduces switching losses, EMI, and component stresses. Further, the availability of dedicated, resonant-mode control ICs makes it easier to implement a resonant-mode design.

This article discusses the most common types of resonant-mode supplies, which contain the central components of PWM designs along with two additional components: a resonant inductor and resonant capacitor (**Fig 1**). Recently, these types of resonant-mode converters have been called "quasiresonant." The resonant-mode technique uses this inductor and capacitor, which comprise a resonant tank, to achieve lossless switching by shaping the transformer's voltage and current. In PWM designs, the power switches are directly tied to their transformers, but in resonant-mode designs, the resonant tank sinusoidally shapes the transformer's input signal.

Another difference between PWM and resonant mode is in the regulation method. PWM designs regulate their outputs by fixing the control frequency and varying the on time of the power switches. Resonant-mode designs achieve regulation by varying the switching frequency and fixing the power switches' on or off times.

The first major advantage of resonant mode comes from its sine-wave switching waveforms. In PWM, the switches turn off at high-current and high-voltage points. Thus, the PWM design's switch must dissipate a large amount of power during the switching transition. In contrast, resonant-mode techniques turn off their switches at either zero-current or zero-voltage points in the sinusoidal waveform; at either a zero-current or zero-voltage point, the switch's power equals zero. Therefore, the switching losses of resonant mode are much smaller than those of PWM designs. Resonant-mode designs also reduce switching stress on components because of reduced power-dissipation requirements. Further, resonant-mode techniques lead to reduced EMI and RFI, unlike PWM methods, because the fixed inductor and capacitor values of the

The term "resonant mode" doesn't refer to any particular power-supply topology, but rather to a whole class of topologies.

resonant tank generate only one, fixed-frequency sine wave that has greatly reduced harmonics.

Other benefits of resonant-mode techniques stem from their higher operating frequencies. The switching losses inherent to PWM designs allow practical switching frequencies of 400 or 500 kHz. The low-loss benefits of resonant-mode techniques start at switching frequencies of approximately 200 kHz and still apply at frequencies as high as 10 MHz, depending on the resonant-mode supply's topology. Zero-current and zero-voltage switching topologies have practical upper-frequency limits of 1 to 2 MHz and 5 to 10 MHz, respectively. Zero-voltage switching is effective at higher frequencies than zero-current switching because it produces less high-frequency switching losses. These higher switching frequencies result in smaller transformer and output-filter components and reduced output ripple. Also, the supply's transient response can be much faster than that of PWM because the feedback-loop bandwidth can be much wider. These features are particularly important if you're designing equipment for distributed-power systems. These systems generally require smaller, card-mountable power supplies that feature medium power—50 to 200W—in a low-profile, lightweight, low-EMI package.

The term "resonant mode" doesn't refer to any particular power-supply topology, but rather to a whole class of topologies (**Ref 1**). These topologies divide logically into related groups, as shown in **Fig 2**. This classification doesn't imply that rigid barriers exist between the various topologies; it simply points out how the various topologies originated. Because of the rapid de-

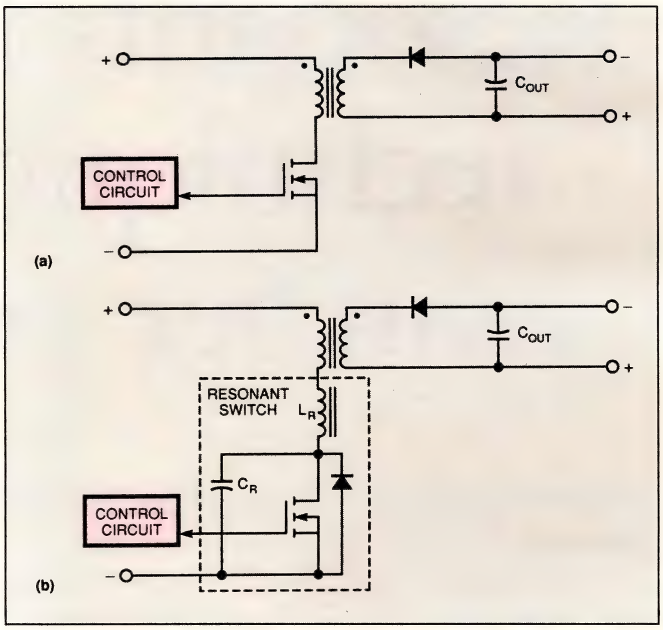

***Fig 1—Resonant-mode circuits differ from PWM** because of the presence of two resonant components—an inductor and a capacitor. By adding C_R and L_R, you can convert the PWM half-bridge configuration shown in **a** to a resonant-mode design (**b**).*

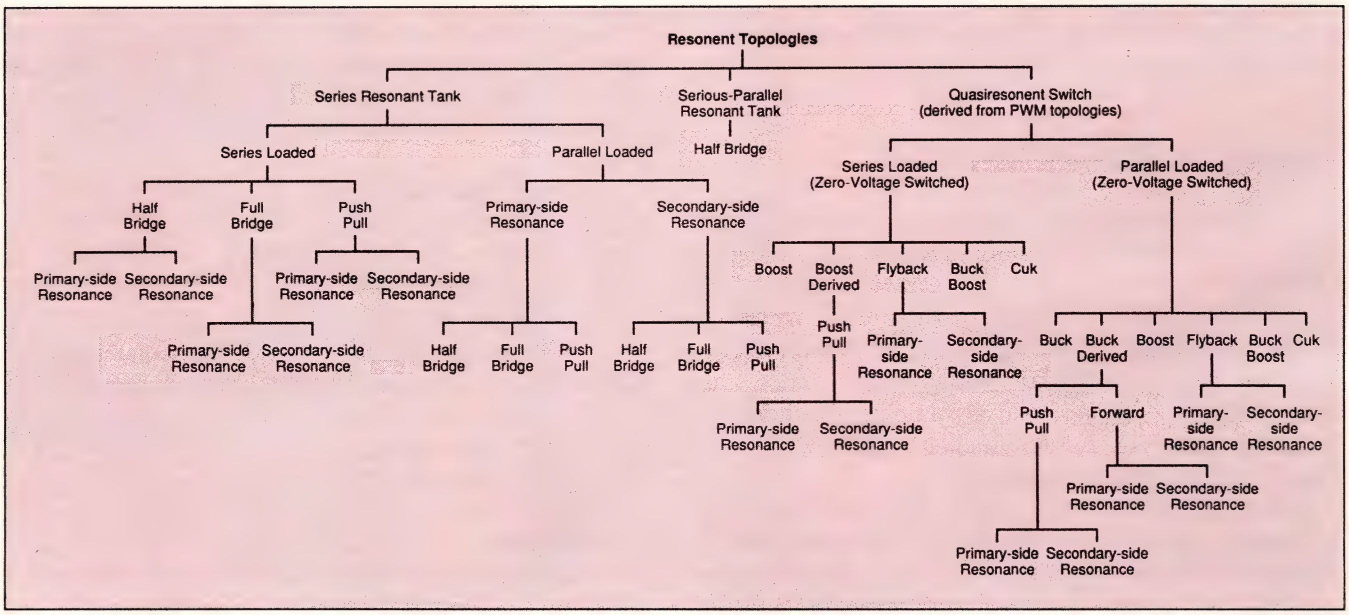

***Fig 2—Resonant-mode topologies** fall into two basic groups: circuits that follow the more traditional, resonant-tank approach and circuits that include a resonant switch.*

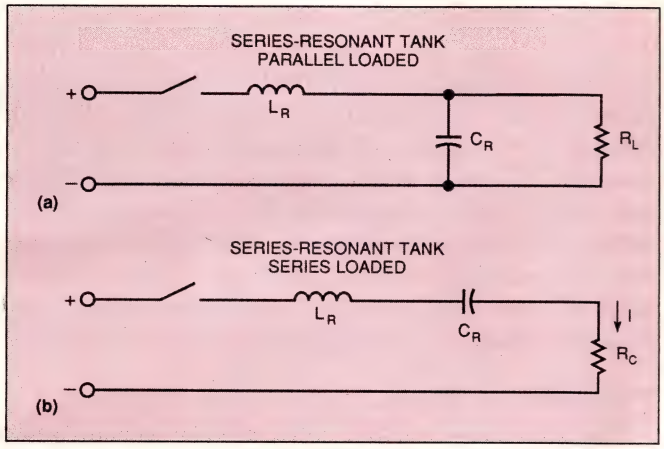

***Fig 3—The connection between the tank and transformer** can be either parallel loaded **(a)** or series loaded **(b)**.*

velopment of new topologies, the chart isn't exhaustive. The traditional topologies stem from the resonant-tank approaches and are shown under the "Series Resonant Tank" branch on the left side of **Fig 2**. More recently developed topologies rely on the resonant-switch approach and are shown on the right side of **Fig 2**, under "Quasiresonant Switch."

The designers who developed early resonant-tank approaches simply modified standard PWM topologies by adding a resonant tank. The resonant tank is usually series resonant; however, a hybrid, series-parallel tank connected in a half-bridge configuration does exist, as shown in the center branch of **Fig 2**. The next level of resonant-tank classification depends on the connection between the transformer and the resonant tank; the tank can be either series loaded or parallel loaded (**Fig 3**). The series-resonant, parallel-loaded converter traditionally is called a parallel-resonant converter.

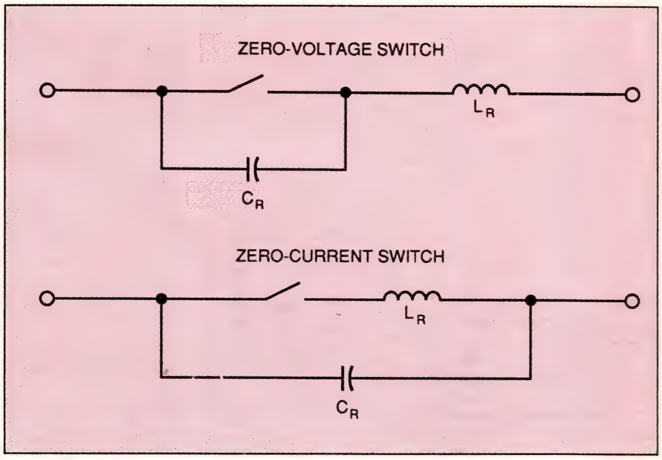

***Fig 4—The resonant-switch technique** simply replaces the switch of a PWM topology with either a zero-current **(a)** or zero-voltage **(b)** resonant switch.*

The next level of resonant-tank classification concerns the type of PWM topology that each class of tank is based on—half bridge, full bridge or push pull. The circuits based on these various topologies differ according to the transformer type, the number and position of switches, the type of output rectification, and the normalized voltage and current stresses expected on all components.

Resonant mode and PWM are close relatives

The resonant-switch technique (**Ref 2**), shown on the right side of **Fig 2**, involves either a zero-voltage or zero-current resonant switch (**Fig 4**) inserted into a PWM-related topology in place of a normal switch. The resonant-switch topologies can replace the familiar PWM topologies, including the buck, boost, flyback, forward, and Cuk converters.

You'll notice further levels of classifications in **Fig 2** that divide all of these resonant-mode designs into either primary- or secondary-side resonance. Secondary-side resonance is accomplished by using the leakage inductance of the transformer as part of the resonant inductor and by moving the resonant capacitor to the secondary side of the transformer. However, primary-side resonance—the more commonly used technique—is simpler to perform.

So far, **Fig 2**'s classifications apply to the supply's transformer and resonant-tank connections. But the various methods of switch control shown in **Fig 5** also

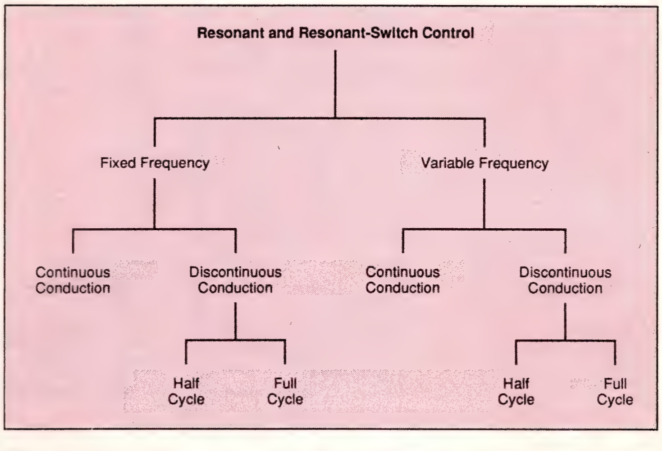

***Fig 5—Discontinuous conduction with a variable control frequency** is the most common implementation of resonant-mode designs. Half-cycle conduction requires the use of a unidirectional switch; full cycle requires a bidirectional switch.*

Resonant-mode designs improve upon PWM techniques by allowing lossless switching at higher frequencies.

determine the supply's operation. If the switch control's frequency is equal to or greater than the resonant tank's natural frequency, the power supply operates with continuous conduction. In other words, the current will be flowing at all times through the resonant components. Continuous conduction is a valuable control method for high-power applications, but this method isn't desirable for most resonant-mode designs because it doesn't provide lossless switching.

Instead, most resonant-mode designs use discontinuous conduction. This condition occurs if the control signal's switching frequency is always below the resonant frequency. With discontinuous conduction, a dead time exists when no current flows in the resonant tank. The switch can either conduct current in one direction (half cycle) or bidirectionally (full cycle).

The circuit shown in **Fig 6** serves as a good example to illustrate the various cycles and required control signals of a typical resonant-mode design. This off-line power supply takes in 110V ac and produces 5V dc at 25A. This 5V supply's design is classified as a series-resonant LC tank with a parallel-loaded transformer and primary-side resonance in the half-bridge configuration. The design implements discontinuous-conduction control with full-cycle conduction. The controller turns off the switch at the zero-current point in the resonant inductor's current waveform.

Waveforms say it all

The waveforms in **Fig 7** illustrate the various intervals during one cycle of this supply's operation. In interval A, initially no current flows in the resonant inductor, L_R, and the voltage across the resonant capacitor, C_R, is zero. The output choke, L_2 (which is a large-value inductor), filter capacitor, C_{OUT}, and resistive load (not shown) collectively resemble a dc current

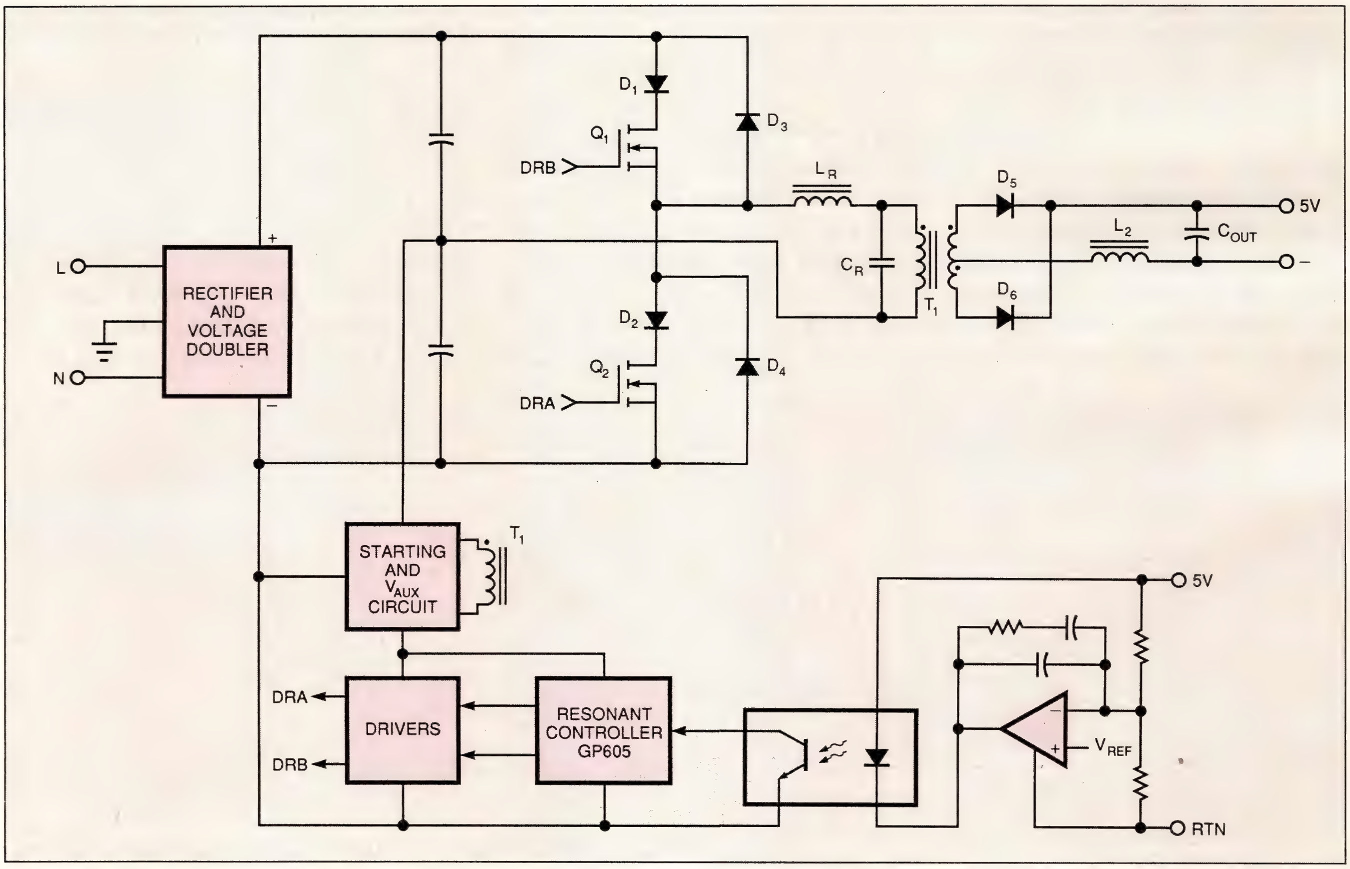
D1
D3
Q1
DRB
LR
D5
5V
L2
COUT
−
CR
T1
D6
L
N
+
RECTIFIER AND VOLTAGE DOUBLER
−
D2
Q2
D4
DRA
STARTING AND VAUX CIRCUIT
T1
5V
DRA
DRB
DRIVERS
RESONANT CONTROLLER GP605
−
+
VREF
RTN

***Fig 6—Switches Q_1 and Q_2 of this 5V switching power supply** alternatively apply half of the rectified voltage to the resonant tank, which comprises L_R and C_R. D_4 and D_5 are ultrafast recovery diodes that conduct the reverse current.*

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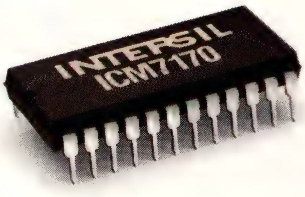

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Resonant mode's higher frequencies result in smaller transformer and output-filter requirements and in reduced output ripple.

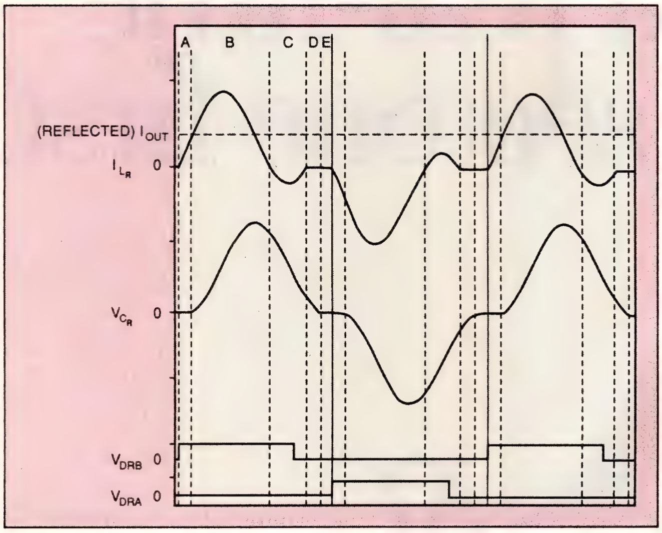

Fig 7—These half-bridge, resonant-converter waveforms *illustrate the current, voltage, and control functions. Note the linear discharge of the resonant capacitor in mode D. The charge left on the capacitor varies with the line voltage. The slope of the discharge varies with the load current.*

load. This load causes both D_5 and D_6 to be on. When V_{DRB} goes high, Q_1 closes, and the current through L_R increases linearly until it matches the output-current requirements.

Interval B begins when C_R begins to charge. V_{CR} and I_{LR} are now sinusoidal in shape because of the resonant tank's action. The load acts as a constant current sink, so it doesn't affect the shape of I_{LR}'s or V_{CR}'s waveforms. The load's only effect is that it causes a dc shift in the current waveform. Note that I_{LR} isn't centered around zero.

Interval C begins when I_{LR} crosses through zero, and current starts to flow back from C_R into the inductor and back to the line. The transformer's primary is still taking from the dc current, which is needed to drive the output choke, from the resonant tank. The FETs, Q_1 and Q_2, although not actively turned off at the beginning of this interval, don't allow reverse current to flow because of their series-blocking Schottky diodes, D_1 and D_2. The antiparallel diodes, D_3 and D_4, carry the reverse current. During interval C, the controller must end the cycle by turning off Q_1's gate drive when the current waveform returns to zero at the end of its negative excursion; hence the name "zero-current switching."

At the end of interval C, I_{LR} is equal to zero, but the resonant capacitor still retains a positive voltage. In mode D, this voltage discharges to zero linearly because the output choke is acting as a constant-current load. In modes A, B, and C, the voltage applied to the output choke is equal to V_{CR} multiplied by the transformer's turns ratio, n. The turns ratio in this application is 1:12. The output-filter cap will try to minimize the ripple by providing current to the load, so in the modes A, D, and E, the choke current will be decreasing.

Interval E, known as the dead time, begins when the resonant capacitor is fully discharged. The freewheeling rectifying diodes, D_5 and D_6, prevent the output capacitor from being pulled below ground. Both D_5 and D_6 turn on to provide current to the choke.

Energy transfers to the output during the tank's resonant cycle (intervals A, B, and C); it also transfers just after the cycle is complete, while a positive voltage still exists on the resonant capacitor (interval D). After C_R discharges, there is a time when no energy conversion takes place (interval E). The conversion ratio—voltage in vs voltage out times the turns ratio—depends on the relative times of intervals A through D vs interval E.

Because the resonant-tank frequency is fixed, modulation of this dead time is an obvious way to regulate the output. By using an error amplifier to compare the output voltage to a reference, you can generate a signal to control the frequency of the GP605 controller. You can use the square pulses of fixed on-time outputs of this controller to trigger the power FETs. The control pulses that turn on the FETs must occur one at a time, and the controller must insert a variable dead time between alternate pulses, as required by the resonant-mode scheme. This type of dual output is suitable for the gate drive of FETs in the half-bridge configuration.

As the load increases, the dc level of I_{LR} increases. The maximum amount of load current is available when the current waveform is just barely able to return to zero; that is, when I_{LR}'s negative peak during interval C is tangent to zero. Under this condition, no dead time (interval E) occurs. If the load (and therefore I_{LR}) increases to the point where the current can't return to zero, you lose all the zero-current switching benefits, and you'll have high losses. Therefore, you have to make a tradeoff between lossless switching and the amount of power supplied to the load. You must design the resonant tank so that I_{LR} has a swing

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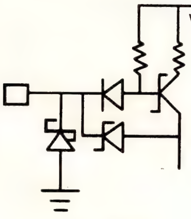

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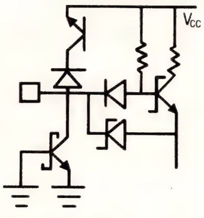

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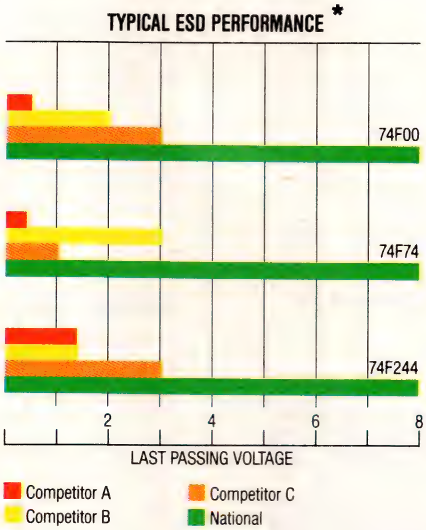

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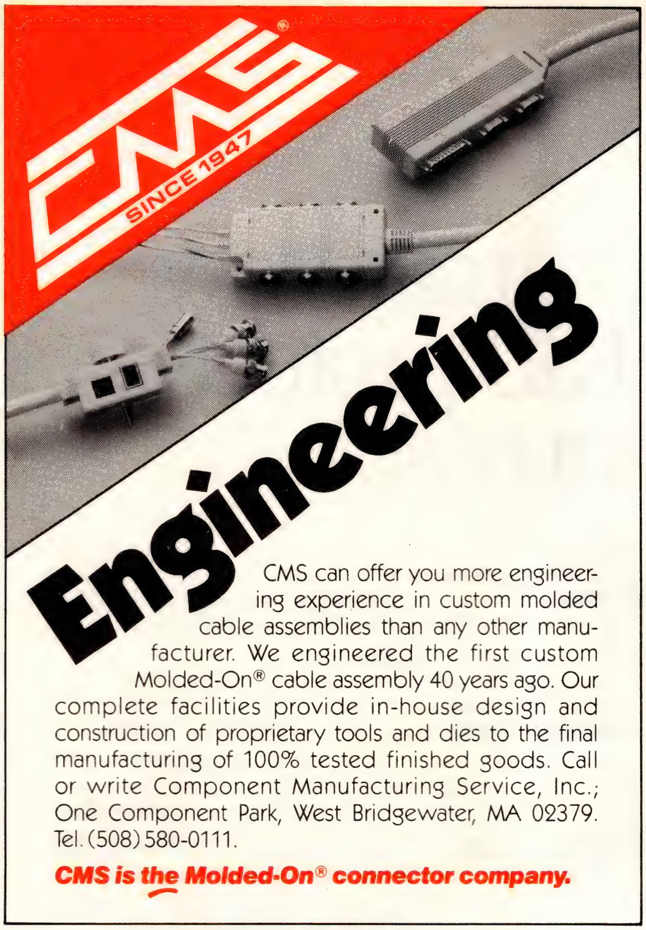

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large enough to fulfill your design's specifications. Part 2 addresses these design concerns and also examines the design of the control loop, resonant tank, and transformer in more detail. **EDN**

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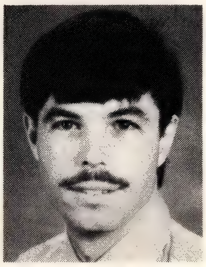
3. Sykes, Fred, "Resonant mode power supplies: a primer," *IEEE Spectrum*, May 1989, pg 36.

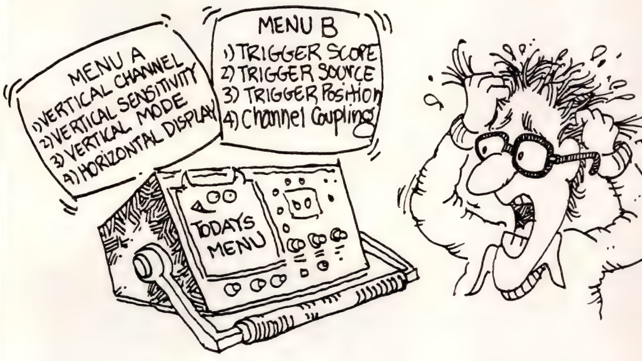
Author's biography



Frederick E Sykes is a design engineer with Gennum Corp in Burlington, Ontario, Canada, where he designs analog ICs for high-performance, power-supply applications. He codesigned the first commercially available, monolithic, resonant-mode controller. Fred has a BEng in electrical and computer engineering from McMaster University (Hamilton, Ontario, Canada). His leisure activities include sailboarding, skiing, and computer programming.

Article Interest Quotient (Circle One)
High 482 Medium 483 Low 484

"USER-FRIENDLY" IS THE WATCHWORD FOR TODAY'S OSCILLOSCOPES.



Recent advances in oscilloscope technology have proceeded at a very rapid pace. Almost across the board these advances have been beneficial. In these "high-tech" units, manufacturers have held out the promise of a scope loaded with every feature under the sun. And from auto setup to menu select capabilities, every function is shown to be accessible at the touch of a button. But a true reading of a scope's user-friendly potential cannot be obtained until the scope is applied to an actual project. Only at that point can it be determined how much time it will take to gain full use of the oscilloscope.

A new unit may allow work to proceed without a hitch. But where things haven't gone smoothly, situations similar to this have been reported. Turn on the new unit and a menu immediately appears. Should horizontal display, triggering, channel coupling, or another of the many alternatives listed be chosen? Triggering is chosen, but then a submenu is displayed. Now a decision has to be made among trigger source, trigger coupling, trigger slope, etc. Okay, trigger source is opted for and set. Now, if information from another menu is needed, trigger source must be exited and the needed menu brought up. With all this going on, the engineer may become distracted from the task at hand — the close observation of waveforms on the screen.

This potential for confusion points up exactly why careful examination has to be made when equipment is advertised as user-friendly. A closer look may reveal that sophisticated, menu-driven scopes are not always the easiest to operate. A new scope that builds and improves on controls that are already being used efficiently may turn out to be the most user-friendly. Toward this end, a number of features have been developed that improve the efficiency and precision of conventional oscilloscopes. Among these features are cursors with digital readouts, auto ranging, and relative hold-off, to name a few.

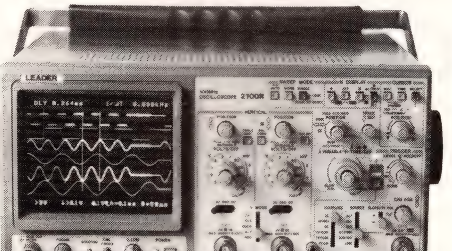
CURSORS WITH DIGITAL READOUTS — A QUANTUM LEAP IN EFFICIENCY

One user-friendly breakthrough, in terms of both speed and accuracy, has been the development of cursors. Whereas older scopes required counting graticule divisions, cursors now allow measurements to be displayed digitally. Cursors supply readouts such as time, voltage, frequency, and phase, plus time and voltage difference ratios. Time difference ratio is ideal for performing phase shift measurement. With voltage difference ratio, the measurements of waveform overshoot can be made. The cursors make measurement of waveform parameters more consistently accurate.

On-screen readouts provide a constant reminder of operating conditions and keep a record of these settings in waveform photographs. Many important settings are displayed, including TV field/line setting, which expands the oscilloscope to video-related applications.

AUTO RANGING AIDS TIME BASE SELECTION

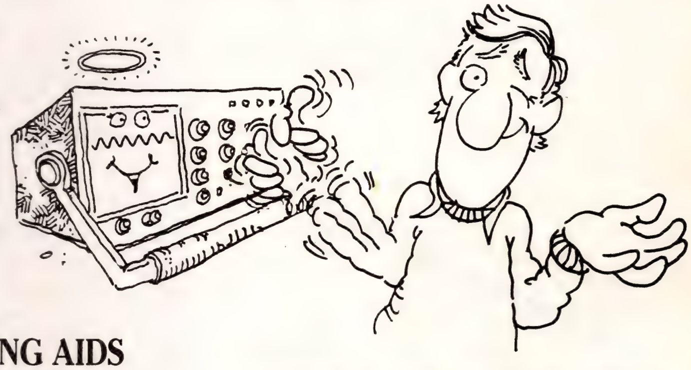
Of great help is a scope that offers both auto ranging and alternate time base. Auto ranging selects from 22 possible time base settings to display an optimum number of cycles. This is another feature that makes an oscilloscope a bit more user-friendly. Alternate time base allows observation of both the main and the delay time base, so that the expanded portion of the waveform can be simultaneously compared with the original.



100 MHz CRT readout Model 2100R from Leader Instruments Corporation.

ANOTHER FEATURE TO CONSIDER CAREFULLY — DOES THE WARRANTY HAVE TEETH?

Another factor that needs to be examined just as closely as those mentioned previously is the warranty. In competing for market share, longer and more extensive warranties are offered every year. Before basing a decision only on warranty, though, consider its true value if the equipment is not reliable. Remember, no warranty can make up the cost of a scope that's out for repairs for 4 to 6 weeks, or more. That's why even more important than the actual wording of a warranty is the reliability that's built into every oscilloscope. Ideally, of course, no piece of equipment should ever break down. But if a unit needs repair, it's important to know who provides the fastest turnaround time in the industry.



Now there is an oscilloscope whose user-friendly format includes all the features discussed earlier, plus many more. This unit, introduced by Leader Instruments Corporation, is the 100 MHz CRT readout with cursors, Model 2100R. The unit is easy to use and also incorporates these additional features: TV full-line selection, alternate triggering, and relative hold-off. This and every other Leader product come with an iron-clad 2-year warranty, which is backed by a return rate of less than 1% during the warranty period and a very rapid turnaround time. In other words, the 2100R offers a complete oscilloscope package.

For more information or Leader's full-line catalog, call toll free: 1 800 645-5104. In NY call 516 231-6900. Or write Mike Hoyer at Leader Instruments Corporation, 380 Oser Avenue, Hauppauge, NY 11788.

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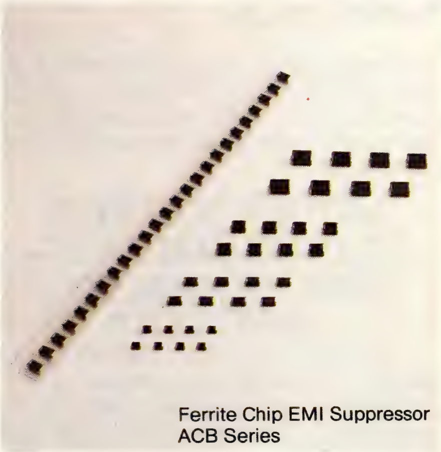

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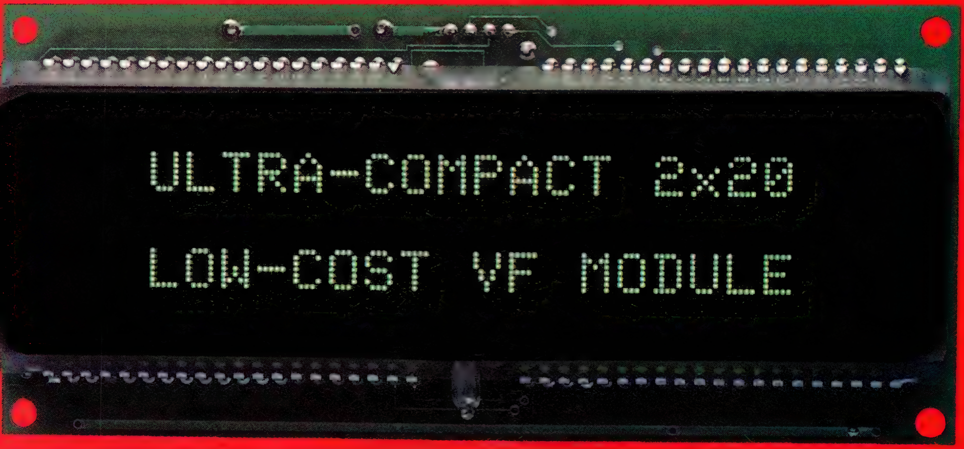

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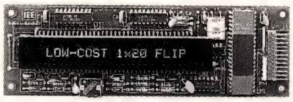

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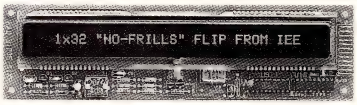

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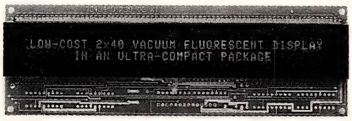
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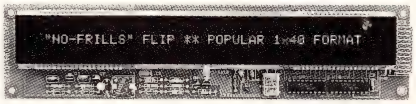

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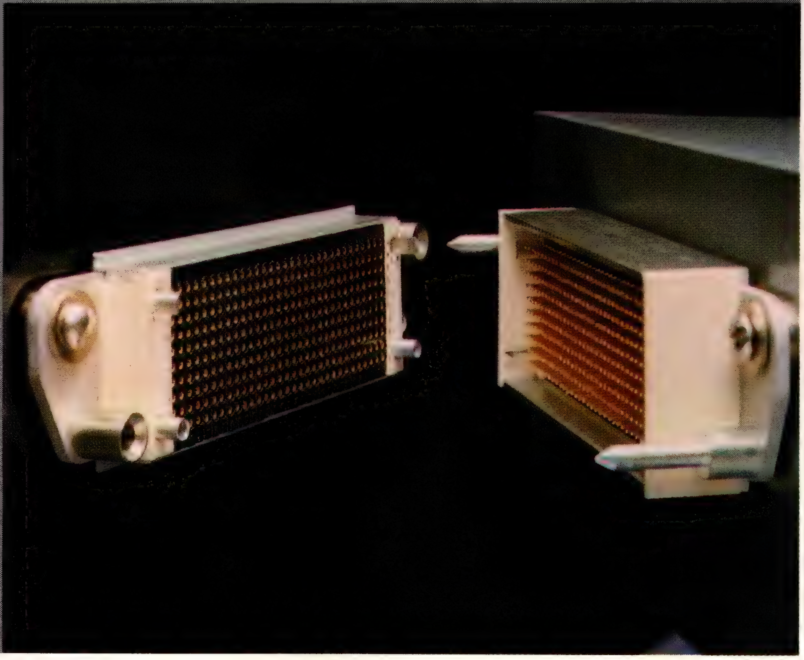

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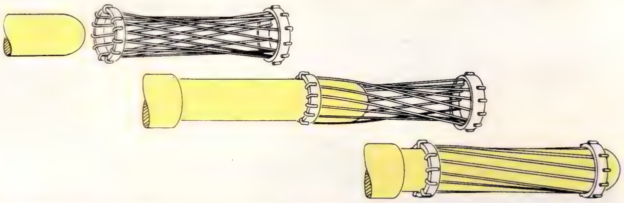

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Model	Input	Features
PM-5050	Thermocouple	J, K, T, S, B, E, N, R linearization
PM-5060	RTD/Thermistor	Supports European and American RTD's
PM-5070	Strain Gage	10V excitation output
PM-5080	Voltage/Current	User-definable scaling

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All units are supplied with a free connector and shipped within 48 hours. Contact DATEL for detailed information.

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CASES	Short-depth, Low-profile, 1/8 and 1/16 DIN, Uncased
POWER	+5 Vdc, 115 Vac, 230 Vac
FEATURES	4-20 mA In, BCD Out, Ruggedized, Units Display

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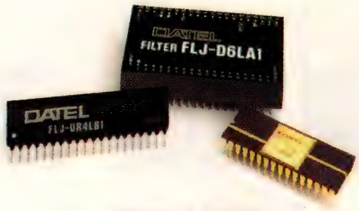

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Precision, performance, portability, and low price are the hallmarks of DATEL's voltage calibrators. The hand-held DVC-350A is a truly portable calibrator with the accuracy (±0.015% of FSR) demanded by critical field applications. The DVC-8500, with 0.005% accuracy, is small enough for the most crowded test bench, but matches the performance of expensive, rack-mounted units.

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DVC-8500	±19.999V dc	0.005%	25 mA	25μV p-p	±4 ppm/ °C

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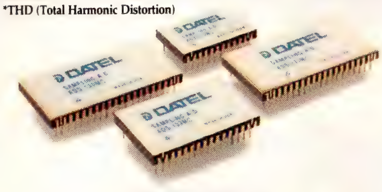
DATEL's video speed 12-bit sampling A/D converters give superior dynamic performance, to bring both harmonic distortion and signal-to-noise ratios to new lows.

Model	Sampling Rate	Effective Bits at Nyquist Frequency	THD* at Nyquist Frequency	Power Dissipation	Package	Price (1-9)
ADS-112	1MHz	11.0	-73 dB	1.3 watts	24-pin DDIP	$259
ADS-132	2MHz	11.0	-73 dB	2.9 watts	32-pin TDIP	$346
ADS-131	5MHz	10.6	-69 dB	4.2 watts	40-pin TDIP	$549
ADS-130	10MHz	10.6	-69 dB	4.5 watts	40-pin TDIP	$775

*THD (Total Harmonic Distortion)



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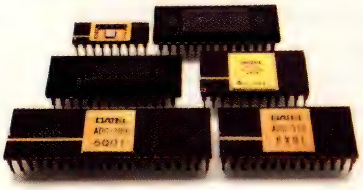
MODEL ADC-	RESOLUTION	SAMPLING RATE (MHz)
207	7 Bits	20
208/300/301/302/303/304	8 Bits	20/20/20/50/100/20
310	10 Bits	20



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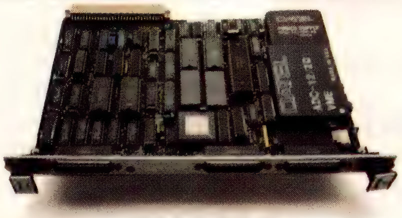
601	16S/8D A/D, 5 TTL, 1 RS-232	12-14-16	300 KHz 68010 CPU
624,6,8	Up to 8 D/A	12-14	Optional Isolation



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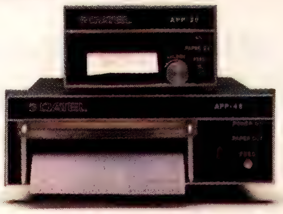
Model	Columns	Interface	Power
DPP-Q7	7	BCD	115, 230 Vac
MPP-20	20	Serial, Parallel	115, 230 Vac, 12 Vdc
APP-20*/48*	20/48	Serial, Parallel, IEEE-488	115, 230 Vac, 12 Vdc

* Mobile mount option available



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Limit noise in designs using advanced CMOS logic

Advanced CMOS devices made with tight line-width transistors provide greater speed, more drive, and use less power than their precursors. You must design more carefully, however, because the cost of these performance increases is a greater level of device-generated noise.

William Hall, *National Semiconductor* and
Charles Pace, *Compaq Computer*

As logic designers find creative techniques to reduce device-generated noise, systems designers live with this noise by employing high-performance design rules. To implement these design rules, you must pay more attention to potential noise sources. By following good design practices, you can achieve maximized system performance and reliability.

Today's migration toward advanced CMOS logic has caused a heightened awareness of prudent, high-performance design techniques and reinforces the need for discipline in digital-logic design. One design-rule violation might create multiple noise manifestations. Proper transmission-line terminations, for example, can combat reflections, crosstalk, and EMI. Many design rules have evolved from rules used with older technologies.

Crosstalk is a phenomenon in which electromagnetic energy is coupled from an active signal to a passive signal. This coupling is caused by the capacitive and inductive interaction of the two signal lines. In most practical applications, these signal lines consist of pc-board traces or backplane wires.

There are two forms of crosstalk—forward crosstalk and reverse crosstalk. You measure forward crosstalk at the far end of the passive line, whereas you measure reverse crosstalk at the near end. Changes in voltages and currents in the active line cause both crosstalk mechanisms.

A current and a change in voltage result from a signal transition on the active line. **Fig 1** illustrates a transition from low to high; a voltage wavefront propagates from the driver to the receiver, and current flows in the same direction. The wavefront propagating down the active line develops current in the passive line through both capacitive coupling and the mutual inductance between the two lines. Layout characteristics determine the efficiency of capacitive and inductive coupling. Long, adjacent signal lines provide effective capacitors and inductors.

The change in voltage across the intrinsic capacitance of the two lines creates a capacitive current (I_C); it flows in both directions on the passive line. The changing current in the active line generates an inductive current (I_L) in the passive line. The mutual inductance (L) of the two lines creates this transformer action. The inductive current flows in the opposite direction from the current flow in the active line. In **Fig 1,** the inductive current (I_L) on the passive line flows from the far to the near end. Summing the capacitive- and

Crosstalk develops on a passive signal line when a portion of the trace runs parallel to an active signal trace.

inductive-current components yields a net current of $I_C + I_L$ toward the near end (passive line) and $I_C - I_L$ toward the far end (passive line). In most pc-board and backplane environments, the inductive current is much larger than the capacitive current. The net-current flow in the passive line will be from the far end to the near end, and it reacts with the impedance of the line to create a voltage ($V = IR$).

What crosstalk looks like

Forward crosstalk appears as a voltage spike at the point on the passive line that coincides with the wavefront propagating down the active line. The spike duration is equal to the duration of the active-signal rise time (t_r). The net current flows toward the near end, causing the voltage to be negative with respect to ground at the far end. The amplitude of the noise spike is directly proportional to the length of the coupled lengths of the two lines.

You can measure reverse crosstalk at the near end of the passive line; it appears as a noise pulse. The pulse width is equal to two line delays ($2t_d$). The active signal takes one line delay (t_d) to propagate from the driver to the receiver. The line delay (t_d) equals the propagation velocity (v) times the line length (L). (For a more in-depth discussion of transmission lines and their effects, see **Ref 1**.)

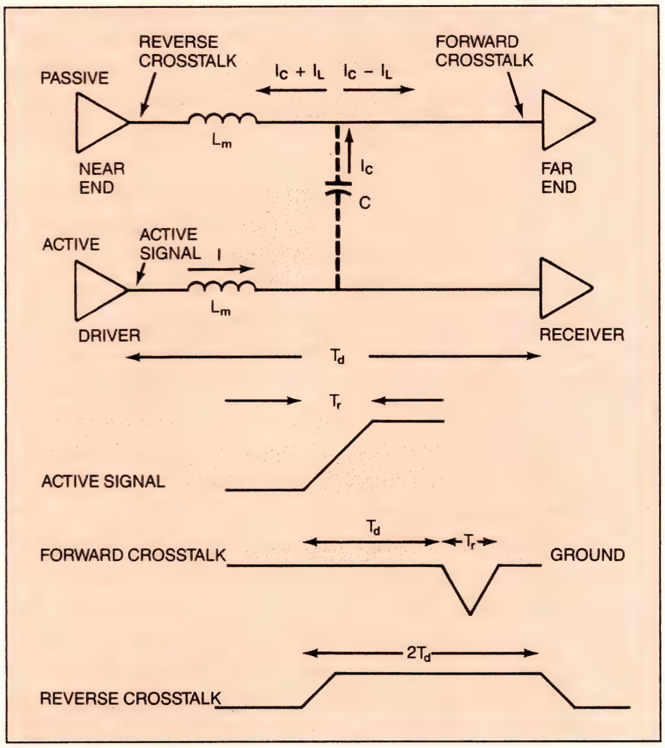


***Fig 1—The inductive and capacitive coupling** of a passive trace to an active one causes crosstalk. You can measure forward crosstalk on the passive trace near the receiving end of the active signal.*

In most cases, the propagation velocity will be approximately 1.7 nsec/ft. As the signal edge propagates down the active line, it acts as a source of current, maintaining the current flow to the near end of the passive line. After the active edge reaches the end of the trace, the edge stops acting as a current source. Because of transmission-line effects, it takes an additional line delay (t_d) for the zero-current condition to propagate from the far end to the near end. This second line delay causes the pulse width of the reverse-crosstalk pulse to be $2t_d$. If the line length is such that $2t_d < t_r$, then the reverse crosstalk will never reach its full amplitude. Assuming that you should limit reverse crosstalk to less than its maximum amplitude, you can solve the maximum coupled line length for $L_{MAX} = t_r/2v$. For advanced CMOS, t_r(FACT) = 3.8 nsec (**Ref 1**). Therefore, L_{MAX}(FACT) = 13.4 in.

The physical relationship between the drivers and receivers on the active and passive lines determines whether forward or reverse crosstalk will be a problem. Advanced CMOS outputs aren't affected by either form of crosstalk, because they have very low impedances. Receiver inputs are more problematic; if you orient the active and passive receivers at the same end of the two lines, forward crosstalk will be a concern. On the other hand, if you locate the two receivers at opposite ends of the lines, then reverse crosstalk might be the bigger problem. Most logic families won't react to short noise spikes (2 to 3 nsec, as measured in the middle of the spike) of forward crosstalk. Reverse crosstalk requires more design attention, however, because of its greater pulse width.

Design rules for minimizing crosstalk

When you're designing to minimize crosstalk, you should consider what sort of signals are sensitive to crosstalk. On a typical pc board, most of the long, adjacent traces are very likely to be data or address buses with synchronous signals. Reverse crosstalk isn't a problem, because these signals tend to run in the same direction. Also, because forward-crosstalk noise is synchronous with the signal edges and occurs during the propagation-delay time of the driver, the receivers won't be clocked while the noise is present.

Other synchronous traces that run near these long buses may require attention if the signals they carry propagate in the opposite direction to the bus, or if they're not synchronized to the bus. Also, if the coupled line length is less than L_{MAX} (calculated above), then crosstalk won't be a concern, because the injected noise would occur within the rise time of the system clock that caused the synchronous transition.

For the signals where line length is greater than L_{MAX}, you can use many layout techniques to eliminate crosstalk. Don't route signals on the same layer (15-mil separation) together for distances greater than L_{MAX}. Signals separated by greater than 30 mil (same layer) will couple minimal energy. Synchronous signals on adjacent pc-board layers offer the greatest potential for cross-coupled energy because of their overlapping geometries. You can eliminate this cross-coupling by routing signals on adjacent layers in perpendicular directions to minimize coupled lengths.

Asynchronous signals are more sensitive to crosstalk noise. In designs where a dedicated plane isn't available, you should route asynchronous signals away from large, long buses. Also, keeping the asynchronous trace length as short as possible minimizes coupling. Finally, placing ground traces between the synchronous and asynchronous traces provides crosstalk shielding.

Wired backplanes present a different dilemma. Crosstalk can occur on long, tightly bundled wires. Here, length rules are highly dependent on the gauge of wire used. Typical backplanes experience minimal crosstalk on wire bundles less than $1.5 \times L_{MAX}$ inches long. For FACT ICs, this measurement translates to 20 in. You should reroute wires that violate this rule out of the bundle or, as an alternative, use twisted-pair or coaxial cable. Very sensitive, long (greater than 3 ft) asynchronous signals should use differential drivers.

Termination resistors reduce crosstalk. Generally, you use terminations to combat reflections on asynchronous signals; reduction of crosstalk is a benefit you get free. If the device at the near end of the passive line in **Fig 1** is an advanced CMOS receiver, then the current flowing from the far end would flow into a high-input impedance and generate a large noise spike. In this case, the input of the receiver sees 100% of the induced crosstalk. If the passive line is terminated in its effective impedance, the induced crosstalk will be reduced by 50%. For advanced CMOS, use an ac termination.

The advent of advanced CMOS technologies has allowed system designers to enjoy advanced bipolar speeds, near-zero standby power, increased transmission-line driving capacity, and increased CMOS-type noise margins. However, the price of this added performance is increased internal rail noise (ground bounce).

One or more outputs switching from logic 1 to logic 0 generates internal rail noise. This switching allows the load capacitance (C_l) to discharge through the lower output transistor and the intrinsic package inductance to ground **(Fig 2)**. The internal rail noise, V_{GB}, is the

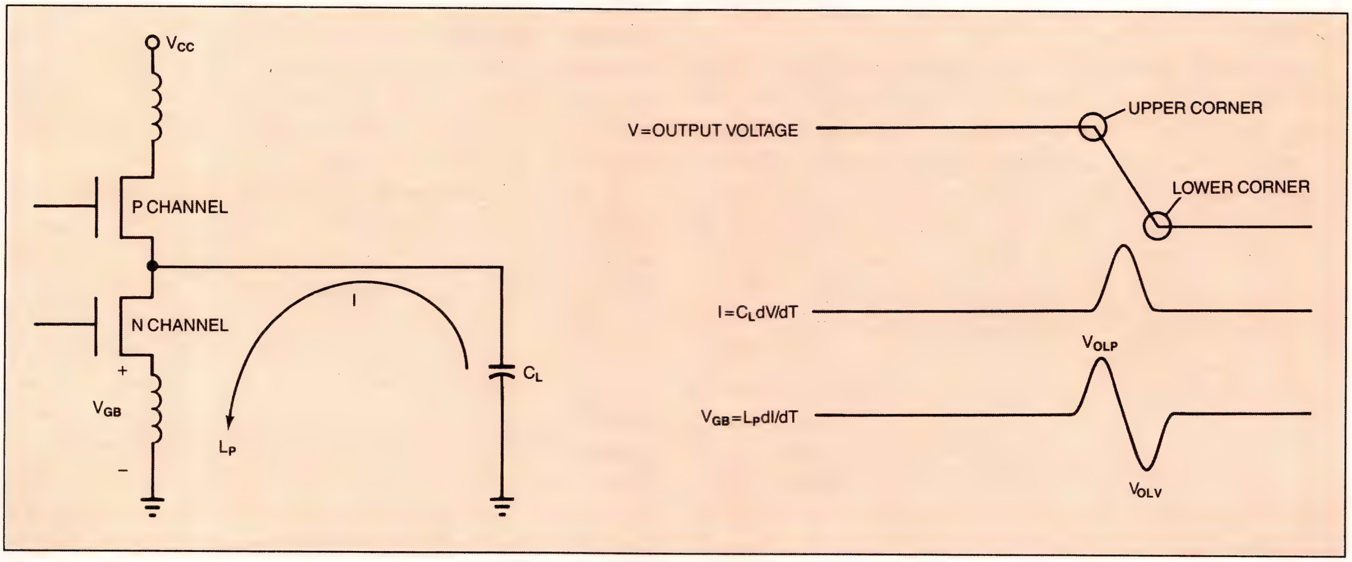


Fig 2—When the circuit tries to discharge the load capacitor, it generates internal rail noise. *The changing current flows through the device package, inducing a voltage across the package inductance. As a result of this induced voltage, the internal device rail is at a different potential than the external system rail.*

Crosstalk is more of a threat to asynchronous signals than to synchronous ones, because the clock generally won't inappropriately latch the noisy signal.

second derivative of the output voltage waveform. The noise consists of a positive spike (V_{OLP}) caused by the upper corner of the output waveform and a negative spike (V_{OLV}) caused by the rapid shut-off of output current. The amplitude of the noise is directly proportional to the number of outputs switching, because the current is additive through the common package inductance. These disturbances couple through a common ground onto quiet, nonswitching outputs and inject an unwanted glitch into the system **(Fig 2)**.

Test fixtures exaggerate rail noise

The internal rail-noise amplitude is difficult to predict in an actual system. You can use test fixtures to measure noise levels; they don't accurately emulate system noise levels, however. Test fixtures utilize IC sockets for multiple measurements, are reconfigurable through inductive switches, and use lumped capacitive loads (50 pF is standard) for repeatability. Actual systems use soldered devices that decrease inductance, and smaller capacitive loads are distributed along a pc-board trace or backplane wire. Therefore, the voltage across the load in a real circuit is lower than in the test fixture.

The distributed inductance of the signal-carrying media acts, with the package inductance, as a voltage divider. As a rule, test-fixture noise will be 2 to 3 times higher than actual system noise. The noise from FACT logic can measure 2.1V in a test fixture (**Ref 2**). In an actual system, most internal rail noise ranges from 0.5 to 1.0V.

As with crosstalk, the key to designing systems that have internal rail-noise immunity is learning where to focus design effort. Like crosstalk, internal rail noise is only a concern on asynchronous signals. Because internal rail noise occurs within the rise or fall time of the synchronous switching outputs that generate it, the noise itself can't be errantly clocked. However, internal rail noise on asynchronous signals can change the state of inactive data. Therefore, you only need to be concerned about asynchronous paths. Fortunately, in most systems, asynchronous paths make up a small fraction of the connections.

To cause a system error, noise energy on a signal line must exceed the input threshold of the succeeding device. Internal rail-noise pulse widths are equal to the edge rates, and they're typically less than 4-nsec wide at the base. To trigger a CMOS-level input, an internal rail-noise pulse must reach an amplitude of 3V. These levels aren't normally reached in either actual systems or test fixtures. However, TTL-level inputs will trigger on internal rail-noise pulses whose amplitudes exceed 1.7V **(Fig 3)**. Although these levels can be found using test jigs, they generally don't occur in actual systems because of the effect of distributed loads. In order to generate more than 1.7V of noise when using advanced CMOS logic, seven or more outputs must be switching.

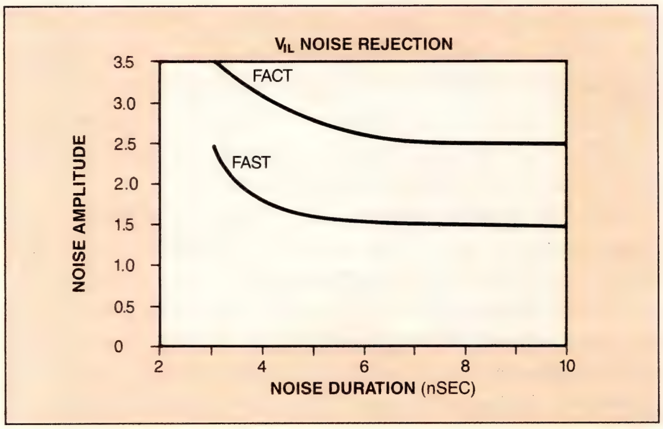


***Fig 3—These curves show that advanced CMOS logic has better noise immunity than FAST logic.** The area below the curves indicates where the signal doesn't have enough energy to switch the inputs.*

To focus on the areas where internal rail noise is most likely to show up, consider using an advanced CMOS octal driving asynchronous signals into devices with TTL thresholds. You can use several techniques to reduce the amplitude of the bounce. The easiest trick is to route the asynchronous signals through the package pins closest to the ground pin. This routing methodology can reduce noise levels by as much as 40% compared with the worst-case pins.

To minimize internal rail noise, you should follow prudent layout techniques. Use multilayer pc boards with dedicated power and ground planes. Solder the device's power and ground pins directly to their respective planes. Avoid the use of ground traces as much as possible—they add additional ground-path inductance. In designs utilizing surface-mount devices, where there are no pins to solder directly to the power planes, keep the V_{CC} and ground connections short. Also, avoid using sockets and wire wrap for end-item equipment. Decouple every driver with a 0.1-μF tantalum capacitor and place them as close as possible to the driver's ground pin. Finally, if all else fails, replace the offending device with FAST, ALS, or one of the new, low-noise advanced CMOS technologies.

The same phenomenon of large, fast current transients that creates internal package noise also places a strain on a system's power-supply network. Because of the high-speed nature of advanced CMOS and other high-performance logic families, you must regard V_{CC} and ground traces as transmission-line networks and not as zero-impedance connections. The use of a good power-distribution network is critical to maintain system reliability and reduce system noise.

The impedance of power-supply networks can vary from more than 100Ω to 2Ω. In TTL's early days, when devices were slow and had limited output drive, engineers designed systems on single-layer boards with V_{CC} and ground traces side by side. Unfortunately, a typical single-layer board with side-by-side V_{CC} and ground traces has a power-supply impedance of approximately 100Ω.

In the beginning, there were double-sided boards

As systems became more complex, and technologies became faster and offered greater output drive, double-sided boards became the norm. Usually, you placed V_{CC} traces on one side and ground traces on the other. Placing the supply traces on opposite sides of a 2-layer board reduces the power-supply impedance to approximately 68Ω.

The emergence of advanced bipolar technologies that feature higher speeds and greater sink-current capability underlines the need for ground planes. Although these bipolar devices can sink large amounts of current, their source capability is small. Therefore, you have limited need for V_{CC} planes. The addition of a ground layer on one side of the board further reduces the impedance to approximately 50Ω.

Advanced CMOS devices have equal pullup and pulldown capabilities. This capability demands that you use both V_{CC} and ground planes and reduces the impedance to approximately 2Ω.

An example highlights the need for low-impedance sources of current. Consider an octal device connected into the middle of eight 100Ω lines **(Fig 4)**. The two 100Ω lines on each side of the driver act like two resistors in parallel, generating a net 50Ω load on each driver. To switch the load from low to high, each driver must supply 94 mA of current (4.8V/50Ω). If all eight drivers switch simultaneously, the combined current requirement exceeds 750 mA. If the power-distribution network can't supply all of that current because of high-impedance connections, the result is a significant V_{CC} droop and reduced performance. This octal device simultaneously driving eight 100Ω lines, with V_{CC} and ground connected by traces to the power supply, yields a V_{CC} droop of 75V (750 mA x 100Ω).

Of course, this droop wouldn't occur. As the device starts to switch, the V_{CC} droop would limit the current available to switch the lines, and output edge rates would slow down. The result is a slow system with noisy signal traces.

To preserve the advantages of advanced CMOS logic, you should use V_{CC} and ground planes. If you use traces or wire-wrap systems, limit daisy chaining on each V_{CC} and ground line. When devices on the daisy chain nearest to the supply are switching, those devices furthest away receive the effects. The resultant noise couples onto the outputs of the devices furthest away, creating noisy signals. When you use power-supply traces, make sure they are gridded; that is, as many connections as possible should be made between each power trace to minimize the effect of V_{CC} and ground noise generation.

The use of V_{CC} and ground planes is only a piece of the design solution to high-speed switching requirements. Even with a 2Ω V_{CC} impedance, the 750-mA current required in the above example still generates 1.5V of V_{CC} droop (750 mA x 2Ω). The second part to

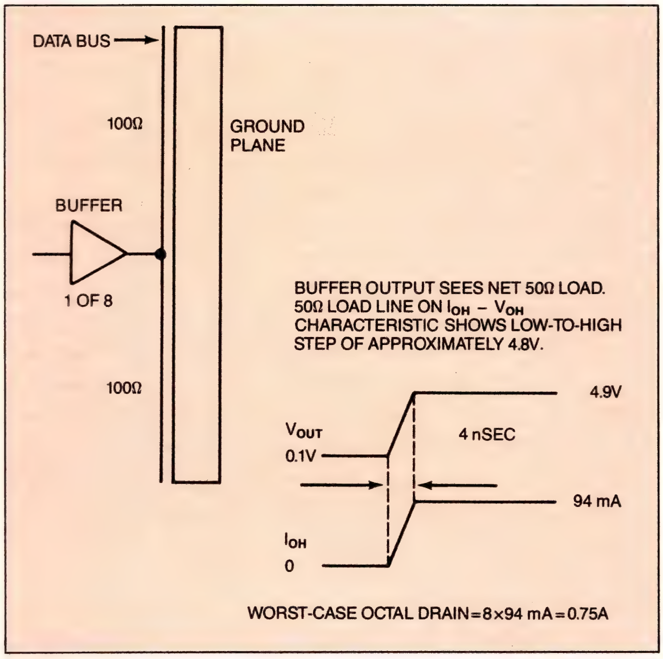

DATA BUS
100Ω
GROUND PLANE
BUFFER
1 OF 8
100Ω
BUFFER OUTPUT SEES NET 50Ω LOAD. 50Ω LOAD LINE ON I_{OH} – V_{OH} CHARACTERISTIC SHOWS LOW-TO-HIGH STEP OF APPROXIMATELY 4.8V.
4.9V
V_{OUT}
0.1V
4 nSEC
94 mA
I_{OH}
0
WORST-CASE OCTAL DRAIN=8×94 mA=0.75A

***Fig 4—If eight outputs, each driving 50Ω loads,** switch simultaneously, then your circuit creates a 94-mA current surge per output line, or 0.75A for the chip, for the 4 nsec it takes to charge the data bus.*

Internal rail noise is the result of outputs switching from high to low states, discharging the load capacitance to ground through the package inductance.

improving high-speed performance is decoupling. Decoupling capacitors act as localized sources of current during switching transients. Proper decoupling can decrease V_{CC} and ground noise to less than 100 mV.

The standard, bipolar decoupling rule suggests that you place decoupling capacitors throughout a board, with one capacitor per buffer and one capacitor for every three logic devices. This number of capacitors is adequate for bipolar families where only the buffers supply the large transient currents necessary for transmission-line driving. Because bipolar logic devices feature very low output drive capability and can only supply small switching currents, they don't require as much decoupling as advanced CMOS devices.

Apply the same decoupling rule to advanced CMOS, but remember that every device can act like a buffer; that is, all advanced CMOS devices exhibit transmission-line driving capability. Simply, the decoupling rule for advanced CMOS is one decoupling capacitor per device, whether it's a buffer or a simple logic device. A good, general guideline is that more decoupling is better than less.

Returning to the octal example, you can calculate the recommended capacitance. Solving for C in the capacitor equation, $I = C\,(dV/dT)$, yields $C = (I\,dT)/dV$, where I is the 750-mA current from the octal example; dT is the time it takes to turn on the current, or the edge rate (4 nsec); and dV is the allowable maximum V_{CC} droop. If your V_{CC} noise limit is 100 mV, then C is 0.030 μF. Therefore, choose a capacitor that's at least this size. Empirically, decoupling capacitors of 0.047 μF are very effective in reducing V_{CC} noise.

The type of capacitor you use is also important. Because they have 4-nsec edge rates, advanced CMOS signals contain frequencies in the hundreds of megahertz. Because of these high speeds, you should use capacitors with good RF characteristics. The most important specification is the inductance of the capacitor, called the effective series inductance, or ESL. Reducing the inductance of a capacitor improves its high-frequency performance. Tantalum capacitors have excellent ESL characteristics and work well as decoupling capacitors.

Keep the leads short

The parasitic inductance of the leads and packaging also affects the performance of the capacitor. The longer the leads, the greater their inductance. Surface-mount chip capacitors have the lowest package inductance of all capacitors, because they have no leads. But these capacitors aren't always an option. When using leaded capacitors, always keep the leads as short as possible.

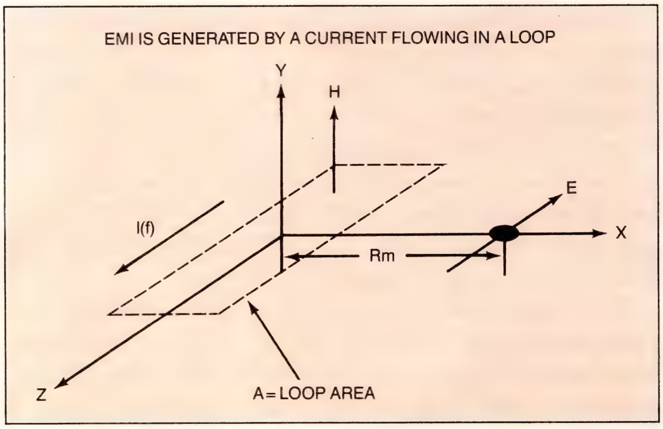
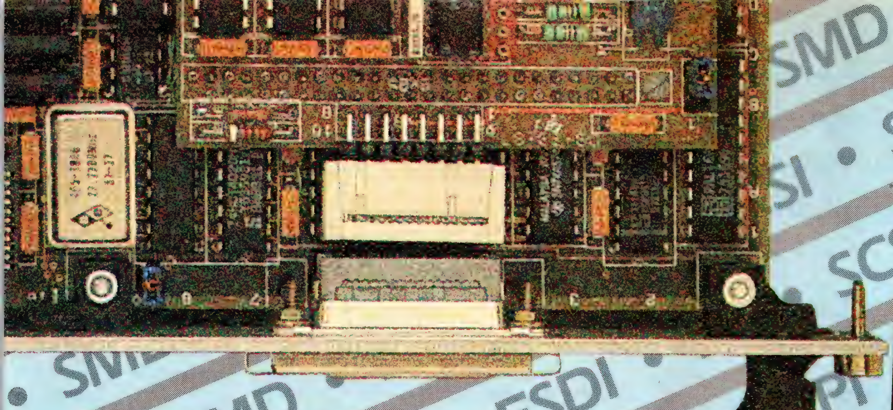


Fig 5—Loops, such as the connections between devices, *power planes, and other devices, are the source of EMI. Signal traces are more efficient radiators because of their larger areas. Long I/O cables are the best radiators but cause the most problems.*

When using bipolar devices, you generally place the capacitor at the ground end of the package to accommodate the greater sink-current capability of these devices relative to their source-current capability. The placement of the capacitor isn't as critical for advanced CMOS devices because they have equal sink- and source-current capability; even so, as a general rule, place the capacitor near the ground end. Locating the capacitor here helps to keep the ground quieter while sacrificing some V_{CC} noise. On boards with ground planes and V_{CC} traces, however, place the capacitor near the V_{CC} end.

Electromagnetic interference (EMI) is the noise created on a passive signal by the changing electric and magnetic properties of moving charge on an active signal. EMI-generated noise can be problematic in several ways. In digital systems, EMI-generated crosstalk can affect signal integrity. The passive signal can also radiate the EMI into the environment, creating more EMI. Analog designs are more susceptible to much lower levels of EMI-generated noise. EMI can also interfere with communications systems that rely on radiated energy, such as radio or TV transmissions. Regulating bodies such as the Federal Communications Commission (FCC) in the USA and the VDE in Europe have stringent regulations concerning the amount of EMI that's acceptable in consumer systems.

Where does EMI come from? Maxwell's equations indicate that current flowing in a loop generates both



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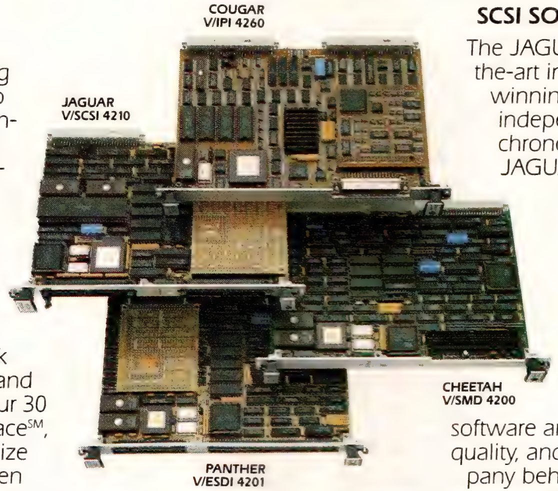

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CIRCLE NO 163

Loops in your design act like big antennae that radiate electromagnetic energy into the environment and induce current flow in nearby traces and wires.

magnetic and electric fields. These fields couple energy onto otherwise passive signals.

Signal characteristics of amplitude, period, duty cycle, edge rate, and ringing determine the frequency content of the signal. **Fig 6** shows the approximate relationship between the signal in the time domain (a) and the signal in the frequency domain (b). A signal that has a period (T), a pulse width of T_d, and an edge rate of T_r will have a frequency spectrum that starts at $F_0 = 1/(c \times T)$. The amplitude of the frequency-domain energy is a function of the amplitude and the duty cycle of the signal. The rest of the spectrum will be harmonics of this fundamental frequency (F_0). **Fig 6** shows the envelope of these harmonics. The three frequencies (F_0, F_1, and F_2) related to the period, duty cycle, and edge rate, respectively, determine the rolloff of the energy content in the frequency domain. Note that as you use faster technologies and system frequencies increase, the three important frequencies (F_0, F_1, and F_2) also increase, generating more energy in the high-frequency end of the spectrum.

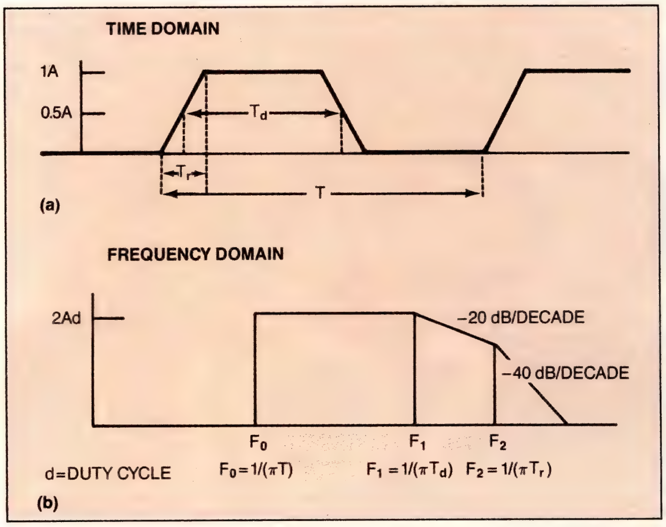

Fig 6—A signal can be represented in either the time domain or the frequency domain. *F_0, F_1, and F_2 are related to the signal period, duty cycle, and slew rate, respectively. They determine the envelope of the energy content in the frequency domain.*

The amount of energy the circuit radiates is determined by the size of the current loop and by the frequency content of the signal. Energy radiation is directly proportional to antenna size. Antennae are most efficient when the wavelength is equal to the antennae size; lower efficiency results when the wavelength is greater than the antennae size. The lower the frequency (and the higher the wavelength), the less efficient the radiation of energy.

Current loops contain signal traces, V_{CC} and ground connections, and I/O cables. A typical loop consists of the device connection from V_{CC} or ground to the output pin, the signal trace, and the V_{CC} or ground return connection. Generally, you should be concerned with the larger current loops. These large loops include long signal traces such as data or address buses, and long I/O cables. Most out-of-specification EMI results from poorly designed I/O cables.

EMI reduction techniques

Even though both system constraints and logic technology determine the signal characteristics, you can use a number of techniques to minimize EMI. The golden rule for EMI reduction is that anything that reduces noise in a system generally reduces radiated energy. Noise is a source of EMI that's typically rich in high-frequency harmonics.

A low-EMI design begins with power and ground. If a device's power and ground aren't clean, it's impossible to achieve clean output signals. Good power-supply design and decoupling techniques are important to ensure the performance of the device, and they're essential to good EMI design.

On the other hand, poor power- and ground-distribution networks can be major sources of EMI. V_{CC} and ground networks can be very inductive, so they tend to ring when excited. This ringing can couple onto the active signals, creating noise on them. Any generated V_{CC} or ground noise also couples onto quiet outputs within the same package. Further aggravating the problem are devices in proximity to the one that's switching. These nearby devices may also experience V_{CC} or ground noise; the noise then couples onto their outputs, creating still more EMI. Using power and ground planes reduces the amount of V_{CC} or ground noise when a device is switching.

In addition to keeping V_{CC} and ground cleaner, decoupling capacitors also minimize the energy radiated by V_{CC} and ground planes. Switching creates a large current disturbance in either V_{CC} or the ground plane; the larger an area that the disturbance covers, the greater the amount of energy radiated. Decoupling capacitors act to locally source or sink current, minimizing the disturbed area on the plane. These "local supplies" minimize the amount of radiated energy by reducing the antenna area. Again, if the capacitor has a large inductive value, then its effect will be attenuated.

Normally, you place large decoupling capacitors

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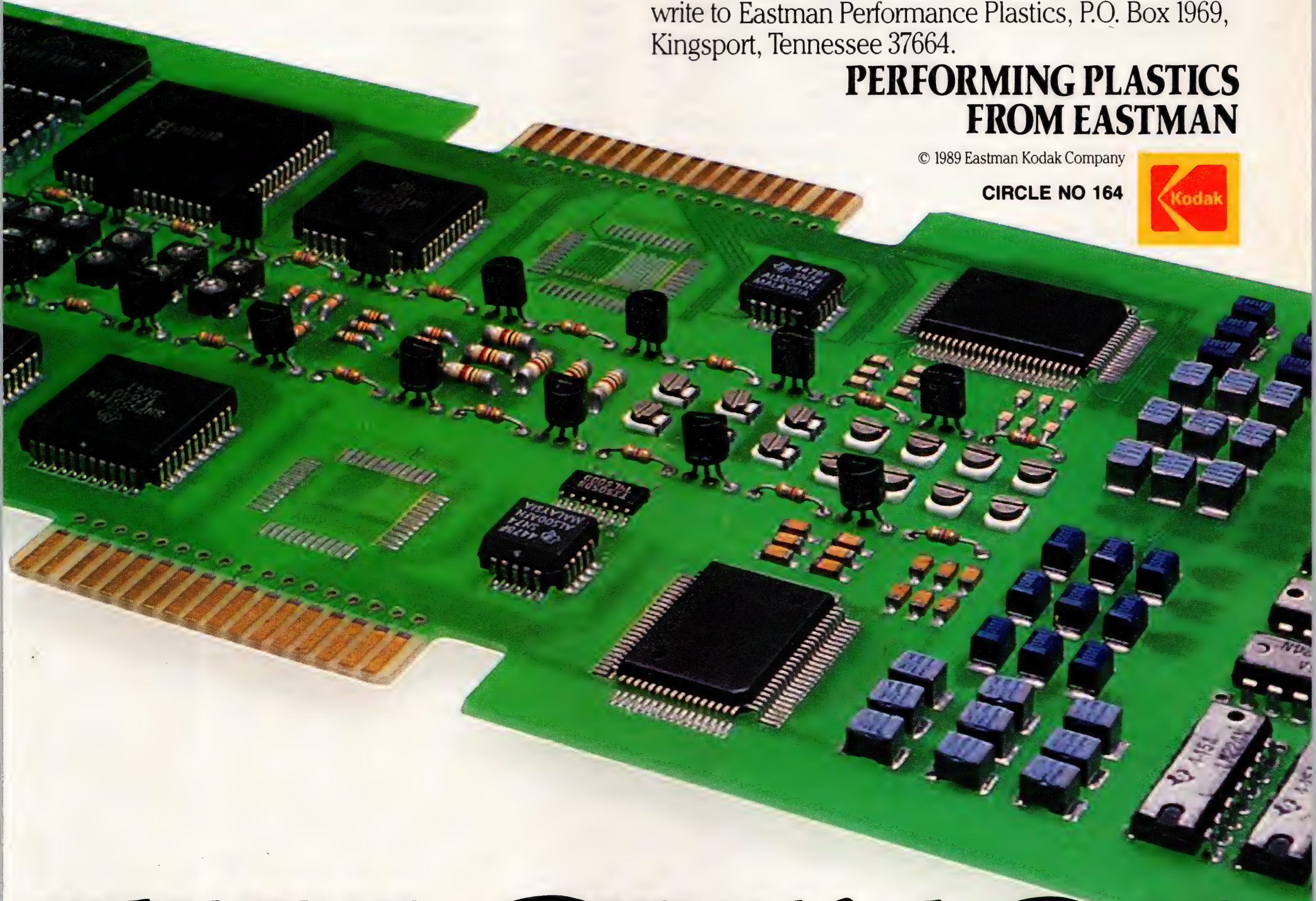

THE CITY OF THE FUTURE

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High-impedance power-supply networks won't supply the current you need to quickly switch high-speed circuits.

where power enters the board, and then you place smaller capacitors—typically in the 0.01- to 0.047-μF range—throughout the board. Studies show that you can reduce EMI emissions by increasing the capacitor values distributed around the board and by reducing the large capacitors near the power connections.

For EMI reduction, use 0.1- to 0.047-μF capacitors for decoupling every advanced CMOS device; use 1- to 10-μF capacitors for decoupling the board at the power connections. Since all of these capacitor values are available in surface-mount packages, you can use these values on both through-hole and surface-mount boards. Surface-mount components always help minimize radiated energy by reducing the net radiating area of the current loops.

High-impedance connections to the power supply can generate power rail noise. An example of a poor power connection is the daughter-board connection on a backplane. When designing plug-in boards where the V_{CC} and ground connections may have greater impedance, maximize the number of these connections. To maintain clean power connections throughout the board, allocate unused connections to power and ground. If power is supplied to your board through wires, it may be advantageous to use twisted-pair wires, or even an EMI choke, on the board. Power-supply cables tend to carry high current transients that, if not properly handled, can create EMI problems.

Beware when using sockets

Using sockets on a board can create additional noise and EMI, because most sockets are highly inductive. Using them increases the V_{CC} and ground noise exposure of the socketed device. The extra inductance in the power connections increases the ringing when the outputs switch. If you must use sockets, use the low-profile pin type. These sockets have the lowest inductance of any socket and will minimize the noise that they create.

The above discussions are particularly important for devices that generate signals that can leave the system. Exercise care to ensure that these devices have the best possible power and ground connections. Locate these external-signal-generating devices as close to the power supply or connection as possible.

Noise coupled onto other traces and reradiated can generate EMI. The most common form of coupling is crosstalk. Crosstalk isn't normally discussed with EMI, but EMI does generate it. The procedures that minimize crosstalk also minimize EMI.

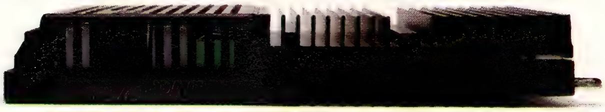
EMI is especially troublesome when the passive (listening) line exits the enclosure. These exiting lines

TABLE 1—ADVANCED CMOS DESIGN GUIDELINES

DESCRIPTION	CROSSTALK	INTERNAL RAIL NOISE	POWER-DISTRIBUTION NOISE	EMI
USE OUTPUTS CLOSE TO GROUND FOR ASYNCHRONOUS OUTPUTS		X		
RUN TRACES PERPENDICULARLY ON ADJACENT LAYERS	X			X
KEEP COUPLED LENGTHS LESS THAN L_{MAX}	X			X
SHIELD ASYNCHRONOUS TRACES	X			X
AVOID WIRE WRAP ON LONG BACKPLANE ASYNCHRONOUS SIGNALS	X			X
SEPARATE ANALOG TRACES	X			X
USE POWER PLANES	X	X	X	X
AVOID WIRE WRAP	X			X
AVOID SOCKETS		X		X
USE DECOUPLING CAPACITORS		X	X	X
USE TERMINATION	X			X
KEEP I/O TRACES SHORT	X			X
MINIMIZE TRACE LENGTH	X			X
MINIMIZE POWER IMPEDENCE			X	X
KEEP SYSTEM BOXES TIGHT				X

Time To Market

Time to market... the span between inspiration and product introduction. You want the shortest path to a successful product launch — but all too often the system power supply becomes a stumbling block . . . development delays, safety agency approvals, EMI/RFI testing, size problems, cooling issues, cost overruns, last minute changes in power requirements, manufacturing disasters...no matter how innovative your product, you know that your customer's satisfaction — and your market opportunity — may ultimately hinge on how well your "custom" power system holds up.



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create most EMI problems, because they're typically long and unshielded. Always keep the length of exiting traces as short as possible. Try to place the device generating the signal close to the exit point. Also, keep these lines away from high-speed digital lines. If necessary, use ground traces as shields between the signal exiting the system and the nearby, high-speed digital lines. Also, try to place components to minimize the number and length of all traces.

EMI consultants suggest that I/O cables cause most EMI problems, so you should build the cables carefully. The slew rate and signal frequencies of I/O signals should be as low as possible. Use shielded cable if you must run high-speed digital signals out of an enclosure. Ideally, you'd use coaxial cable, but unfortunately, coaxial cable is too expensive and bulky for systems with high I/O counts.

One alternative to coaxial cable is shielded ribbon cable, which takes up less space and provides more signal connections per dollar, and the shield around the cable effectively reduces EMI. If you must use unshielded ribbon cable, try alternating active signal lines with ground lines to reduce EMI. Approach I/O cable design with caution. The cost of retrofitting correct EMI deficiencies could outweigh the savings of using a less expensive cable system.

The design of the shield ground is also critical. If the shield isn't grounded to a good chassis ground, then the shield might become one big radiator. The shield connection must also be a good RF connection; one small wire from the cable shield to the chassis isn't a good RF connection. Expose the shield material all around the cable, and solder it directly to the chassis ground. Any void in the shield connection acts like an antenna and radiates energy.

Openings in enclosures are trouble spots

Be careful when designing the system enclosure. Openings radiate energy much like an antenna does. Obviously, some openings—such as access doors and vent openings—are always required, but you should shield them to minimize escaping EMI. Use wire mesh with small ventilation holes to minimize EMI. For access openings or enclosure joints, metal gaskets can form a tight EMI seal.

Although many designers think of EMI attenuation as black magic, the techniques for minimizing EMI are actually well known, and most systems utilize them. These same guidelines minimize internal switching noise, output ringing, crosstalk, and other high-performance noise conditions. Generally, minimizing extraneous system noise helps to minimize EMI.

Using advanced CMOS devices requires more attention to noise-reducing techniques than older, lower-performance technologies such as HC (High-performance CMOS) or LS (Low-power Schottky). However, advanced CMOS logic is as easy to use as high-performance, bipolar technologies such as AS, ALS, and FAST.

In addition, many of the aforementioned guidelines apply to more than one type of noise abatement. **Table 1** summarizes many of the design techniques you can use to limit noise and identifies the type of noise that each technique affects.

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Author's biography

William Hall is the marketing manager for Advanced CMOS products at National Semiconductor's Digital Logic Div. Bill directs new-product development and is responsible for marketing communications and field training for the FACT product line. He has a BSEE from Drexel University and relaxes by golfing and fishing.

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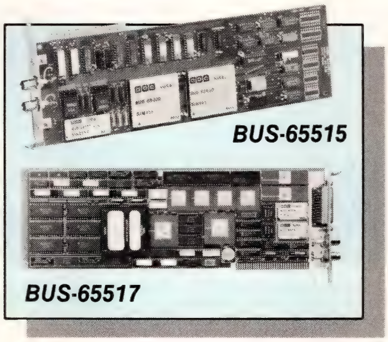

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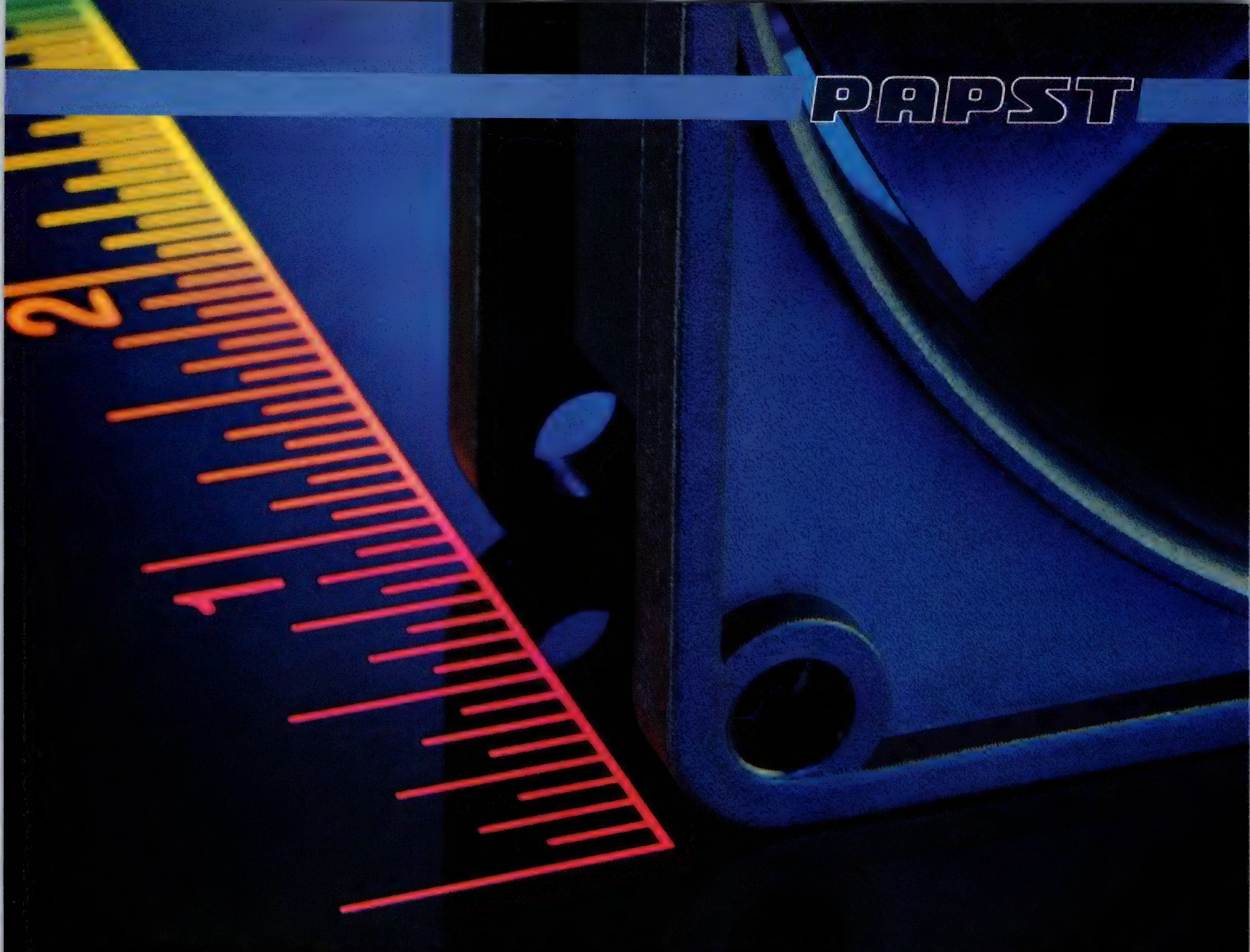

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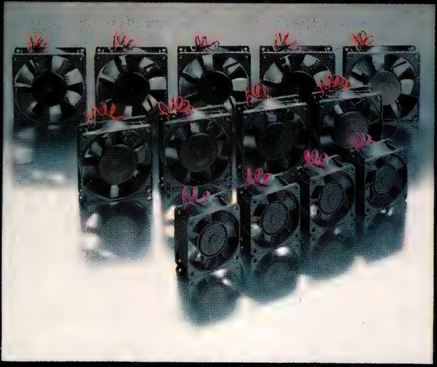

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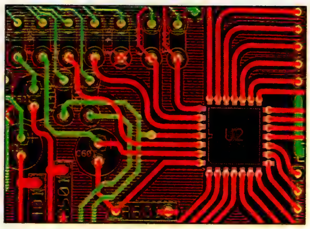

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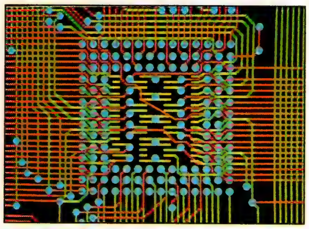

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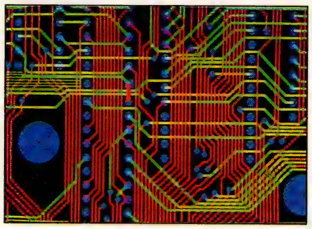

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CIRCLE NO 170

Hands-on experience paves the way for future MCA designs

The advent of the IBM Micro Channel Architecture (MCA) represents performance and architectural improvements compared with the earlier PC/AT bus. But designing for the PS/2 is a tougher challenge than designing for the PC/AT: MCA add-in cards must achieve higher performance and provide additional features while using less pc-board real estate.

Tom Darbonne, Vinita Singhal, and Mike Webb,
Altera Corp

IBM Personal System/2 (PS/2) personal computers have a new bus for add-in cards called the Micro Channel Architecture (MCA) bus. This bus works with 16- and 32-bit processors, as well as 8-, 16-, and 32-bit peripherals. It includes a welter of new features such as high-performance multidevice bus arbitration, level-sensitive interrupts, and no jumpers or DIP switches for selecting options.

This article first describes the differences between the PS/2 and the PC/AT, including detailed descriptions of the design requirements for the new MCA features. It then goes through a sample design and concludes with a designer's tips section filled with things that you can't learn from IBM's documentation alone and that were derived from actual, sometimes painful, hands-on experience with various MCA-based personal computers from IBM.

The PS/2's MCA bus has four major differences from the PC/AT bus, all of which affect your add-in cards' design:

- Physical card changes including size, mechanical specifications, and specialized connectors for certain types of add-in cards
- Software-controlled registers that replace DIP switches and jumpers for configuring the card and selecting options and are called POS (programmble option select) registers by IBM
- A more sophisticated DMA-arbitration scheme to allow multimaster operation
- Enhanced performance via 32-bit bus cycles for those PS/2s with 32-bit CPUs.

MCA physical characteristics

MCA cards—or "adapters," as IBM calls them—are significantly smaller than PC/AT bus cards: 33 vs 55.4 in.^{2} of usable area. This is roughly a 40% reduction in board real estate (**Fig 1**). In addition, because MCA bus timing is more critical, IBM specifies the locations of the bus-interface components so that they will be close to the bus connector to ensure short circuit-board lands. IBM also specifies the location for parts with significant power dissipation to ensure proper cooling.

The PS/2's MCA bus has four major differences from the PC/AT bus, all of which affect the design of your add-in cards.

Further, the MCA specification requires that your MCA card have power and ground-plane layers to minimize system and radiated noise.

The MCA specification permits 8-, 16-, or 32-bit connectors. Thus, you can plug 8-, 16-, or 32-bit cards into an MCA mother board. Additionally, the 8- and 16-bit connectors may have a video extension, which lets an adapter control the video port. Plus, 32-bit adapters may have a matched-memory extension, which directly connects an add-in memory and the system microprocessor for certain PS/2s, such as the Model 80 (see **Fig 2**). Your add-in card can have an 8-, 16-, or 32-bit bus.

Option selection and configuration

PC/AT add-in cards use jumpers and switches for configuring the cards, which leads to frequent confusion when configuring a system. The PC/AT static configuration methods sometimes lead to hanging the system when address conflicts arise among add-in cards. The MCA replaces conventional jumpers and switches with well-defined programmable registers for the add-in cards' feature settings.

POS registers reside at I/O addresses 0100_{HEX} through 0107_{HEX} on each add-in card, and IBM suggests standard uses for many of these register bits. Other objectives of the POS scheme are to permit the installation of multiple identically featured cards, to positively identify any card by slot, and to resolve resource-assignment conflicts.

Each add-in card type must have a unique 16-bit identification number. Each adapter identification number requires two read-only registers at addresses 0100_{HEX}, for the low-order byte, and 0101_{HEX}, for the high-order byte, on every card. IBM suggests the following uses for adapter identification numbers: 0000_{HEX}, device not ready; 0001_{HEX} to 0FFF_{HEX}, bus master; 5000_{HEX} to 5FFF_{HEX}, DMA devices; 6000_{HEX} to 6FFF_{HEX}, direct program control or memory mapped; 7000_{HEX} to 7FFF_{HEX}, storage or multifunction cards; 8000_{HEX} to 8FFF_{HEX}, video.

Multimaster operation

The MCA coordinates multiple bus masters with a distributed bus-arbitration scheme. Any resident subsystem can compete to share or control the bus. The PS/2 mother board effects MCA arbitration through circuitry that IBM calls the central arbitration-control point (CACP). The CACP resolves all requests for system control via three signals: ARB/−GNT, −PREEMPT, and −BURST. During arbitration, the highest priority adapter wins the next bus cycle. Only one adapter may be at a given arbitration level.

Add-in cards on the MCA bus can be non-DMA bus slaves, DMA slaves, or bus masters. The interface requirements for a bus-master adapter on the MCA are a superset of those required by a DMA bus slave (**Fig 3** shows default cycle timing). A bus slave can supply data to or receive data from a given bus only under the control of a bus master. Conceptually, you can have more than one bus slave on a given add-in adapter provided you incorporate the appropriate addressing and control for the multiple slaves. Examples of common bus slaves are add-in memory cards and low-to-medium-performance peripheral cards.

Whereas a bus slave uses address and control lines from the bus purely as inputs, a bus master drives these signals to execute independent transfers of data across the bus. Bus-master cards do not have to wait for service from another master and can initiate and complete transfers more quickly than slaves. However,

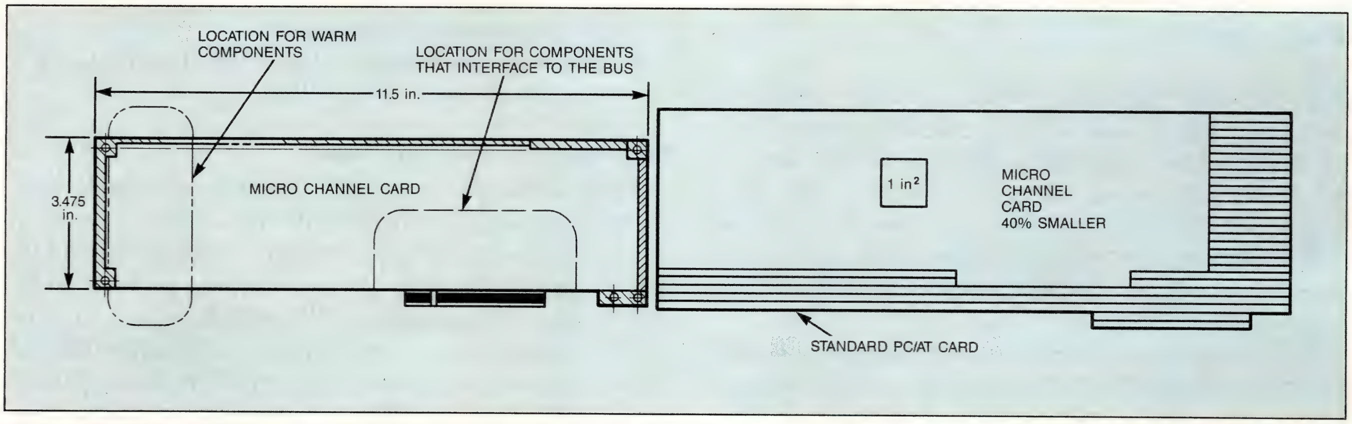
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***Fig 1—Micro Channel Architecture cards** are significantly smaller than PC/AT bus cards.*

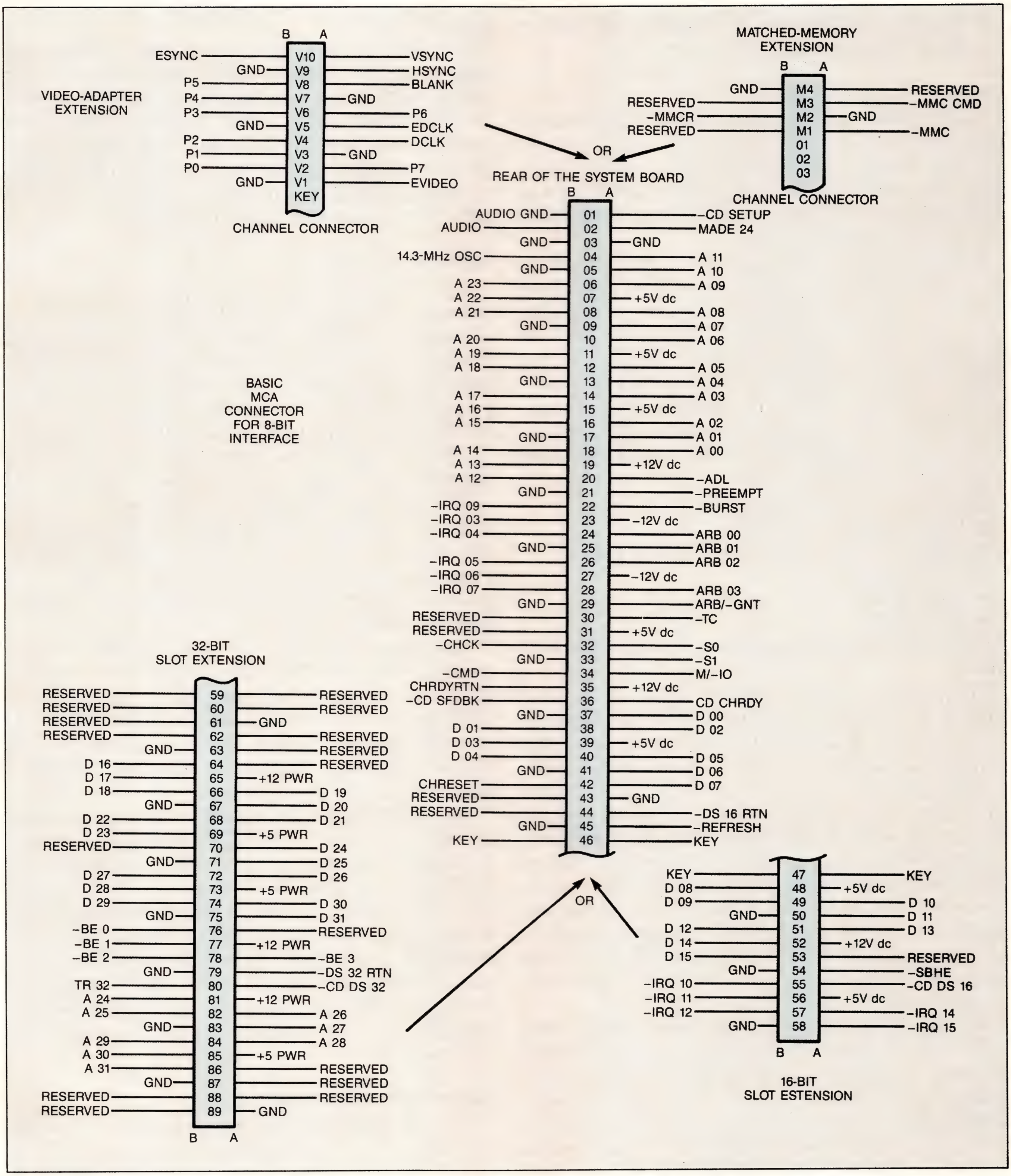


Fig 2—Your MCA add-in adapter can *have an 8-, 16-, or 32-bit bus plus a video-adapter or matched-memory extension.*

Because the MCA specification permits 8-, 16-, or 32-bit connectors, you can plug 8-, 16-, or 32-bit cards into an MCA mother board.

bus-master peripheral cards are usually more complex and costly than bus slaves.

Enhanced bus performance

The simplest way to increase a computer's throughput is to widen the width of its data bus. In the PC era, this widening has happened twice: first by going from the 8-bit 8088 bus to the 16-bit 80286 bus and more recently in moving to 32-bit buses using the 80386 and now the 80486 processors.

Because IBM PCs use only Intel μPs, some of the MCA specs reflect the peculiarities of these parts. Intel μPs have both memory- and I/O-address space. The μPs use an $M/\overline{IO}$ control line to distinguish between these two memory spaces. The MCA also has this dual address space and an M/−IO bus line. The MCA supports 8-, 16-, and 32-bit data transfers across the bus, depending on the system's and add-in cards' capabilities. The MCA handles 32-bit addresses and data with these additional signals:

- A_{24} to A_{31}—upper address bits
- D_{16} to D_{31}—upper data bits
- $-BE_0$ to $-BE_3$—byte-enable control signals
- −CD DS 32(n)
- −DS 32 RTN
- TR 32 RTN.

Note: (n) indicates that each bus slot has its own such line.

You'll need a 32-bit data-bus interface for your adapter to achieve the maximum MCA data-transfer rates. However, a basic problem of aligning data arises in a system that has a mix of 8-, 16-, and 32-bit cards. Ideally, the hardware should properly and transparently align data transfer between any two cards to the applications software. For example, a 16-bit disk-controller card should properly transfer data to a 16- *or* 32-bit memory card with no changes in the disk-controller driver's software. The PS/2 incorporates an address-bus translator and data-bus steering logic to solve this data-alignment problem. Otherwise, the MCA bus would not be able to use its full bandwidth during all transfers.

An MCA bus cycle to an adapter uses −CD DS 16(n) plus −CD DS 32(n) signals to indicate whether the adapter's data width is 8, 16, or 32 bits. Each adapter slot has its own set of these lines, and the particular adapter drives them when appropriate (**Fig 2**). If neither signal becomes active during the cycle, then the bus master knows it's communicating with an 8-bit adapter. If both signals are active, a 32-bit adapter is present.

You generate these signals as unlatched address decodes of the port locations found on your adapter. Your design must drive the appropriate −CD DS signals to their correct states within 60 nsec of receiving a valid address from the MCA bus. This interval gives the central bus-control logic on the mother board time to detect the adapter's bus-width signals and respond with the most efficient data-transfer cycle.

Odd-aligned transfers

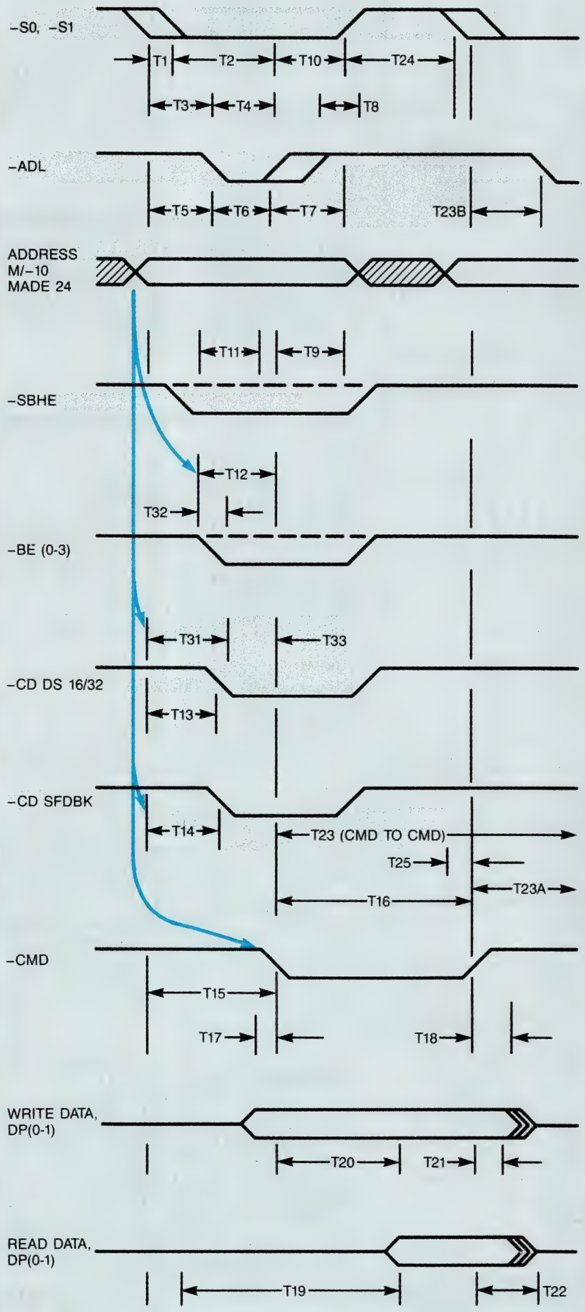
Intel μPs have signals to coordinate "odd-aligned" transfers—for example, transferring 16-bit data to an odd memory address. These signals perform the same functions on the MCA bus (see the Intel 80386 data sheet for details). To correctly align a data transfer on the MCA bus, a bus master must assert the correct set of byte-enable control lines, which are −BE(0-3), A_0, A_1, and −SBHE. Be aware that the 16- and 32-bit adapters you design should decode A_0, A_1, and −SBHE to indicate which bytes are being read and written. PS/2 personal computers having 286 and 386 μPs generate the −SBHE signal. You access 32-bit adapters, on the other hand, by using −BE(0-3) to generate the control signals for the 32-bit adapters' four, 8-bit data transceivers.

For example, consider the case of a 16-bit master trying to write to a 32-bit adapter. The master's problem entails accessing D_{16} through D_{31}, which only 32-bit CPUs normally use, then generating −BE(0-3) to select which bytes to transfer. Steering logic on the PS/2 mother board solves the problem of accessing the upper data bytes for the 16-bit master.

The steering logic automatically transfers the master's D_0 to D_{15} data on the MCA bus's D_{16} line through D_{31} lines if the address corresponds to a high-order word ($A_1 = 1$) and the TR32 signal is not active, that is, a 16-bit master has control. The address translator on the mother board also solves the second part of the problem by generating −BE(0-3). Logic on the mother board translates the A_0, A_1, and −SBHE signals into the appropriate combination of −BE(0-3) signals. The mother board's logic performs similar translations for 8-bit masters.

Add-in-card design example

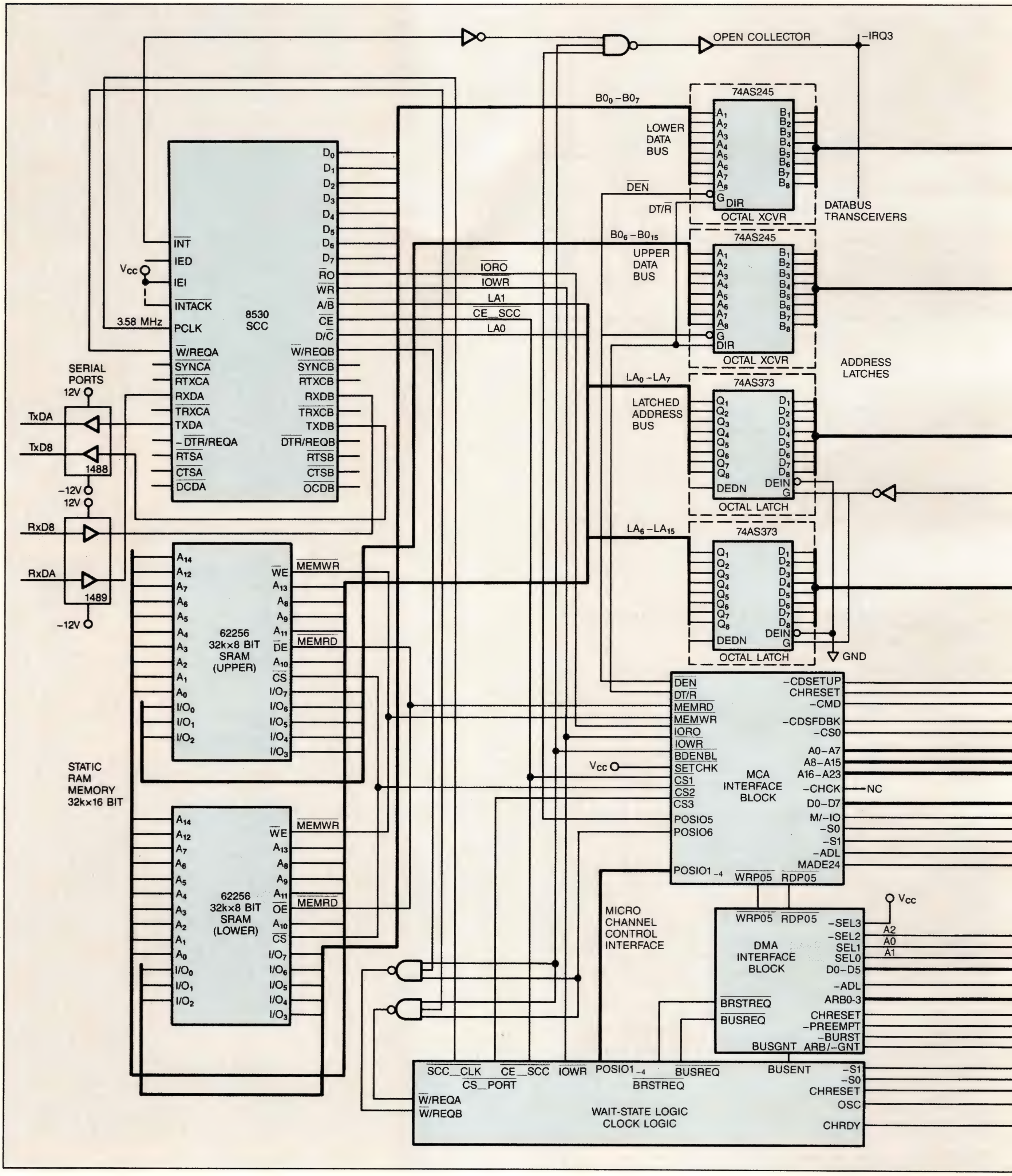
A real design is one of the best ways to clarify a new bus structure. A multifunction card is a good MCA design example because such a card is a popular add-in for personal computers and illustrates interfaces to

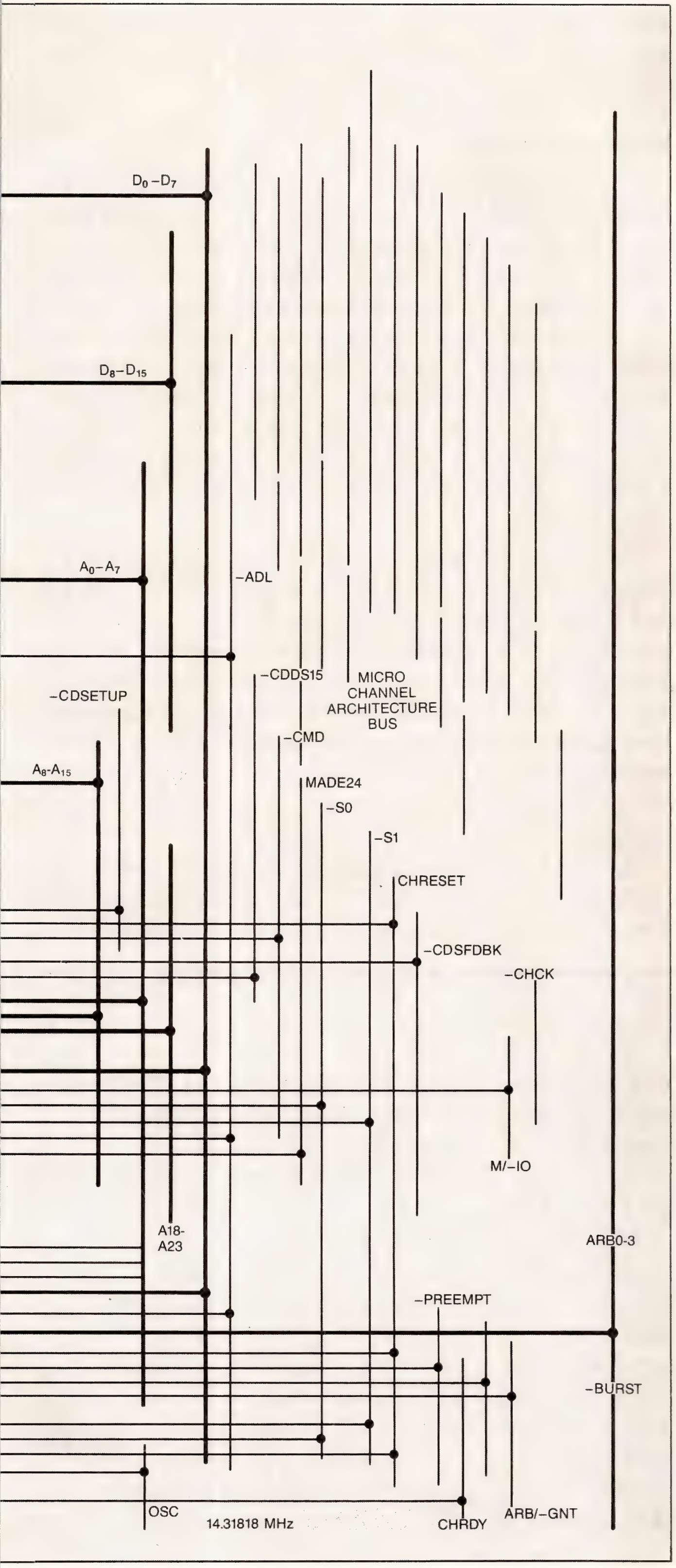


	TIMING PARAMETER	MIN/MAX
T1	STATUS ACTIVE (LOW) FROM ADDRESS.M/-10.-REFRESH VALID	10 / — NSEC
T2	-CMD ACTIVE (LOW) FROM STATUS ACTIVE (LOW)	55 / — NSEC
T3	-ADL ACTIVE (LOW) FROM ADDRESS.M/10.-REFRESH VALID	45 / — NSEC
T4	-ADL ACTIVE (LOW) TO -CMD ACTIVE (LOW)	40 / — NSEC
T5	-ADL ACTIVE (LOW) FROM STATUS ACTIVE (LOW)	12 / — NSEC
T6	-ADL PULSE WIDTH	40 / — NSEC
T7	STATUS HOLD FROM -ADL INACTIVE (HIGH)	25 / — NSEC
T8	ADDRESS.M/-10.-REFRESH.-SBHE HOLD FROM -ADL INACTIVE	25 / — NSEC
T9	ADDRESS.M/-10.-REFRESH.-SBHE HOLD FROM -CMD ACTIVE (LOW)	30 / — NSEC
T10	STATUS HOLD FROM -CMD ACTIVE	30 / — NSEC
T11	-SBHE SETUP TO -ADL INACTIVE	40 / — NSEC
T12	-SBHE SETUP TO -CMD ACTIVE	40 / — NSEC
T13	-CD DS 16/32 ACTIVE (N) (LOW) FROM ADDRESS.M/-10.-REFRESH VALID	— / 55 NSEC
T14	-CD SFDBK ACTIVE (LOW) FROM ADDRESS.M/-10.-REFRESH VALID	— / 60 NSEC
T15	-CMD ACTIVE (LOW) FROM ADDRESS VALID	85 / — NSEC
T16	-CMD PULSE WIDTH	90 / — NSEC
T17	WRITE DATA SETUP TO -CMD ACTIVE (LOW)	0 / — NSEC
T18	WRITE DATA HOLD FROM -CMD INACTIVE (HIGH)	30 / — NSEC
T19	STATUS TO READ DATA VALID (ACCESS TIME)	— / 125 NSEC
T20	READ DATA VALID FROM -CMD ACTIVE (LOW)	— / 60 NSEC
T21	READ DATA HOLD FROM -CMD INACTIVE (HIGH)	0 / — NSEC
T22	READ DATA BUS 3-STATE FROM -CMD INACTIVE (HIGH)	— / 40 NSEC
T23	-CMD ACTIVE TO NEXT -CMD ACTIVE	190 / — NSEC
T23A	-CMD INACTIVE TO NEXT -CMD ACTIVE	80 / — NSEC
T23B	-CMD INACTIVE TO NEXT -ADL ACTIVE	40 / — NSEC
T24	NEXT STATUS ACTIVE (LOW) FROM STATUS INACTIVE	30 / — NSEC
T25	NEXT STATUS ACTIVE (LOW) TO -CMD INACTIVE	— / 20 NSEC
T31	-BE(0-3) ACTIVE FROM ADDRESS VALID (32-BIT MASTERS ONLY)	— / 40 NSEC
T32	-BE(0-3) ACTIVE FROM -SBHE. A0. A1 ACTIVE	— / 30 NSEC
T33	-BE(0-3) ACTIVE TO -CMD ACTIVE	10 / — NSEC

Fig 3—The design example uses *this default timing.*

The MCA replaces conventional jumpers and switches with well-defined programmable registers for the feature settings of add-in cards.





both memory and I/O devices on the MCA bus. This example of a multifunction card includes 32k words of CMOS static RAM (SRAM) and a dual-channel serial controller. PLDs, or dedicated MCA-interface devices like the EPB2001 and EPB2002 (see **box,** "EPLDs integrate PS/2 MCA functions"), are one way to implement control interfaces between the MCA bus and a PS/2 feature adapter. However, this example treats the interface logic generically to help you make your own tradeoffs when selecting devices for your MCA bus-interface logic.

The block diagram in **Fig 4** shows the overall structure of the design. On the right are the MCA-bus lines, which run to all add-in card slots. The board's MCA-interface block **(Fig 5)** performs mandatory POS-register functions, which the MCA specification requires for all add-in cards. In addition, the MCA-interface block integrates board-control logic, board-identification-number storage, and address decoding. The DMA-interface block oversees DMA-arbitration **(Fig 6).**

This board appears to the PS/2 as either an 8-bit I/O peripheral for accesses to the 8530 serial communications controller (SCC) or as a 16-bit, 32k-word memory extension, depending on whether the PS/2 receives an I/O or memory access. The board's two 74AS245 data-bus transceivers buffer data transfers between the MCA bus and I/O or memory functions.

The board permits no byte accesses to memory—only 16-bit accesses. Consequently, you need not selectively enable the buffers using −SBHE. Two 74AS373 flow-through latches hold addresses during bus transfers. The −ADL line from the MCA bus controls the latching. −ADL needs to latch only the 16 low-order address bits because the board's memory capacity is only 64k bytes. The MCA-interface block's chip-select logic handles upper-order address decoding for the I/O and memory chips on the board.

MCA-interface block

In this application, the MCA-interface block is the primary control interface. This block contains the control logic for the MCA-bus interface, as well as logic for chip-select decoding and the POS registers. **Fig 5** shows the basic control-logic section. You can implement the POS registers and chip-select decoders in a variety of ways, ranging from discrete TTL or PAL

Fig 4—This multifunction card appears to *the MCA bus as either an extended memory or two serial I/O channels.*

The MCA coordinates multiple bus masters with a distributed bus-arbitration scheme in which any subsystem can compete to share or control the bus.

devices to special-purpose ICs.

As required for any MCA add-in, the MCA-interface block reserves two bytes at locations 0100_{HEX} and 0101_{HEX} for the board's identification number. These locations are read-only locations accessible from the MCA bus. These numbers are unique to a given board design, and IBM allocates them through its Independent Developers Assistance Program (IDAP) to registered independent developers. You can build these and other POS registers several ways, depending on your needs. Implementations of the MCA POS registers 0100_{HEX} and 0101_{HEX} range from read-write logic or register files to simple hard-wired registers.

The four other required POS registers, residing at 0102_{HEX} to 0105_{HEX} in this application, control I/O remapping, memory remapping, the number of I/O wait-states, DMA-request source selection and masking, interrupt masking, and DMA arbitration level and "fairness." Fairness is a feature of the MCA's DMA-arbitration procotol that prohibits high-priority adapters from monopolizing the MCA bus. The DMA-interface block needs the latter five POS register bits to control bus access. These five bits set the arbitration-priority level and fairness for the adapter, based on the values written into the bits at configuration time.

The board-control logic in the MCA-interface block provides all required data-bus transceiver-control signals, $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$), and I/O and memory-control strobes, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, $\overline{\text{MEMWR}}$, $\overline{\text{MEMRD}}$. The MCA-bus −CMD transfer strobe and the bus-cycle status lines trigger these signals. Thus, these MCA-bus signals directly drive the onboard read-and-write strobes.

Mute before boot

The board-enable output of the MCA-interface block, $\overline{\text{BDENBL}}$, masks DMA requests and interrupts prior to enabling the card at system-boot time. This output reflects bit 0 of POS register 0102_{HEX}. In addition, the MCA-interface block internally factors this bit into the $\overline{\text{CSx}}$-enable functions to disable chip selects when the board is disabled. This factoring also suppresses generating the −CD SFDBK signal prior to card setup because no adapter card can be active on the MCA bus and generate that signal before the main processor examines all add-in cards to ensure that no address conflicts exist.

The chip-select block in the MCA-interface block includes the chip-select outputs for the CMOS SRAM and the serial-communications controller. In addition, one of the $\overline{\text{CSx}}$ outputs drives the −CD DS 16 (card data size 16) output to the MCA whenever the MCA bus accesses the SRAM, which is organized as words. Because the card's memory is organized only as a 16-bit memory, the −CD DS 16 output is a nonlatched OR of the memories' chip selects. In this case, −ADL latches the first three chip-select outputs.

The −CD SFDBK (card-select feedback) line to the MCA bus is an unlatched OR of the appropriate chip selects. In this example, this signal incorporates all

EPLDs integrate PS/2 MCA functions

The Altera EPB2001 and EPB2002 are PS/2 interface devices implemented as CMOS erasable PLDs (EPLDs). The EPB2001 handles all essential interface functions between a PS/2 add-in card, or adapter, and the MCA bus. The EPB2002 provides optional DMA functions. Typically, you need no additional glue logic. The EPB2001 fits into the MCA-interface block, and the EPB2002 fits into the DMA-interface block, as shown in **Fig 4** of the text.

The EPLDs let you configure the interface's features. The devices replace 18 or more MSI/TTL and standard PAL devices. The 84-lead EPB2001 and 28-lead EPB2002 together occupy less than 2 in.^{2}. You can use them in tandem or independently.

The EPB2001 provides general-purpose interface features, such as POS registers 0100_{HEX} to 0105_{HEX}, including board identification numbers; access to POS register contents on adapter-accessible I/O lines; adapter address remapping via programmable chip-select logic; and board-control signals.

The EPB2002 offers DMA-arbitration features, such as arbitration-level POS bits, arbitration "fairness," burst and nonburst transfers, and executing the arbitration protocol. Pin-strapping options let you map the POS bits into any valid locations. When used in conjunction with the EPB2001, you need no additional components to fashion a DMA slave adapter's interface.

$\overline{\text{CSx}}$ functions, with the exception of −CD DS 16.

The address-remapping fields specified in the POS registers should control several predefined ranges for each of the board's chip-select signals. This scheme allows dynamic reassignment of any I/O or memory address during setup to avoid system-address conflicts. The computer's power-on self test (POST) in its BIOS routines automatically performs this configuration process each time the system boots. These configuration routines use an IBM-specified file, the ADF (adapter description file), which comes with every adapter, to properly handle this automatic system configuration. The IBM documentation in **Refs 1, 2,** and 3 contains detailed definitions of these files.

The design example's 8530 serial-communications controller (SCC) packs two serial channels in a single 40-pin device. The SCC needs no local oscillator. The MCA bus's OSC line furnishes a precise 14.31818-MHz clock. A divide-by-4 counter, which OSC drives **(Fig 7)**, derives a 3.58-MHz clock signal for the SCC.

The 8530's interface timing is straightforward: The 8530 requires that you set up $\overline{\text{CE}}$, D/$\overline{\text{C}}$, and A/$\overline{\text{B}}$ prior

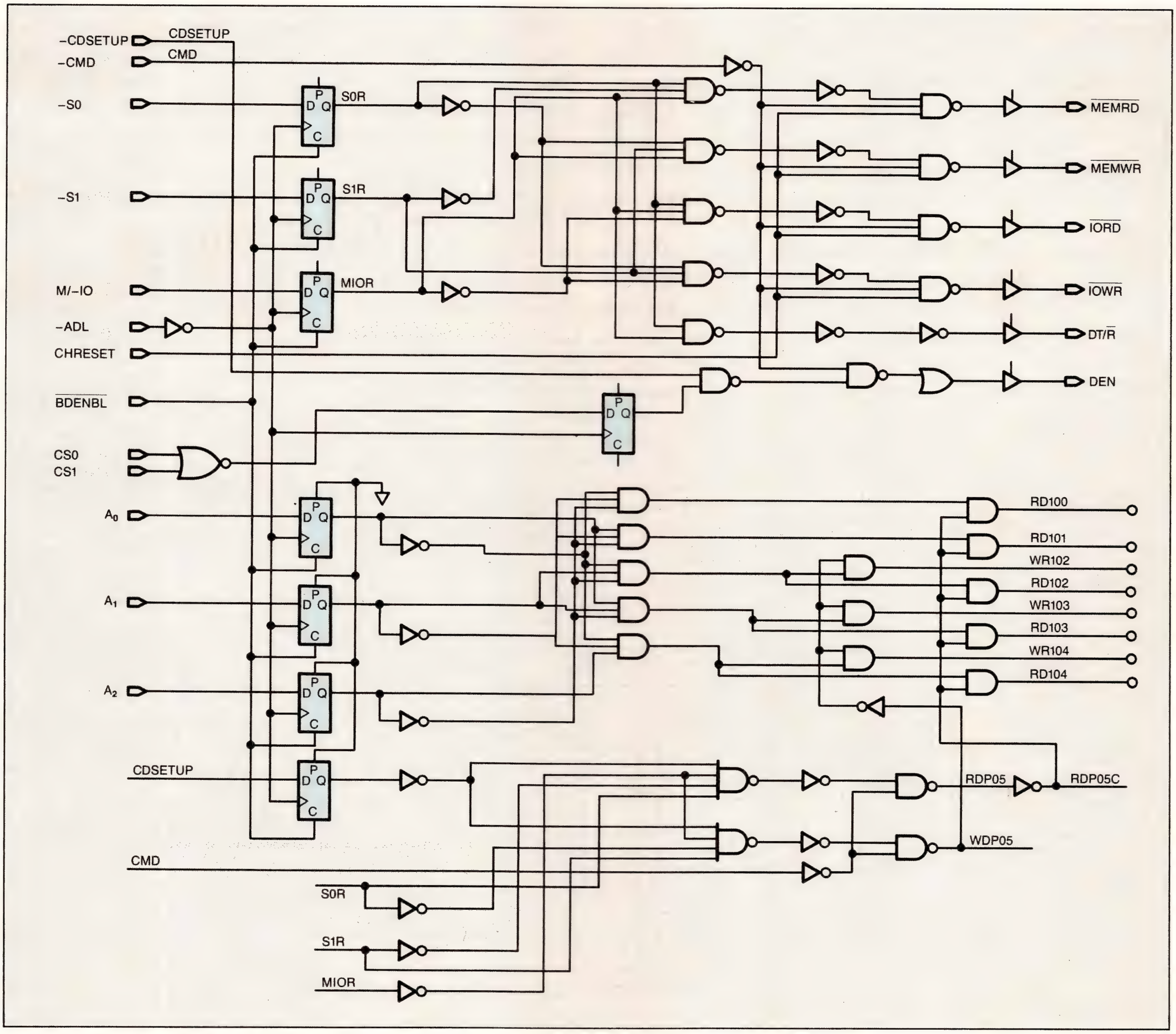


Fig 5—Fig 4's MCA-interface block *handles all the non-DMA transactions between the MCA bus and onboard devices.*

A real design is one of the best ways to clarify a new bus structure.

to either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ going active low. $\overline{\text{CE}}$'s setup time is 0 nsec; $\text{D}/\overline{\text{C}}$ and $\text{A}/\overline{\text{B}}$ have an 80-nsec setup time prior to their strobe's edge. All signals have a 0-nsec hold time for the rising (inactive) edge of the strobe. The setup time for data in a write cycle is 10 nsec preceding the active $\overline{\text{WR}}$ edge. In a read cycle, the 8530 supplies valid data on pins D_0 through D_7 within 250 nsec of the $\overline{\text{RD}}$ active edge.

Given this inherent timing, how do you make the SCC work with the MCA bus? In this design, the SCC's $\text{D}/\overline{\text{C}}$ and $\text{A}/\overline{\text{B}}$ inputs come from the latched inputs that the 74AS373 devices hold. The MCA guarantees a minimum setup time of 85 nsec from when addresses are valid on the MCA bus to when −CMD falls. Using 74AS373s, the delay from the MCA's input to the output, which is latched onto the board's local address bus, is only 5 nsec. The address is consequently valid at the 8530 more than 80 nsec before the strobe's edge because the −CMD line triggers the strobe by going active.

Further, the delay from addresses being valid on the A_0-A_{23} inputs until the adapter's MCA-interface block's $\overline{\text{CSx}}$ outputs become valid is 30 nsec. This last delay still results in the chip-select signal appearing 55 nsec before the 8530 requires it, thus leaving an ample timing margin in the $\overline{\text{CE}}$ path. The MCA-interface block latches the $\overline{\text{CE}}$ line with −ADL and holds it valid for the entire bus cycle.

Data-buffer operation

For both memory and the SCC's I/O operations, bidirectional data-bus buffers latch the data. The board's MCA-interface block begins latching operations within 20 nsec after MCA-bus signal −ADL goes active. The MCA-interface block first sets the direction of the data transfer with its $\text{DT}/\overline{\text{R}}$ line and then, within 20 nsec after $\text{DT}/\overline{\text{R}}$ falls, latches the data with its $\overline{\text{DEN}}$ line. The MCA-bus's −CMD signal gates either $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$. The MCA spec requires a minimum of 40 nsec from when −ADL goes active to when −CMD goes active.

The board's MCA-interface block must generate the $\overline{\text{DEN}}$ for the data-bus transceivers in 20 nsec. Allowing for a 9-nsec delay through the 74AS245 transceivers, data appears at the serial-communications controller inputs 11 nsec before the $\overline{\text{IOWR}}$ strobe occurs. This

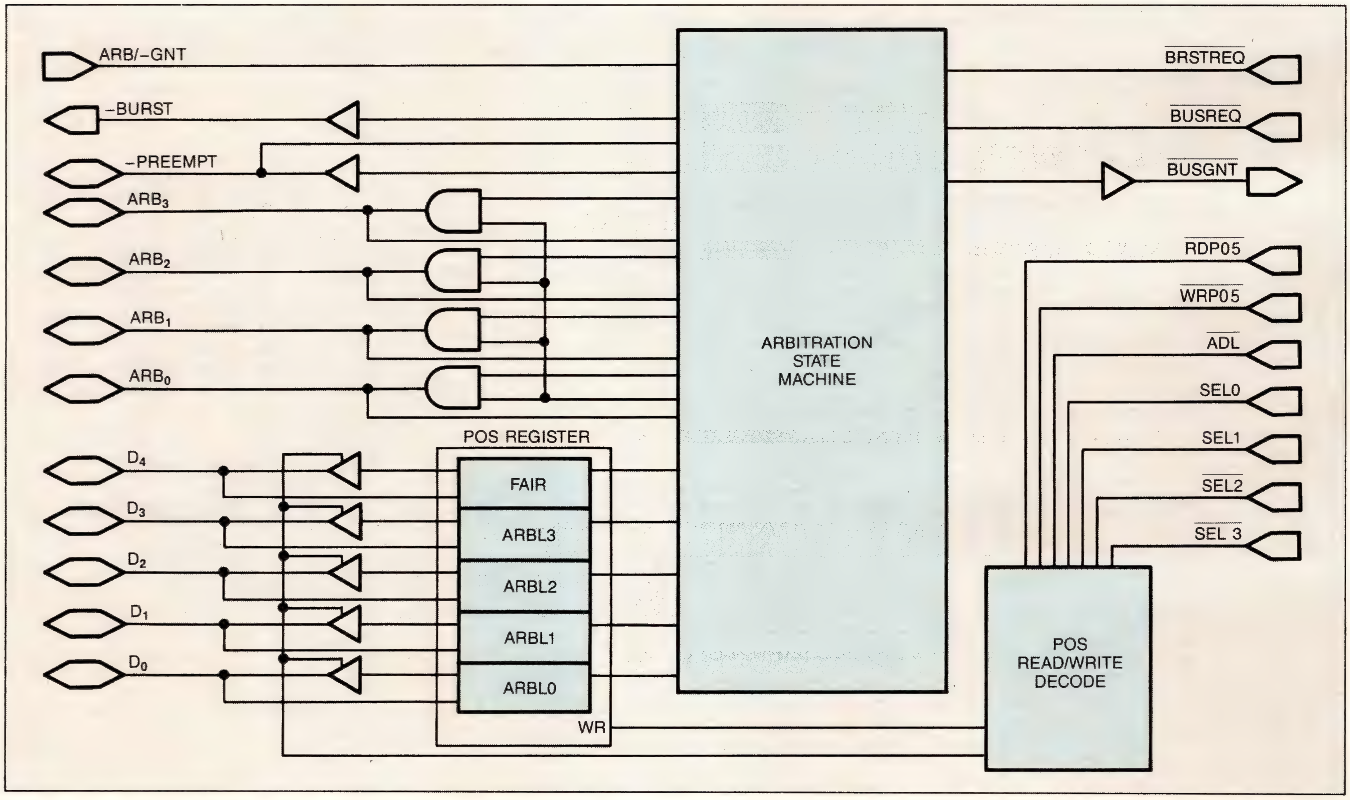


Fig 6—Fig 4's DMA-interface block *oversees DMA arbitration and DMA transactions.*

ADC603 10MSPS 12-Bit Sampling ADC

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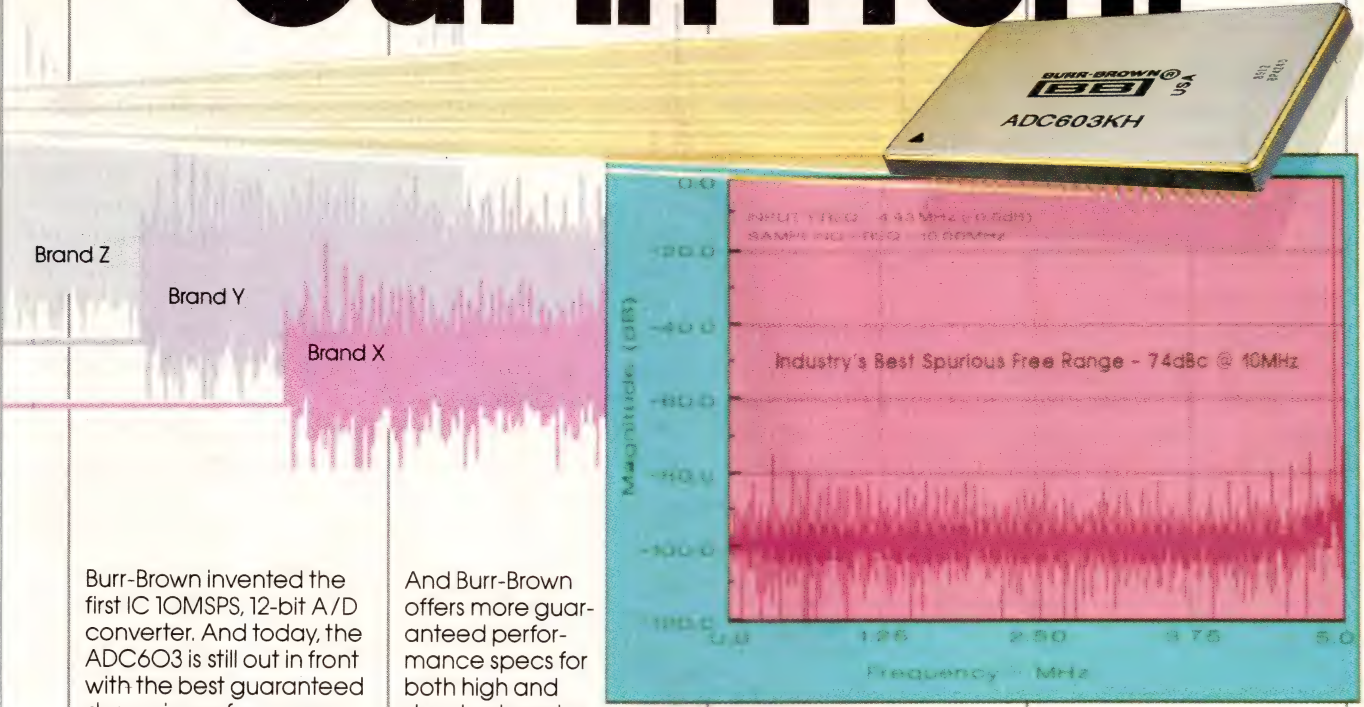

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You must follow IBM's syntax rules strictly because the system's error messages are terse and do not point specifically to syntax-rule violations.

timing meets the 8530's setup requirements.

The MCA specification requires that adapters' bus drivers go to the high-impedance state within 30 nsec after –CMD goes inactive. The 74AS245's 9-nsec delay coupled with the 20-nsec –CMD to $\overline{\text{DEN}}$ delay on the trailing edge matches the bus spec well.

Interrupt handling

For interrupts, an open-collector, 24-mA driver connects the SCC's $\overline{\text{INT}}$ output to the MCA bus's interrupt line –IRQ3. The MCA gives you a choice of several prioritized –IRQx lines. In this case, selecting the –IRQ3 line sets up the board's interrupt as the alternate serial port defined for the PS/2. This design treats interrupt acknowledgement as a standard I/O read-and-write operation without special timing.

The DMA-interface block implements the bus-arbitration protocol defined for the MCA in an asynchronous state machine (**Fig 8**). The DMA-interface block uses four of the five POS register bits to control the 4-bit arbitration level (priority) for the board. The fifth bit enables "fairness." This example uses POS register 0104_{HEX}, bit locations D_3 to D_7, to select DMA-arbitration level and fairness.

A POS-register bit selects which channel of the SCC is the DMA requestor. You can program the 8530 to

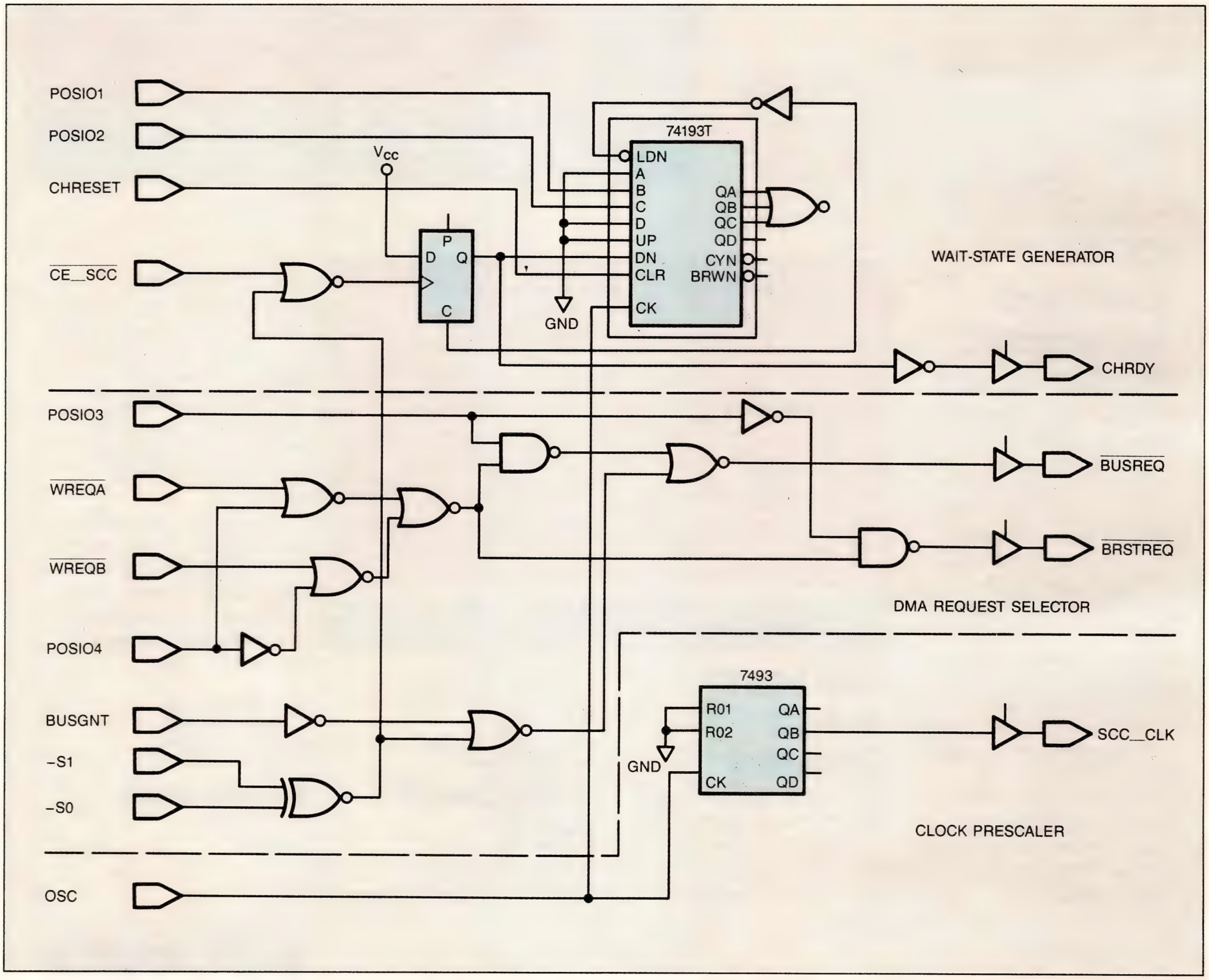

Fig 7—Because the MCA bus supplies a precise, *high-frequency clock signal, OSC, the wait-state generator and serial-communications controller need no onboard clock.*

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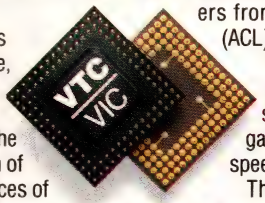

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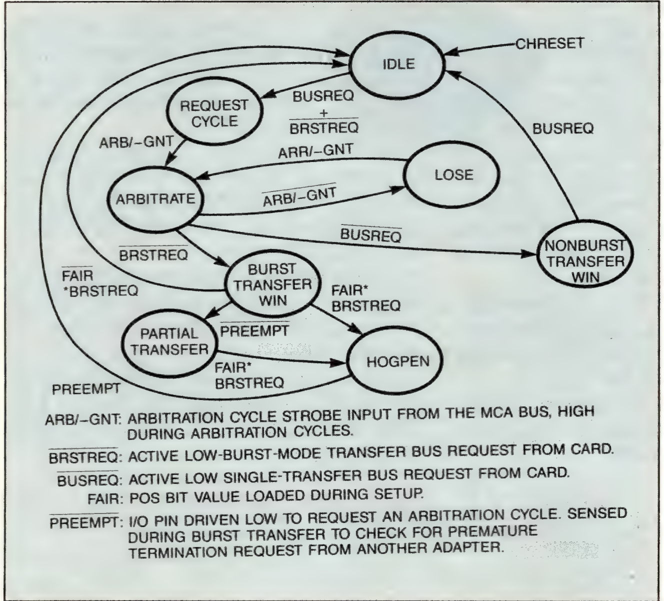
Because IBM PCs use only Intel µPs, some of the MCA specs reflect the peculiarities of these parts.

assert its interrupt signals, $\overline{\text{W}}$/REQx, on a character-received or transmit-buffer-empty condition. These signals go to either the DMA-interface block's $\overline{\text{BRSTREQ}}$ (burst transfer) or $\overline{\text{BUSREQ}}$ (nonburst transfer) inputs and result in the DMA-interface block asserting the MCA-bus signal −PREEMPT.

The board's wait-state generator must insert wait states in two cases. First, although timing for the serial-communications controller's interrupt assertion is not critical, timing for the removal of the request *is.* To properly terminate the cycle, −BURST must be inactive 35 nsec *before* −CMD rises. Therefore, to guarantee correct burst operation, the strobe's width, and therefore −CMD's active width, must be 360 nsec. To avoid DMA overruns (erroneous extra transfers), wait states must extend the DMA transfer cycle.

Second, the serial-communications controller requires an overall width for $\overline{\text{RD}}$ or $\overline{\text{WR}}$ of 250 nsec. Because the default MCA cycle allows only a 90-nsec −CMD width, a wait-state generator must extend these cycles.

The timing source for the wait-state generator **(Fig 7)**, which is the OSC signal from the MCA bus, has a period of about 70 nsec. The wait-state generator pulls CDCHRDY, a wait-state request signal, on the MCA bus inactive low for the number of OSC clock edges set by a value written into a POS register. The number of wait states can vary from 0 to 6. The actual wait-state generator consists of a loadable down-counter. The counter automatically reloads each time it reaches zero. While it is counting down, the counter holds CDCHRDY low.



ARB/−GNT: ARBITRATION CYCLE STROBE INPUT FROM THE MCA BUS, HIGH DURING ARBITRATION CYCLES.
$\overline{\text{BRSTREQ}}$: ACTIVE LOW-BURST-MODE TRANSFER BUS REQUEST FROM CARD.
$\overline{\text{BUSREQ}}$: ACTIVE LOW SINGLE-TRANSFER BUS REQUEST FROM CARD.
FAIR: POS BIT VALUE LOADED DURING SETUP.
$\overline{\text{PREEMPT}}$: I/O PIN DRIVEN LOW TO REQUEST AN ARBITRATION CYCLE. SENSED DURING BURST TRANSFER TO CHECK FOR PREMATURE TERMINATION REQUEST FROM ANOTHER ADAPTER.

Fig 8—This asynchronous state machine *determines whether the add-in board captures the bus for a DMA transfer.*

The 32k-word static RAM on the multifunction card comprises two 32k×8-bit CMOS SRAM devices: 100-nsec cycle-time 62256LP-10s. The memories' output delay from the occurrence of $\overline{\text{OE}}$ to the appearance of valid data is 50 nsec. The chips' specification for minimum write-enable strobe width ($\overline{\text{WE}}$) is 75 nsec, with a 40-nsec data-setup time from the $\overline{\text{WE}}$'s trailing edge. On the other hand, the MCA guarantees an 85-nsec setup time for addresses before the occurrence of −CMD. A 5-nsec delay through the 74AS373s still leaves more than 80 nsec of address-to-$\overline{\text{MEMRD}}$ or -$\overline{\text{MEMWR}}$ setup time for the SRAM devices. Even assuming a minimum strobe width of 90 nsec (the minimum −CMD width for the MCA), this timing allows 170 nsec of total address-access time for the SRAMs.

Of course, the 30-nsec chip-select decoding delay in the MCA-interface block reduces the total chip-select access time for the SRAMs themselves to 140 nsec. Because the output-enable delay of the SRAMs is 50 nsec—even with a 9-nsec delay through the 74AS245 transceivers—data is valid on the bus in time to meet the MCA's 60-nsec maximum-delay specification for read data.

The SRAMs require data to be valid for 40 nsec, overlapping $\overline{\text{WE}}$, to guarantee correct writing to the selected locations. The MCA specifies 0 nsec of write-data setup before the leading edge of −CMD as well as a minimum 90-nsec −CMD width. This timing results in 80 nsec of overlap—more than adequate even with the 9-nsec buffer delay.

Design tips

When designing the previous example, we discovered additional unpublished characteristics of the MCA. The following design guidelines summarize experience obtained during extensive debug work with several MCA-based machines and designs. These tips can help when you begin your own MCA add-in card design:

1. ADFs (adapter description files)—You must follow IBM's syntax rules strictly because the system's error messages, which it generates during configuration, are terse and do not point specifically to syntax-rule violations. For example, if you omit the "Help" field in a NamedItem structure, the BIOS flags a seemingly unrelated divide-overflow exception error. The ADF syn-

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When you design adapter cards, you must keep in mind that the mother board already uses certain I/O and memory addresses.

tax is not case sensitive.

The following notation refers to the POS registers in the ADF:

- POS[0] is the POS register located at I/O address 0102_{HEX}
- POS[1] is the POS register located at I/O address 0103_{HEX}
- POS[2] is the POS register located at I/O address 0104_{HEX}
- POS[3] is the POS register located at I/O address 0105_{HEX}.

IBM reserves bit 0 in POS[0] and bit 7 in POS[3] for card enable and −CHCK (channel check) functions; therefore, you must not write to them. You must specify the letter "X" in these bit positions in the ADF when specifying configuration data for POS registers 0 and 3 to avoid writing to those two bits.

2. The POST (power-on self test) in the Model 50 PS/2 writes a "0" to the −CHCK bit (POS[3], bit 7) even if the ADF specifies an "X" for that bit. This erroneous write could be a potential problem if an adapter implements −CHCK. You must, in this case, specify this bit as a "1" in your ADF for correct operation.

3. The following inconsistencies with setup (−CD SETUP (n)) cycles occur on the Model 50 PS/2:

- The length of the −CD SETUP (n) cycles varies for POS register read/write operations to the different POS registers.
- −CD SETUP (n) can become valid during a preceding bus cycle. A flow-through latch −CD SETUP (n) enabled by −CMD ensures that −CD SETUP (n) is recognized only between bus cycles when −CMD is high.

4. When you design adapter cards, you must keep in mind that the mother board already uses certain I/O and memory addresses. The technical-reference manuals for each PS/2 model detail these "reserved" addresses. These addresses can differ from model to model. I/O and memory space for an adapter designed on the basis of system I/O and memory maps for Models 50 and 60 need to be checked against those for Models 70 and 80. For example, in the system board I/O address map, I/O addresses $00E0_{HEX}$ and $00E1_{HEX}$, which do not appear on the Model 50 and 60 address maps, are reserved in Models 70 and 80. A potential bus-contention problem exists if your adapter uses these I/O addresses.

5. Status signals −S0 and −S1 become valid on the Model 50 at a different time than on Models 70 and 80. The time from status valid until −ADL goes active low is 12 nsec. IBM documentation shows no maximum specification for this interval. Observations of this timing parameter for the different systems are

- Model 50—40 to 50 nsec
- Model 70—60 to 70 nsec
- Model 80—60 to 70 nsec.

These measurements were made with a logic analyzer having a 10-nsec resolution.

These variations can directly affect any board-level timing, especially asynchronous timing, generated from a decode of valid −S0 and −S1 signals.

6. Master mode operation—Any controller responding to a slave request must allow 30 nsec before sampling −CD DS16, −CD DS 32, −CD SFDBK, or CD CHRDY if it places an address on the bus within 30 nsec after ARB/−GNT goes low. This 30-nsec interval allows the slave adapter time to generate an internal acknowledge that it has been selected—the DMA-interface block asserts BUSGNT in this case. −CMD can occur a minimum of 115 nsec after the master gives the address to the MCA bus.

7. The matched-memory cycle is a special type of 32-bit transfer available on some 80386 PS/2 machines. The matched-memory cycle's primary use is to expand the system RAM via the MCA bus. These cycles allow a fast transfer between the 80386 and MCA memory, which takes only three 16-MHz clocks (187 nsec) vs the normal four clocks (250 nsec). This increase in speed lets the 80386 run with one wait state instead of two. Matched-memory cycles do not appear to be consistent between the various PS/2 models. The 16-MHz Model 80 can execute matched-memory cycles; the 20-MHz Models 70 and 80 ignore them. Bus masters cannot run matched-memory cycles.

References

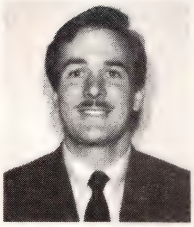
1. IBM Personal System/2 Model 50/60 Technical Reference (IBM# 68X-2224).

2. IBM Personal System/2 Model 80 Technical Reference (IBM# 68X-2256).

3. IBM Personal System/2 Model 50,60,80 MCA Architecture (IBM# G360-2637) Rev. 5.3, May 1987.

4. Altera Micro Channel Handbook, May 1988.

Authors' biographies



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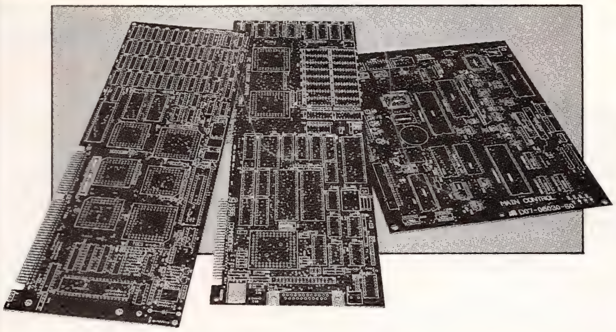

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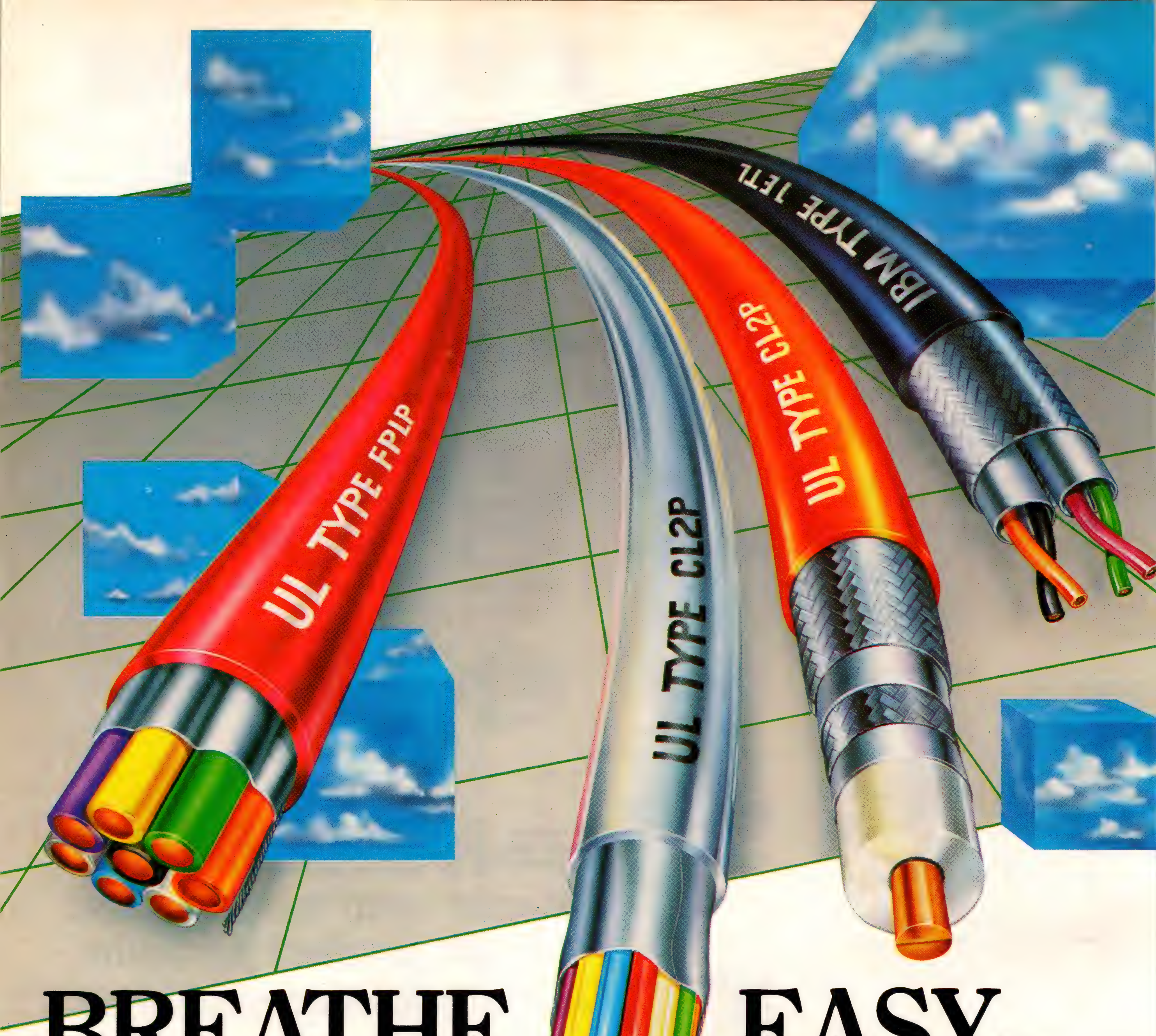

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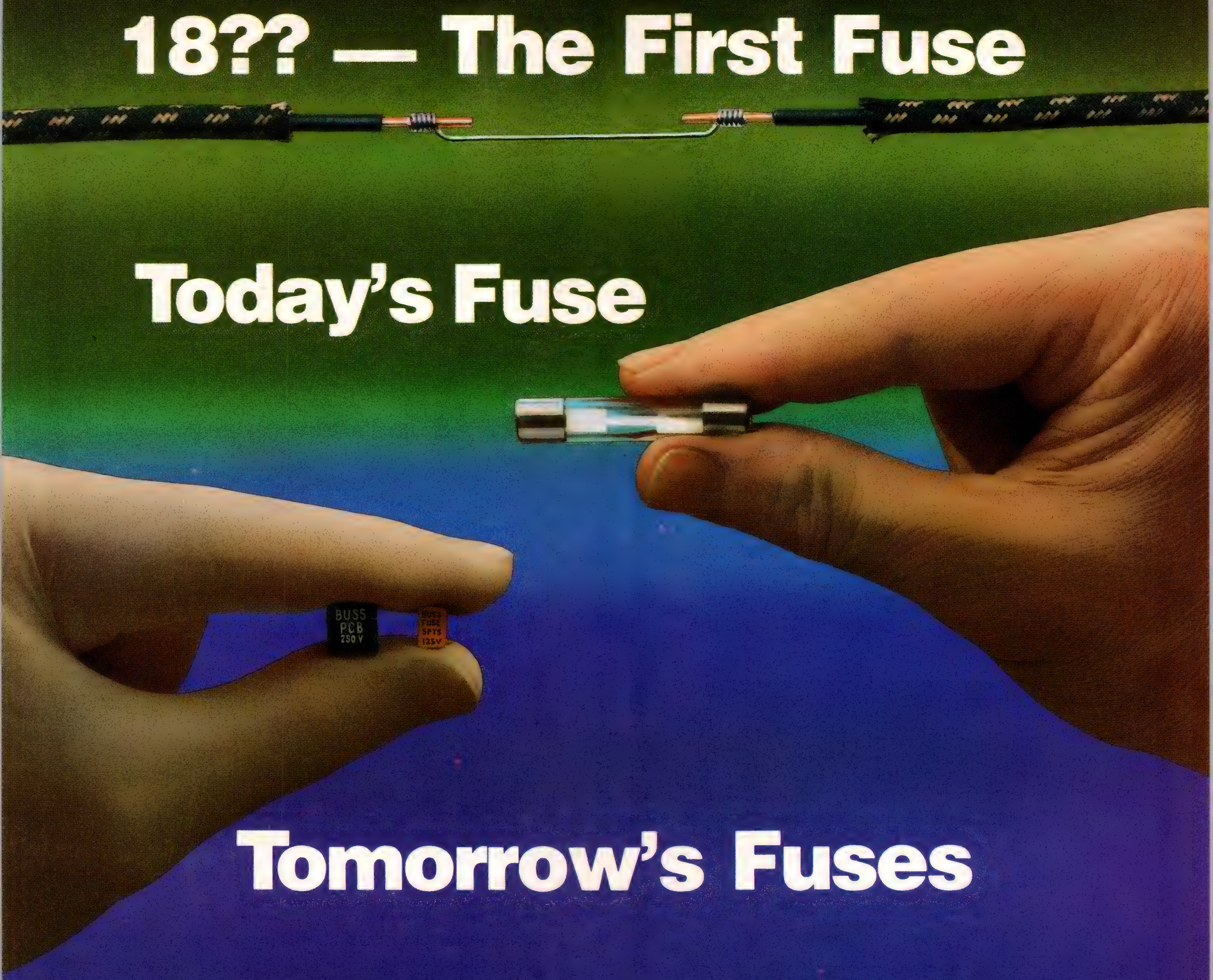

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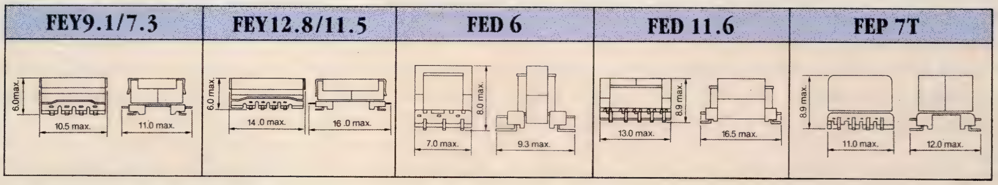

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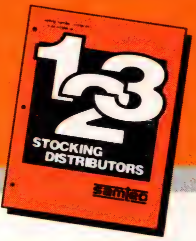

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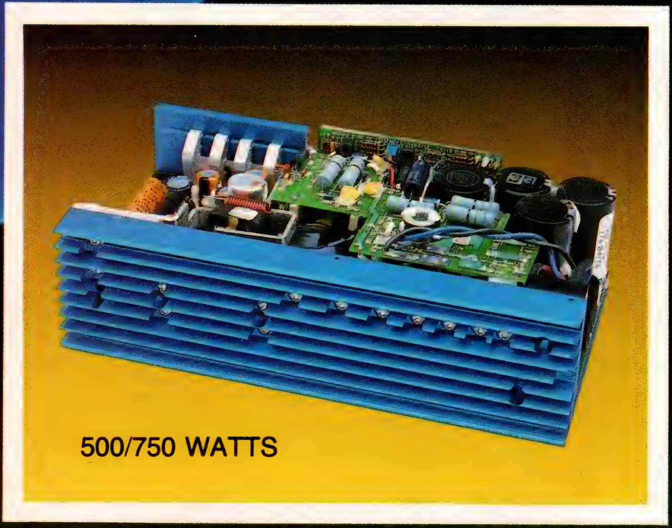

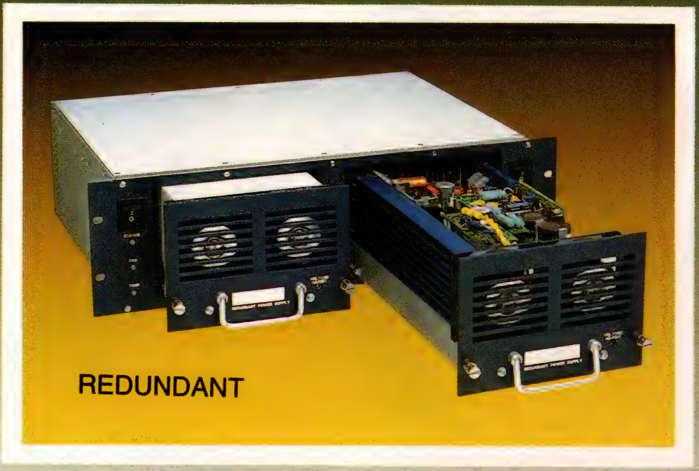

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Message protocol unloads VMEbus processors

Integrating VMEbus boards made by different manufacturers can be a daunting task. To lighten the burden, manufacturers and systems engineers should adopt a simple, uniform way to exchange information between VMEbus boards. The MPP (message-passing protocol) is one such method.

J H Brand and L de Graaf, *Compcontrol BV*

The MPP (message-passing protocol) standardizes the exchange of messages between transmitting boards and receiving boards in VMEbus systems. The MPP can reduce the load on transmitting boards, such as CPU boards, because the receiving boards (intelligent peripheral controllers in VMEbus systems) perform all the overhead in data transfers—including arbitration in multiprocessing systems.

The basic structure of the protocol is a simple, linked-list queue (**Fig 1**). A transmitting processor enters a message in a receiving board's queue by finding the end of the queue and adding pointers to its message. The receiving board finds messages by following the linked list of message pointers.

The transmitting board stores its messages either in RAM or on a disk in the system until the receiving board is ready to receive the message. Theoretically, any number of processors can gain access to a given receiving board; the receiving board decides when and in what order it will execute the pending commands. The number of messages that a transmitting board can queue up depends only on the amount of memory or disk space that it has available to hold messages.

The transmitting and receiving boards communicate by using unspecified software constructs such as interrupts or mailboxes. The MPP leaves you free to allocate priorities, and it allows a receiving board to give time-out signals to a transmitting board if a message isn't handled within a set period.

An added feature

One particularly attractive feature of the MPP is its ability to teach commands to receiving boards. Formally defined, a protocol is a state machine that effects message transfers. The state machine must be completely separate from and unaffected by the contents of the messages it handles. Therefore, the message can be anything from mere data to a complete, executable program. You can install a new receiving board in an MPP-equipped VMEbus system by using only one command in software: "learn new command." If you prefer, you can load application-specific software into a receiving board as the need arises.

The MPP is relatively hardware independent, and its hardware requirements are minimal. Each transmitting board needs a few bytes of RAM to store address

The number of messages that a transmitting board can queue up depends only on the amount of memory or disk space that it has available.

pointers; the receiving boards need enough RAM to store a minimum of one message at a time. Both types of boards should have dual-access RAM, to allow access across the VMEbus in addition to local, onboard access. Moreover, a DMA controller on each of the receiving boards helps large multiprocessing systems to increase the efficiency of the VMEbus traffic.

The MPP makes few demands on local memory; it needs only four long words to set up the initial queue, plus an overhead of about 15 long words for each message as it's added to the queue. The message itself can be any length. You can standardize the software for the transmitting boards, because each transmitting board gains access to a receiving board's message queue in the same manner.

Each message in a queue has a fixed-size header that holds information about the message. The following are examples of such information and the actions on that information:

- A command block tells the receiving board what to do.
- Once it has handled the message, the receiving board should use the message's interrupt-priority level when responding to the transmitting board.
- The interrupt vector is the address of the sending processor's interrupt routine, or the address of the mailbox to which the receiving board must reply when it has handled the message.
- A data block and a status block, including error messages, inform the receiving board what action to take if it cannot act on the message.

Message queue is different for each board

Each receiving board has its own queue of messages. At the risk of some confusion, you should note that a receiving board can also initiate a message transfer if the receiving board is intelligent and has enough onboard RAM to store a message. When a receiving

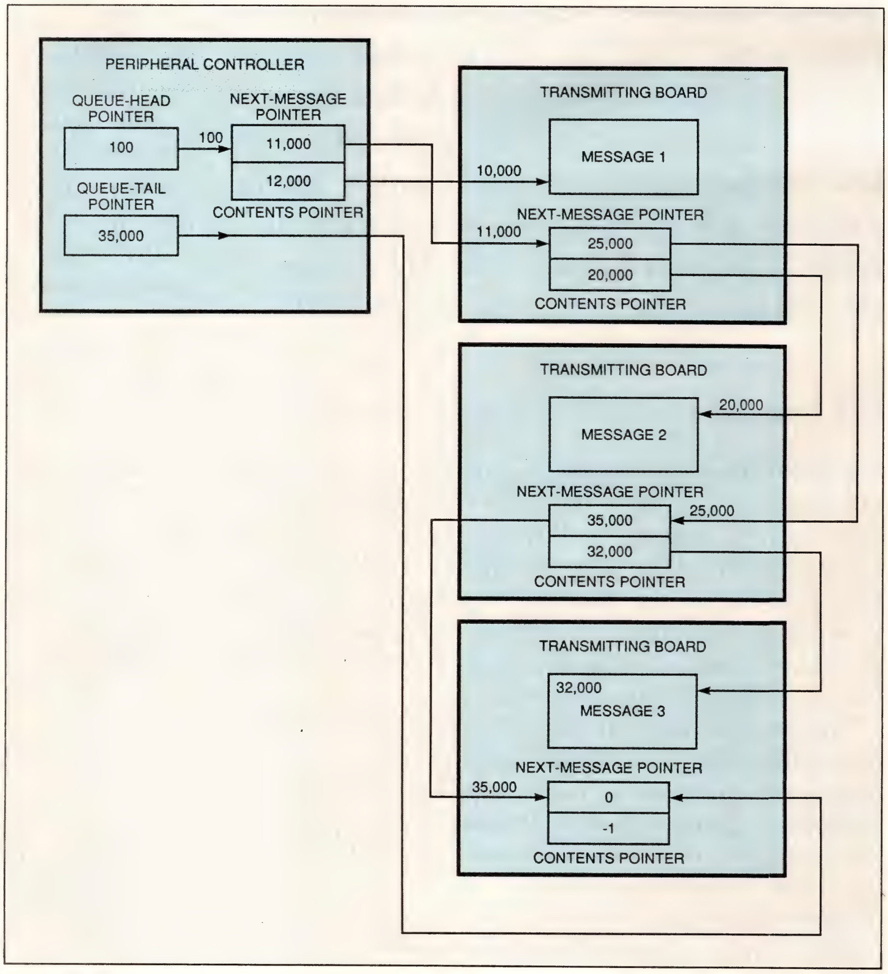

Fig 1—The message-passing protocol (MPP) *uses a queue of linked message pointers distributed around a VMEbus system to inform a receiving board of pending messages. The example addresses shown are arbitrary and are included only for clarity.*

board switches roles and transmits a message, it enters a message in the relevant receiving board's queue just like any other transmitting board.

Returning to **Fig 1**, you can see that the bulk of a receiving board's message queue is distributed around the transmitting boards in a system. The receiving board maintains only pointers to the head and tail of the queue and pointers to the first queued message. The transmitting boards hold the pointers to all other messages in the queue. Each entry in the queue consists of two long words; the first gives the address of the next queue entry (the next-message pointer), and the second gives the address of the current message (the contents pointer).

A next-message pointer of 0 and a contents pointer of −1 signal the last entry in the queue (the "null" message). These pointer contents are arbitrary, inaccessible numbers that indicate that no associated message exists. At system initialization **(Fig 2)**, the queue-head pointer and the queue-tail pointer are the only two entries in the queue, and both point to the same null message.

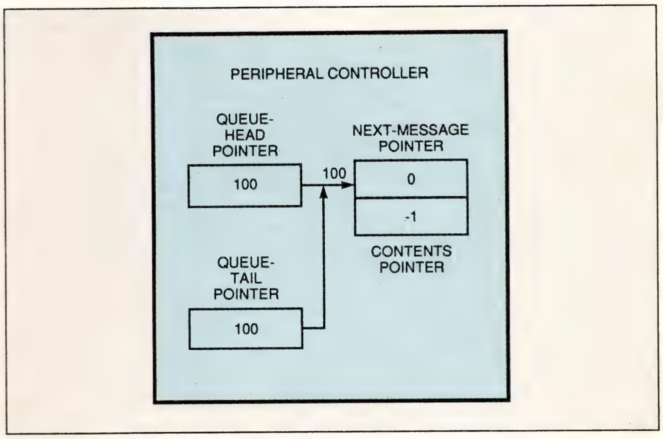

Fig 2—At system initialization and when the queue is empty, *the queue-head pointer and the queue-tail pointer on the receiving board point to the same address—to a null entry—showing that no messages are pending.*

The receiving processor's local memory contains two long-word locations, which store the queue-head pointer and the queue-tail pointer; the queue-head pointer holds the address of the head of the queue (also held on the receiving board), while the queue-tail pointer holds the address of the queue tail (held on the last of the transmitting boards in the queue).

If you want to send messages

Fig 3 shows the procedure that a transmitting board uses to initiate communication by adding a message to a receiving board's queue. The transmitting board first concocts the message in its own local RAM or on disk, and then it copies the existing "null" message into its own RAM (address $11{,}000_{\text{HEX}}$ for the arbitrary example in **Fig 3**). It then alters the old "null" message to point to message 1 (address $10{,}000_{\text{HEX}}$) and the next queue entry (address $11{,}000_{\text{HEX}}$). This queuing action can generate a local interrupt to inform the receiving board that a transmitting board has updated the receiving board's queue, thus obviating the receiving board's polling of its own queue.

Each transmitting board repeats this procedure for each message it wants to send **(Fig 4)**, thus creating a linked list. Adding another message to the queue in **Fig 4** would, in fact, produce the situation in **Fig 1**.

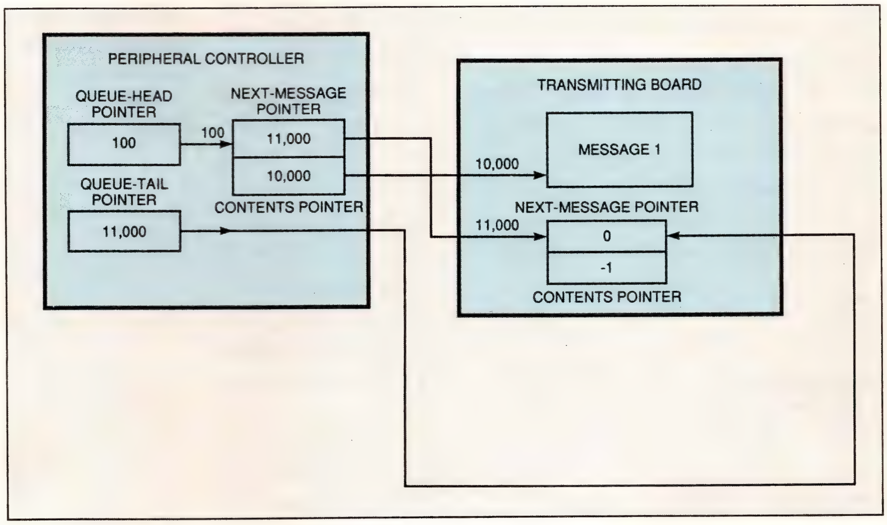

Fig 3—The first transmitting board to queue a message *copies the receiving board's null message into its next-message pointer. Then the transmitting board loads the addresses of its message and next-message pointer into the receiving board's next-message pointer and queue-tail pointer.*

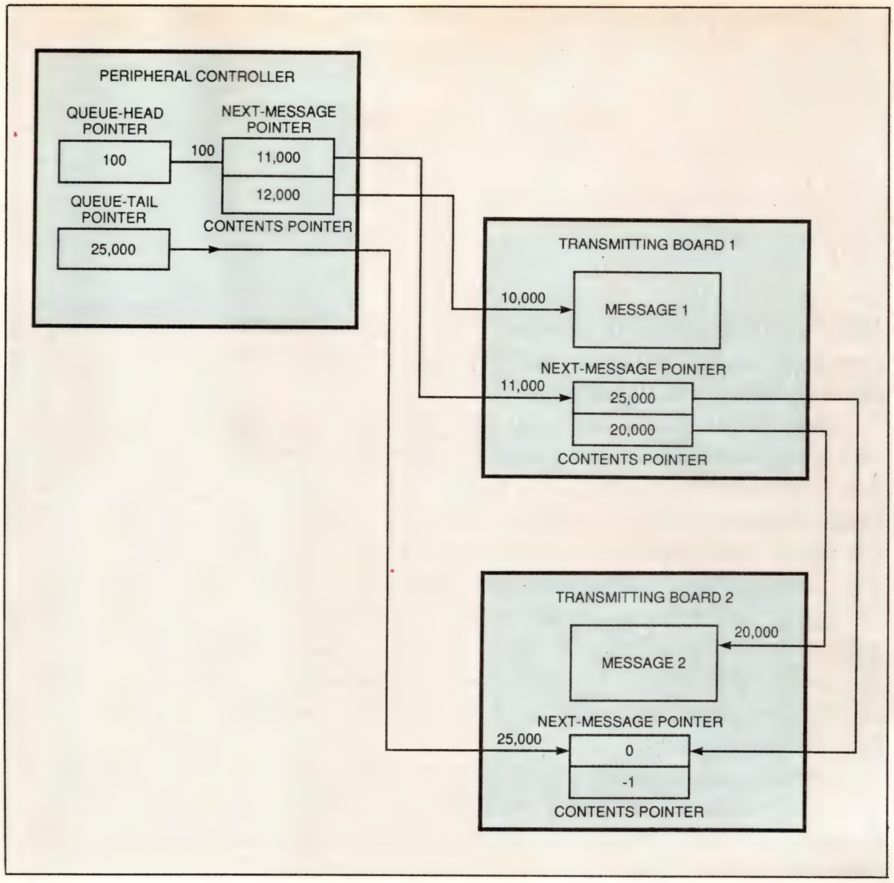

Fig 4—Subsequent transmitting boards *that wish to transmit a message to the receiving board examine the receiving board's queue-tail pointer to find the end of the queue. They insert their message in the queue by repeating the action outlined in* ***Fig 3.***

The procedure allows a transmitting board to transmit a message without having to wait for the receiving board to first act on a previously sent message. The transmitting board has two ways of ensuring that only one transmitting board can update the message queue at a time: it can either hold on to the VMEbus while it is updating the message queue (which takes only four VMEbus cycles), or it can set a semaphore that prevents other transmitting boards from getting access to the queue-tail pointer.

To receive a message, a receiving board must remove the message from the queue. Removing a message from the linked-list queue is as simple as queuing one up. As you can see in **Fig 4**, the receiving board obtains the address of the first message ($10{,}000_{\text{HEX}}$) from its contents pointer, transfers the message to its own local memory, and acts on it.

After the receiving board processes the message, it updates its next-message pointer and contents pointer (currently holding $11{,}000_{\text{HEX}}$ and $10{,}000_{\text{HEX}}$) to their new values ($25{,}000_{\text{HEX}}$ and $20{,}000_{\text{HEX}}$). The receiving board then signals the transmitting board that its message has been acted on and that a return message—if required—has been stored. The transmitting board's next-message pointer and contents pointer then get set to 0, showing that the message buffer (together with the associated next-message pointer and contents pointer) is free for reuse.

The simplicity of this protocol confers several advantages. For example, checking for the cause of a system lockup is a relatively simple matter. Such lockups are endemic to multiprocessing systems. A system can stall because two programs are locked in a "fatal embrace," each suspended and waiting for the other to answer a message. In an MPP-equipped system, when a lockup occurs, the queue holds a complete chain of messages in its linked list, and a quick study indicates the offending programs. The MPP system is also easy to expand; a new transmitting board needs only a copy of the protocol and the address of the queue-tail pointer on each receiving board with which it must communicate. EDN

Authors' biographies

J H Brand is a design engineer and has been with Compcontrol for four years. He designs and develops VMEbus modules and writes driver and test software for his designs. He has an engineering degree from Rotterdam's Institute for Technology. In his spare time, he enjoys music, motorbike riding, and visiting foreign countries.

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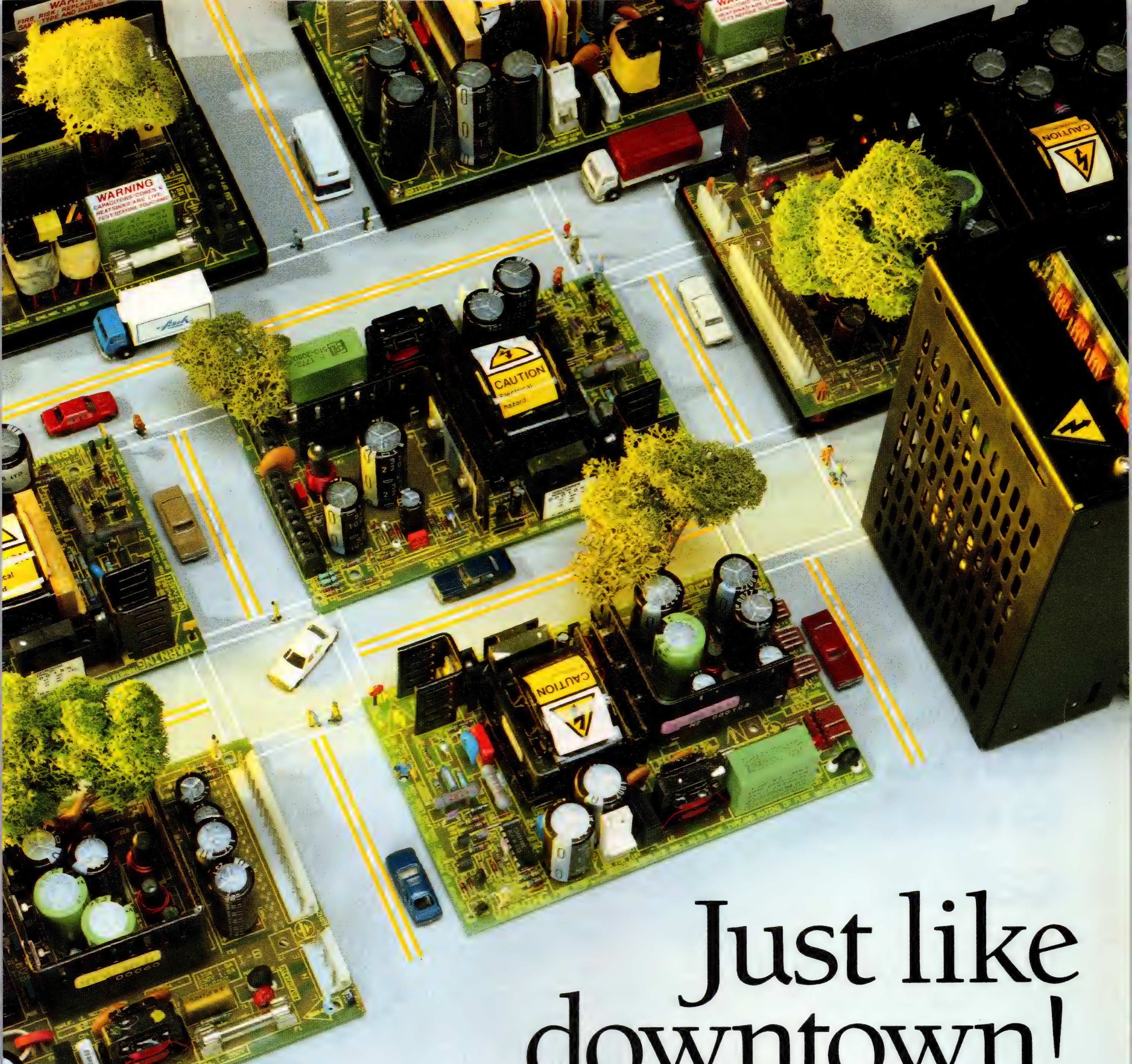

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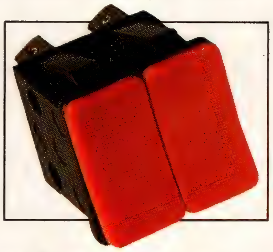

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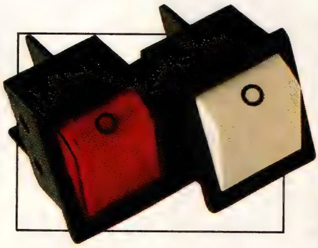

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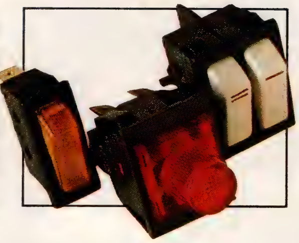

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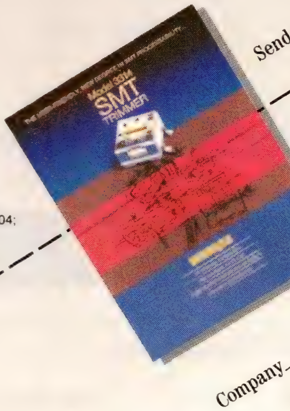

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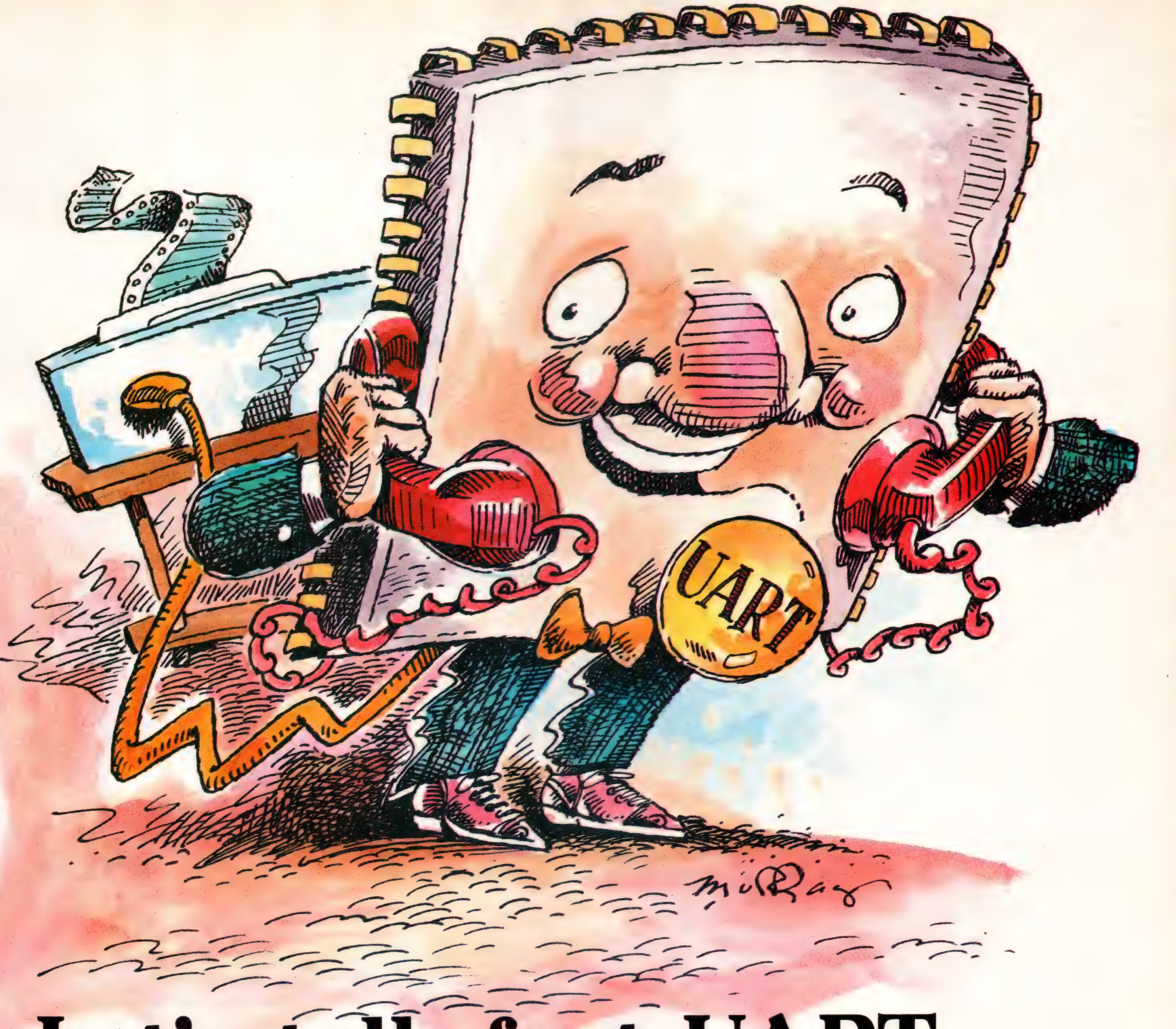

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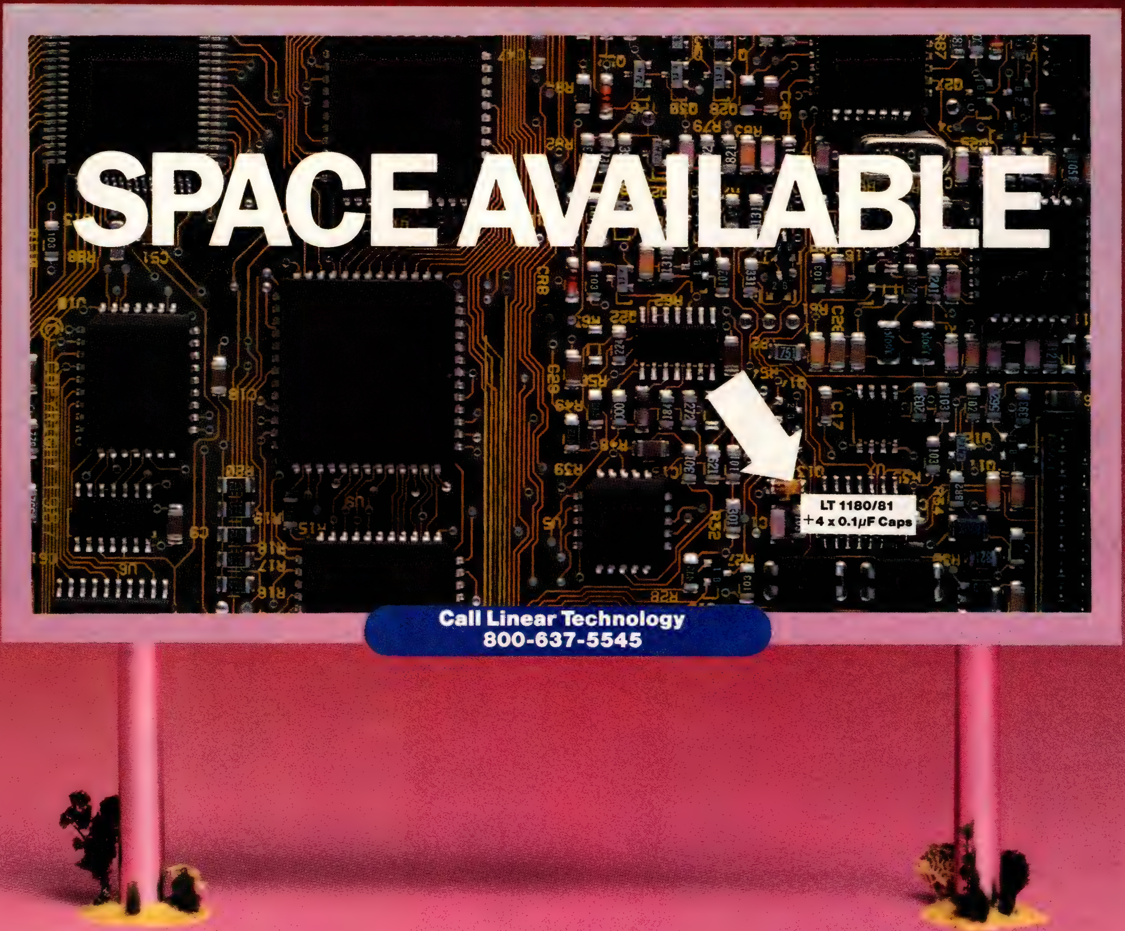

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LT1030	4	0	±12V	YES*	YES	N/A
LT1032	4	0	±12V	YES*	YES	N/A
LT1039	3	3	+5V, ±12V	YES*	YES	N/A
LT1039-16	3	3	+5V, ±12V	NO	YES	N/A
LT1080	2	2	+5V	YES*	YES	1µF
LT1081	2	2	+5V	NO	YES	1µF
LT1130	5	5	+5V	NO	YES	1µF
LT1131	5	4	+5V	YES*	YES	1µF
LT1132	5	3	+5V	NO	YES	1µF
LT1133	3	5	+5V	NO	YES	1µF
LT1134	4	4	+5V	NO	YES	1µF
LT1135	5	3	+5V, ±12V	NO	YES	N/A
LT1136	4	5	+5V	YES*	YES	1µF
LT1137	3	5	+5V	YES*	YES	1µF
LT1138	5	3	+5V	YES*	YES	1µF
LT1139	4	4	+5V, +12V	YES*	YES	1µF
LT1140	5	3	+5V, ±12V	YES*	YES	N/A
LT1141	3	5	+5V, ±12V	YES*	YES	N/A
LT1180	**2**	**2**	**+5V**	**YES***	**YES**	**0.1µF**
LT1181	**2**	**2**	**+5V**	**NO**	**YES**	**0.1µF**

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DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

Multiple technologies produce fast clock

Michael A Wyatt
SSAvD Honeywell Inc, Clearwater, FL

By combining SAW, GaAs, and high-speed bipolar devices, you can achieve an ECL-compatible clock oscillator **(Fig 1)**. The heart of the circuit is the SAW-stabilized network that surrounds Q_1, the DXL2401 GaAs FET from Gould Dexcel Div (Santa Clara, CA). The 1143 SAW oscillator from RF Monolithics (Dallas, TX) has 180° of phase shift at resonance and couples the energy from Q_1's drain to its gate. L_1 and C_1 tune Q_1's drain to 1143 MHz; L_2 and C_2 tune Q_1's gate to 1143 MHz. These networks also maintain the proper phase relationship for oscillation at 1143 MHz. The frequency of oscillation and temperature drifts are strictly determined by the SAW characteristics. High-quality SAW devices typically have Qs in the neighborhood of 6000 and frequency-drift rates as low as 1 ppm/°C.

An ultrahigh-speed, bipolar, ECL-compatible decision IC, the Sony CBX1107Q, functions as a comparator and ECL-level translator. C_1 couples Q_1's output to the CBX1107Q's noninverting data input. R_1 acts as a load resistor and supplies bias voltage to pin 1 of the decision IC. The inverting data input of the CBX1107Q is directly connected to the bias voltage, V_{BB}, which configures the IC as a high-speed analog comparator with input levels around V_{BB}. R_2, R_3, and the −2V supply provide the proper termination and voltage level for ECL-compatible logic from the CBX1107Q's data outputs. **EDN**

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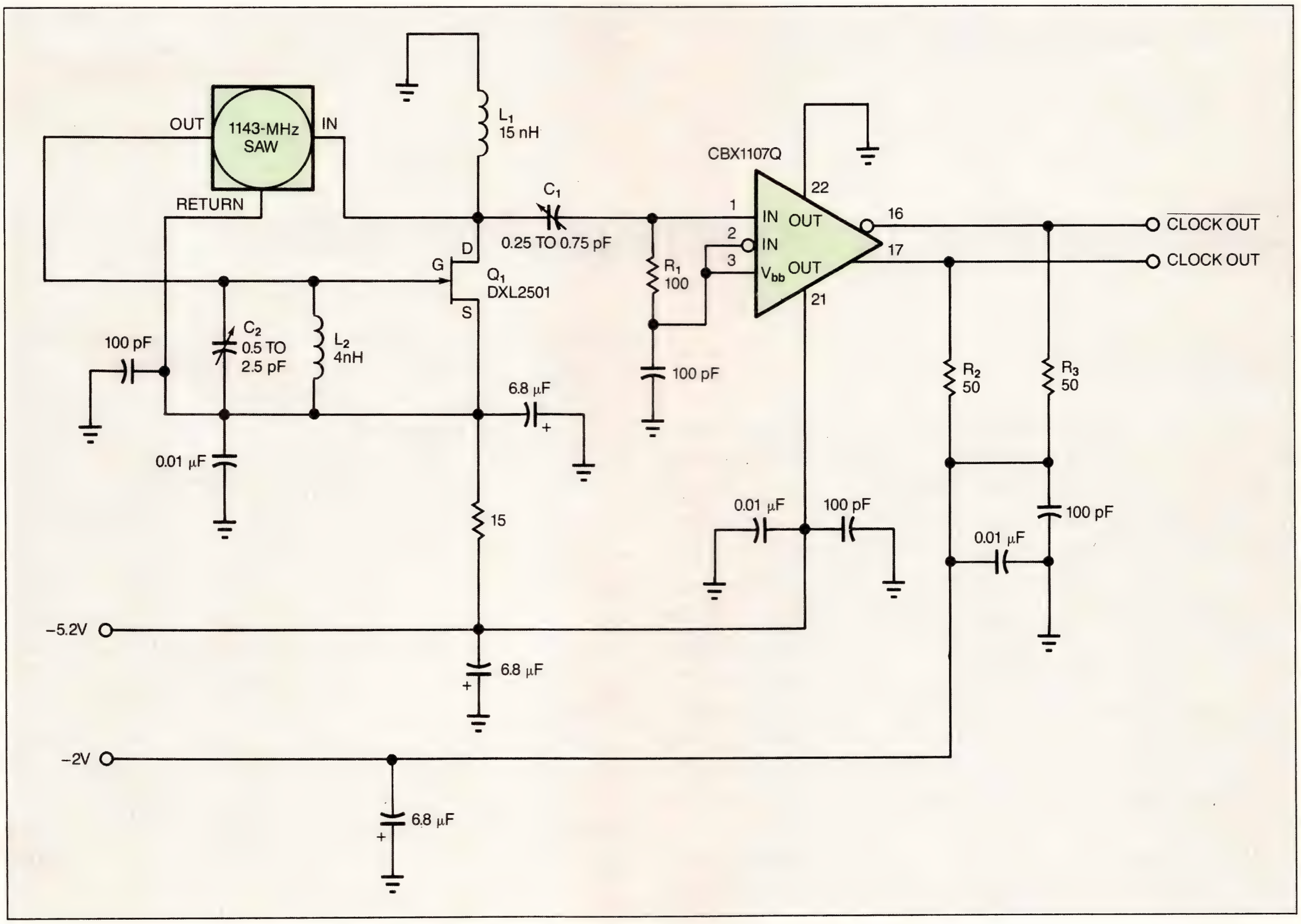

*Fig 1—**By combining SAW, GaAs, and ECL devices,** this circuit implements a fast, stable oscillator.*

Two ICs implement digital noise filter

James W Harrigfeld
Harmonic Research Inc, Paramus, NJ

A simple digital noise filter **(Fig 1)** requires two ICs that can be found in most of the standard logic families. IC_{1A}, a 4-bit, serial-in parallel-out shift register, samples the input signal at a rate set by the clock frequency, f_C, and stores the four most recent samples. IC_2, a four-bit comparator, monitors all these samples and latches the input signal into IC_{1B} only if the current input and last four samples all match. Signals, glitches, or noise with periods less than $3 \times 1/f_C$ won't pass through to the output latch. To obtain the least amount of delay, set the frequency of this circuit's clock as high as possible, but make sure that the frequency is low enough to catch wide glitches. Set the clock period to about the same width as the biggest glitch you expect.

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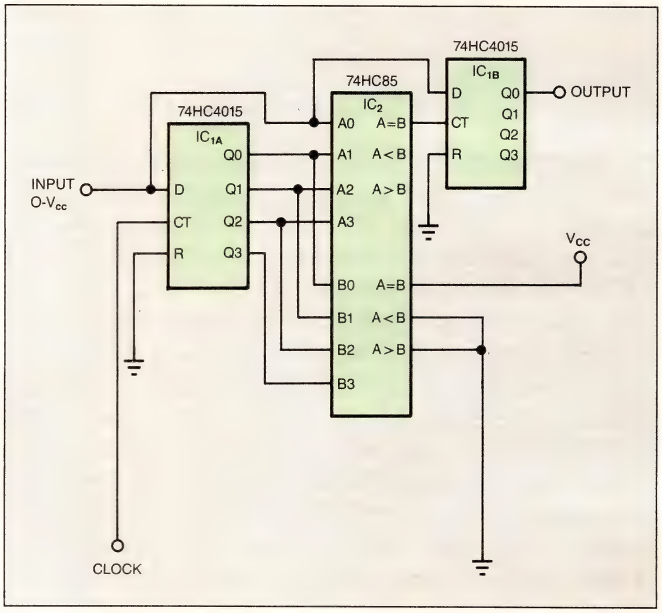

***Fig 1—This digital noise filter rejects glitches** and signals that have a period less than three times the period of the circuit's clock.*

Clock disabler preserves signal integrity

Mitchell B Kary
Analogic Corp

In an asynchronously sampled data-acquisition system, the pc-board layout and high-impedance grounds can cause clock modulation that results in spurious tones and an increase in the noise floor of the converted signal. These problems arise because the clock noise is not correlated with the analog-signal and reference-voltage inputs. You can reduce clock modulation of the signal and reference inputs of a successive-approximation A/D converter by disabling the converter's clock input after signal acquisition. By disabling the clock after the track mode, all clock-induced noise on the analog and reference inputs settles prior to the input sampling, which occurs on the negative edge of the hold signal.

Fig 1's circuit disables the clock input of the 4201, 4202, and 4203 16-bit sampling A/D converters (Analogic Corp, Peabody, MA) following the assertion of the converter's end-of-track (EOT) signal. The circuit configures two NAND gates, IC_{2A} and IC_{2B}, as a reset/set flip-flop. Upon power-up or converter reset, C_1, R_1, and D_1 differentiate the RST pulse and provide a negative edge that resets the NAND-gate pair. When IC_{2A} and IC_{2B} are in this reset state, they enable IC_1, which provides the clock input to the converter. C_2, R_2, and D_2 differentiate the falling edge of the EOT signal, which sets the reset/set flip-flop pair. In this state, the logic high on the clock-enable line forces IC_1's output, and thus the converter's clock input, to a logic high. The A/D converter remains in this "quiet" mode until the falling edge of the hold signal resets the flip-flop **(Fig 2)**.

This technique can result in a 2-to-1 reduction of the rms modulation noise and is especially valuable in hybrids and in pc-board layouts where real estate is minimal or where low-impedance ground planes aren't possible.

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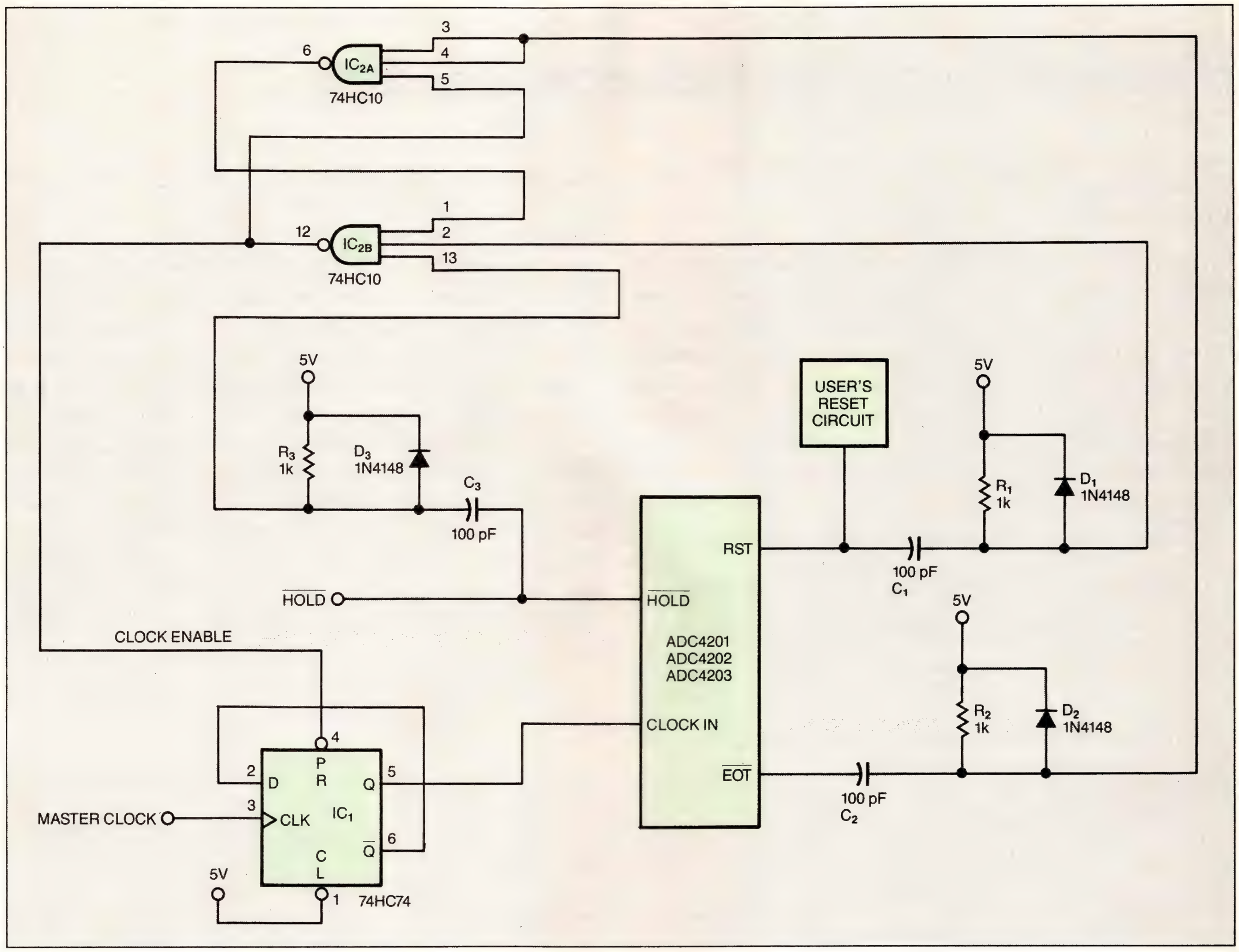

Fig 1—Methods to reduce noise *in asynchronously sampled systems include shutting down the system clock between the track and hold modes, as shown in this circuit.*

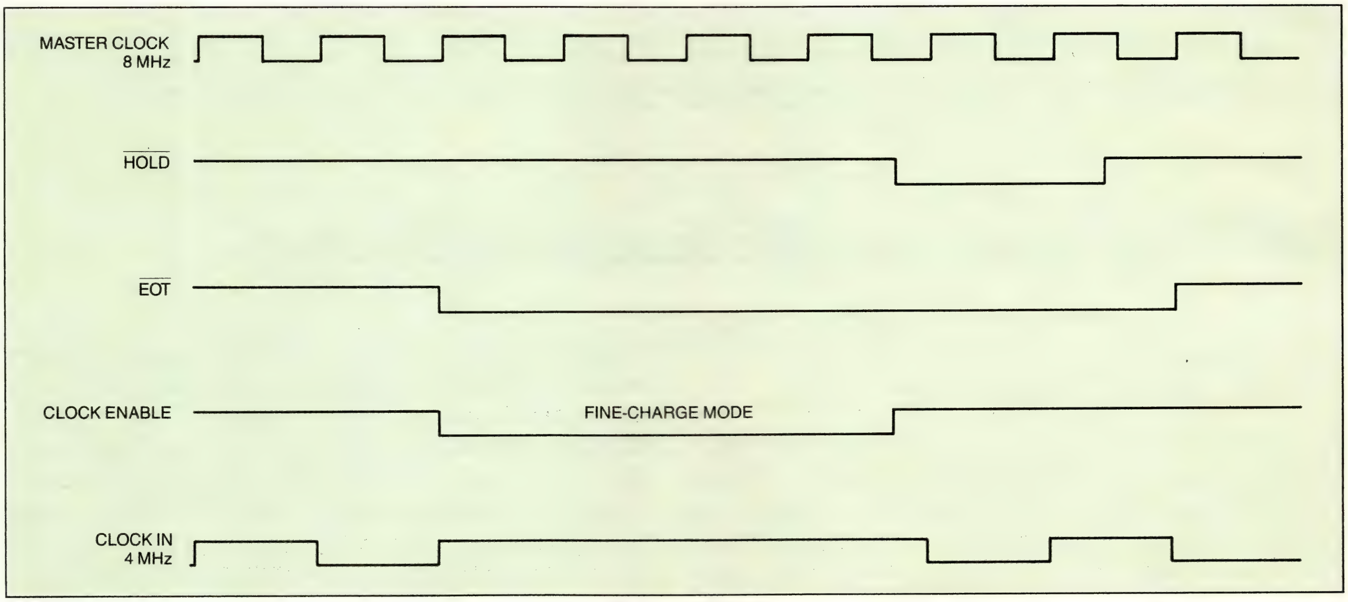

Fig 2—Disabling the input clock *between the falling edges of the* $\overline{EOT}$ *and* $\overline{HOLD}$ *signals reduces clock modulation and signal noise.*

Single cable carries bidirectional data

Terje Kvinge
EB-Nera, Bergen, Norway

The circuit in **Fig 1** enables bidirectional transfer of digital data over a single coaxial cable. Practical uses for the circuit include point-to-point communications inside computers or processors. The circuit operates with independent NRZ data streams as fast as 34M bps in each direction with cables as long as 20m. The DS26C32 CMOS line receiver from National Semiconductor can perform both receiver functions (IC_{1B} and IC_{1D} and driver functions (IC_{1A} and IC_{1D}) because of its low-impedance output when used as a driver. The series-output resistors, R_1 and R_2, terminate the line and ensure that no reflections occur. Because both drivers "see" these resistors, the line voltage theoretically can have three levels. But, because the trigger level on the receiver is set to three quarters or one quarter of the supply voltage, depending on the output state, the receivers always detect correct data (**Table 1**).

The DS26C32 isn't the ideal component for this application. A better choice would be a CMOS buffer that has a lower output impedance and less input capacitance. By using a specially designed driver/receiver, this circuit should be able to transmit data at 100M bps. If implemented in GaAs technology, the circuit might handle data rates as high as 1G bps. **EDN**

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TABLE 1—DATA-TRANSMISSION TRUTH TABLE

INPUTS		LINE RECEIVER TERMINALS (V)				OUTPUTS	
A	B	V_{A+}	V_{A-}	V_{B+}	V_{B-}	A	B
0	0	0	1.25	0	1.25	0	0
0	1	2.5	3.75	2.5	1.25	0	1
1	0	2.5	1.25	2.5	3.75	1	0
1	1	5	3.75	5	3.75	1	1

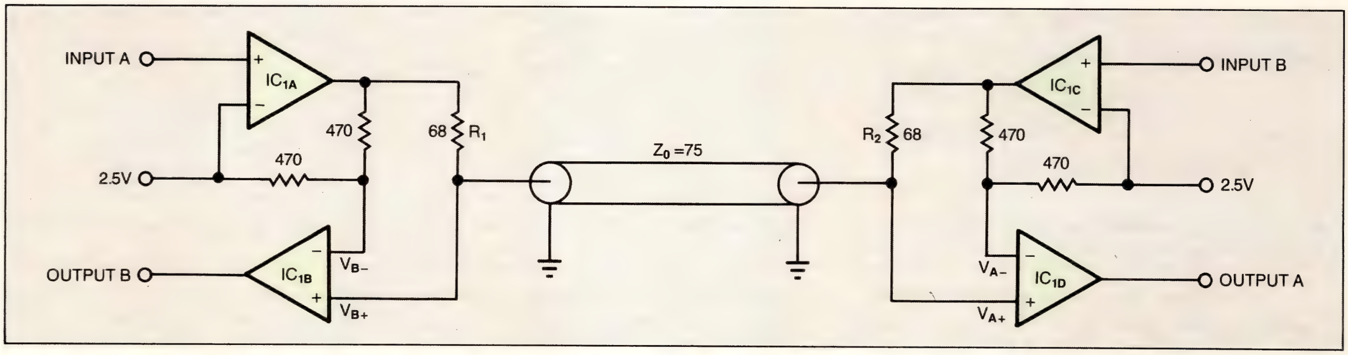
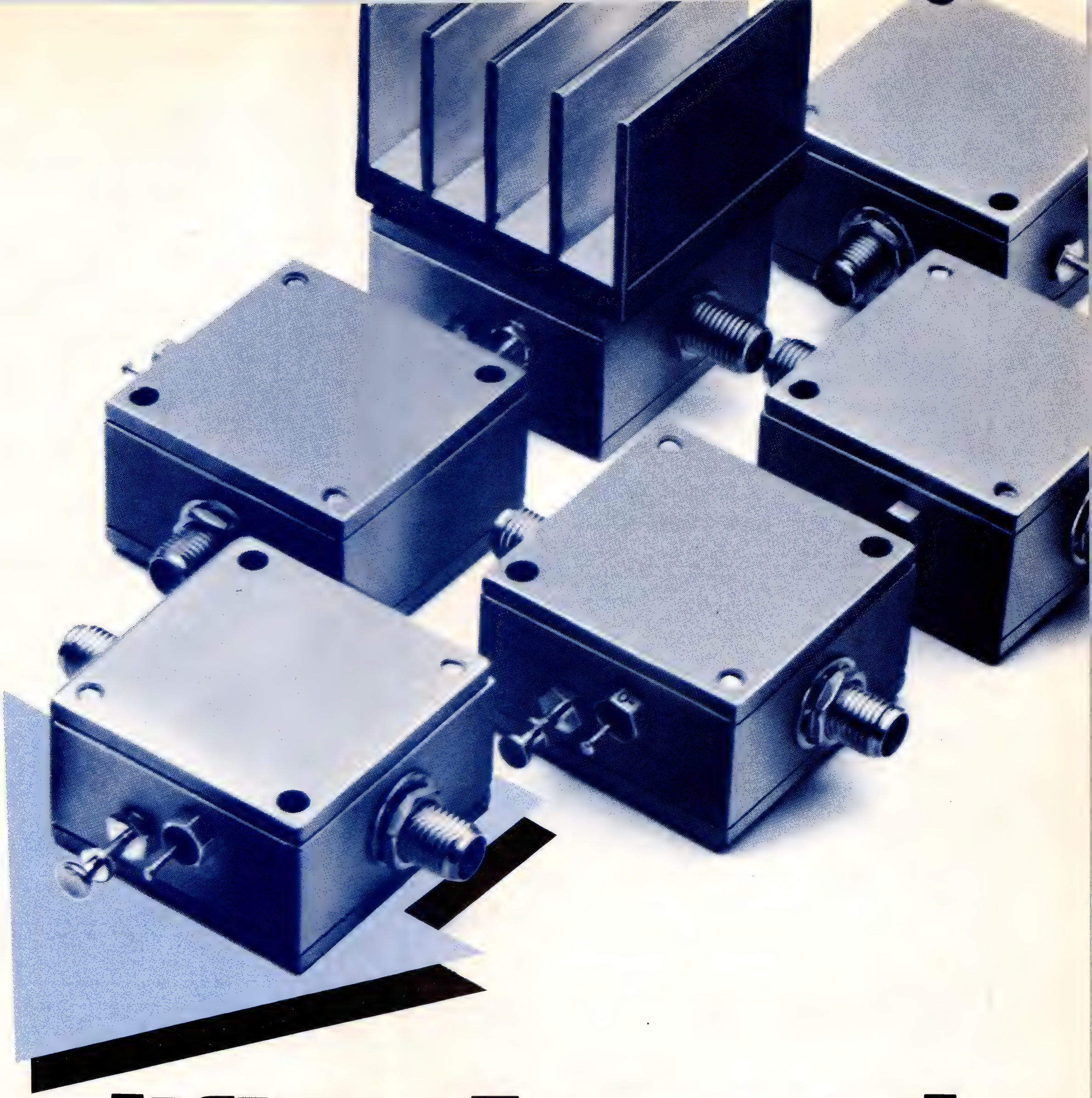


***Fig 1—By using CMOS receivers** as both receivers and drivers, this circuit transfers bidirectional data over a single coaxial cable.*

SAW oscillator uses IC leads as inductors

Steve Kenney
Scientific Atlanta, Norcross, GA

The SAW-oscillator design in **Fig 1** eliminates the need for many external components by using a wideband amplifier that doesn't need external bias circuitry and by using the leads of the amplifier as tuning inductors. The 0.12-in. leads of the NE5205's EC package form L_1 and L_2. These inductors provide the necessary phase shift for oscillation to occur at the peak of the SAW resonator's insertion loss. If you're using a surface-mount D package, you can form these inductors with a microstrip line. The design uses the Sawtek 851500—a 600-MHz, 180° quartz resonator. The Q of this device with a 50Ω load is 5300. By inserting fixed values or a varactor diode for the capacitor C_T and by keeping the capacitance in the range of 4 to 14 pF, you can tune the output frequency to within 0.05% of 600 MHz without degrading the phase noise. You can also modify this circuit for other output frequencies by changing



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ZFL-1000	0.1-1000	17	+9	6.0	79.95
ZFL-1000G*	10-1000	17	+3	12.0	199.00
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ZFL-1000H	10-1000	28	+20	5.0	219.00
ZFL-500HLN	10-500	19	+16	3.8	99.95
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95
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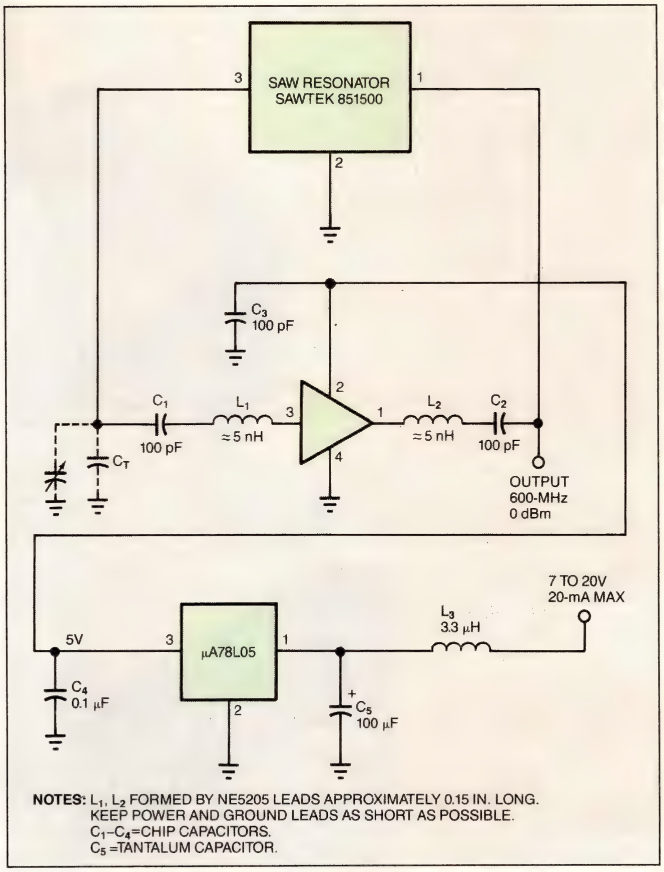

***Fig 1—By using the amplifier leads as inductors,** this 600-MHz SAW oscillator requires fewer parts than conventional SAW designs.*

the SAW resonator. The circuit's upper-frequency limit is approximately 700 MHz, because at this frequency the NE5205's gain drops below the insertion loss of most SAW resonators.

Fig 1's circuit produces about 1 mW of output power with an SSB phase noise of −80 dBc/Hz at a 100-Hz offset from the carrier frequency and −110 dBc/Hz at a 1-kHz offset. (The unit dBc represents the decibels above or below the power level of the carrier frequency.) You can increase the output power, which degrades the phase noise, by increasing the regulator voltage.

To use the oscillator in a phase-locked loop, it's best to add a varactor diode in parallel with a fixed C_T. When the oscillator isn't locked, you can expect a maximum load pull of approximately ±15 kHz with a 2:1 VSWR. In other words, the oscillator's output frequency will change by about ±15 kHz with a 2:1 load change, including the effects contributed by any reactive load elements. To use this design with a mixer or other high VSWR load, you can use an additional NE5205 as a buffer amp. EDN

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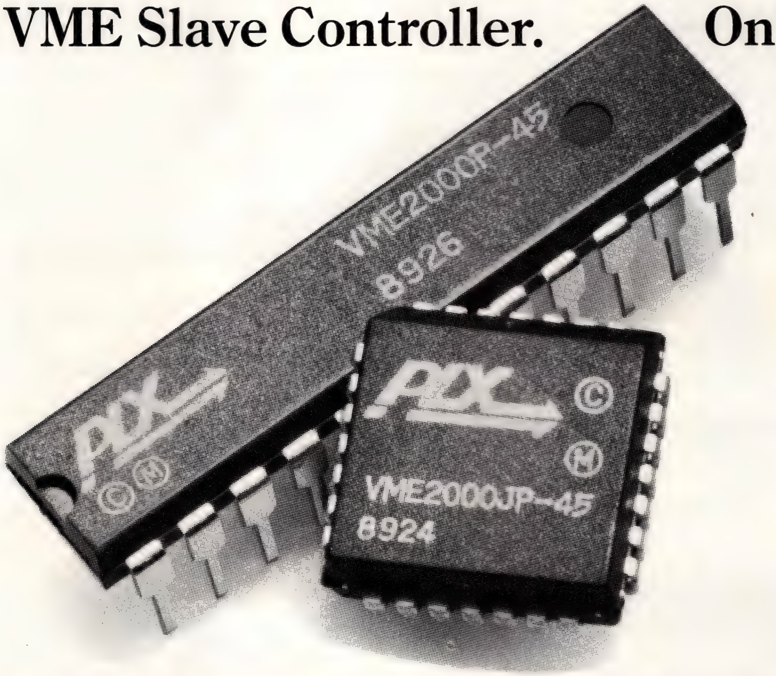

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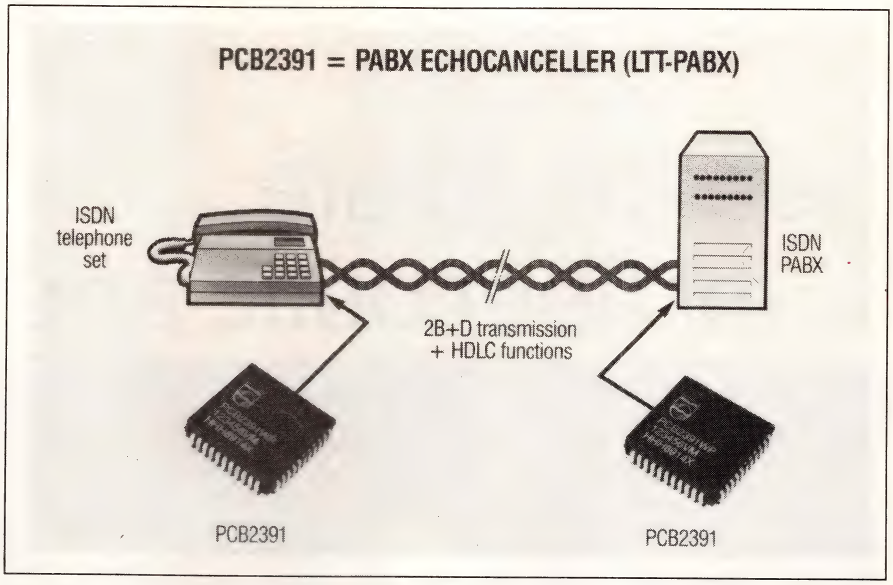
CIRCLE NO 193

NEW PRODUCTS

INTEGRATED CIRCUITS

ISDN Echo-Canceller IC

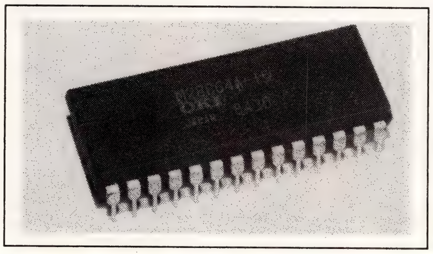
- *Optimized for PABX extension lines*
- *Features on-chip layer-2 functions*


PCB2391 = PABX ECHOCANCELLER (LTT-PABX)
ISDN telephone set
ISDN PABX
2B+D transmission + HDLC functions
PCB2391
PCB2391

Optimized for PABX extension lines, the PCB2391 ISDN (Integrated Services Digital Network) echo canceller also supports remote multiplexers and can operate in public exchange lines. The IC, which incorporates layer-2 functions, is line-polarity independent and needs no active external components to send signals on the line. The PCB2391 provides full duplex transmission of 2B + D (144k-bps) channels via normal twisted-pair wires, and also features a 1B + D mode for time-slot saving on the exchange side. Attenuation tolerance is 18 dB min at 100 kHz. The layer-2 functions are in full accordance with the ECMA-40 standard and include a 32-byte FIFO for data transfer to and from a microcontroller. The PCB2391 offers a 2.048M-bps interface for use with standard codecs and is controlled via a data/address multiplexed microcontroller interface. On the line side, the IC uses a Manchester biphase code at a line rate of 152k bps. Adaptive echo-cancellation and decision-feedback mechanisms are applied internally. The PCB2391, which comes in a 44-pin plastic leaded-chip carrier, operates from a single 5V supply and consumes less than 100 mW (40 mW in the power-down mode). $43 (1000).

Philips Components, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 724324.

Circle No. 399



64k-Bit EEPROM

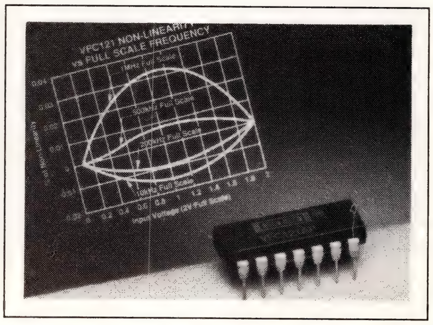
- *Organized as 8k × 8 bits*
- *Has 10-year data-retention time*

The MSM28C64A 64k-bit EEPROM joins the company's previously introduced MSM28C16A 16k-bit device. Organized as 8k × 8 bits, the electrically erasable, electrically programmable ROM works from a single 5V supply for read, write, and erase functions. Standby current is typically 100 μA. TTL compatible, the MCM28C64A has a guaranteed minimum of 10,000 write cycles/byte. The chip features an access time of 120 nsec, which makes it suitable for use with most μP-based systems. Its 10-year minimum data-retention time eliminates the need for battery backup. The MSM28C64A comes in a JEDEC 28-pin DIP. $17.25 (100).

Oki Semiconductor, 785 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 720-1900. **Circle No. 400**

Precision V/F Converter

- *Works from a single supply*
- *Operates to 1.5 MHz*



The VFC121 V/F converter operates from a single supply ranging from 4.5 to 36V with full-scale input voltages to within 2V of the supply. Performance specs include a maximum nonlinearity of ±0.03% at 100 kHz, with operation to 1.5-MHz full scale where needed. Gain drift is only ±40 ppm/°C max at 100 kHz. The VFC121's serial output simplifies isolation of analog-input sections from digital-system elements. The device also provides a 2.6V reference for sensor excitation or external biasing. Specified for use over the industrial temperature range, the VFC121 comes in an 8-pin DIP. $7.35 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. **Circle No. 401**

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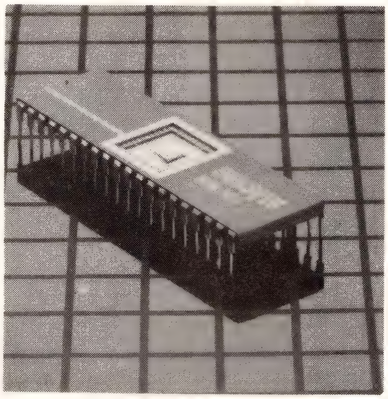
CIRCLE NO 27



A/D 3-Digit LCD Driver

- *Interfaces with pressure sensors*
- *Has 10-bit internal resolution*

Specifically designed to interface with semiconductor pressure sensors, the SM201 contains all necessary active devices to take the output from a basic bridge-type sensor and convert it to a calibrated 3-digit LCD readout. Included in the SM201 are 7-segment decoders, display drivers, a voltage reference, and a clock. The device features 10-bit internal resolution over a temperature range of −10 to +70°C, autozero capability, alarm drivers, and automatic shut-off options. The SM201, which operates with supply voltages from 2.5 to 10V, uses dual-slope integration to convert the analog sensor input into a digital signal to drive a 3-digit LCD. In custom applications, the SM201 can drive user-defined segments such as company logos. To maximize battery life, which is critical in hand-held pressure gauges, the SM201 provides programmable on-time selection. Two types of sensor excitation are available—a switched voltage source and a switched current source. Additional features include a selection option for peak or continuous reading and a low-battery indicator. The SM201 is available in 40-pin plastic or ceramic DIPs or in a 44-pin small-outline package. From $9.75 (100).

SenSym Inc, 1244 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500. **Circle No. 402**

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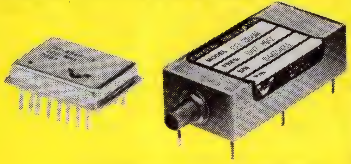
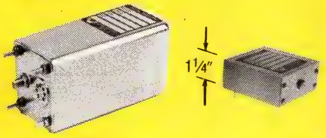
VECTRON

Small Sinewave XOs 4-1,000 MHz



	CO-484	CO-286 WL1
Frequency:	4-200 MHz	4-1,000 MHz
Noise:	−145 dBc/Hz	−155 dBc/Hz (floor at 100 MHz)
Stability: Opt:	±25 ppm over 0/+70°C ± 5 ppm over 0/+50°C ±50 ppm over −55/+85°C	
Size:	0.8″ x 1.0″ x 0.2″	1.0″ x 2.0″ x 0.6″

Reduced Noise OCXOs



	CO-245L2	CO-318L2
Aging:	5 x 10^{-10}/day	
Temp.:	4 x 10^{-11}/°C	4 x 10^{-10}/°C
Noise: @ 1kHz:	−160dBc/Hz	−155dBc/Hz
@50kHz:	−168dBc/Hz	−163dBc/Hz
Size:	2¼″ x 2¼″ x 4¼″	2¼″ x 2¼″ x 1¼″

VECTRON

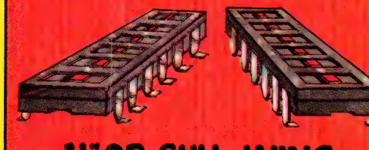
The Crystal Oscillator Company

VECTRON LABORATORIES, INC.
166 Glover Avenue. Norwalk, CT 06850.
Phone: (203) 853-4433. FAX: (203) 849-1423.

CIRCLE NO 195

SURFACE MOUNT DIP SWITCH

SURFACE MOUNT



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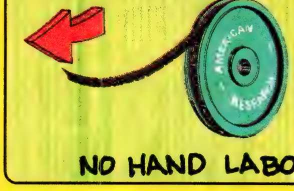

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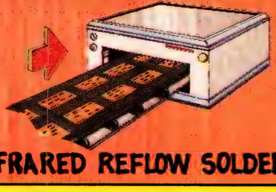

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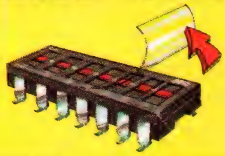

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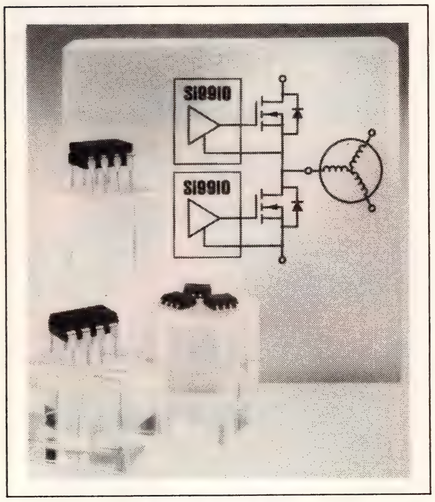


Power MOSFET Driver

- *Includes on-chip protection*
- *Provides low- or high-side drive*

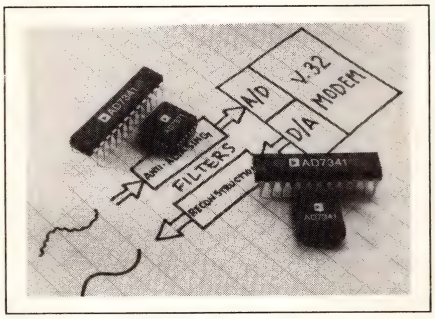
The Si9910 driver IC accommodates the operating conditions of the power MOSFET, thus protecting the MOSFET and optimizing its gate drive. The Si9910, which you can use as either a low- or high-side driver, includes a low-impedance, emitter-follower output and a Schmidt-trigger input. The on-chip protection circuitry protects the driven MOSFET against excess dv/dt and di/dt, undervoltage, and overcurrent by monitoring its operating conditions via feedback loops and then altering the Si9910's output drive. Designed to drive a wide range of power MOSFETs in motor-control applications from dc to 220V ac, the Si9910 simplifies the implementation of special features such as speed- and position-control functions. 8-pin DIP, $1.71 (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000. **Circle No. 403**

Voiceband Switched-Capacitor Chips

- *Antialiasing (receive) filter*
- *Reconstruction (transmit) filter*

The AD7371 antialiasing (receive) filter and the AD7341 reconstruction (transmit) filter provide the necessary signal conditioning between the analog signal environment and the system A/D and D/A converters. Both voiceband filters use switched capacitor architectures to achieve a S/N ratio of >75 dB. The devices are suitable for 12- to 14-bit applications including V.32 modems (full duplex, 9600 bps) and cellular telephones. The AD7371 antialiasing filter combines a second-order continuous filter with an eleventh-order switched-capacitor filter, yielding a passband from 180 to 3500 Hz. The AD7341 reconstruction filter contains a ninth-order switched-capacitor lowpass filter with a cutoff frequency of 3500 Hz that smoothes the digitally created (DAC output) transmit waveshape. Both filters have a passband ripple of < 0.4 dB and a gain error within ±0.5 dB. They sample at 57.6k samples/sec, derived from a user-supplied clock operating at 288, 576, 864, or 1152 kHz. The devices are available in either a 24-pin DIP or a 28-pin plastic leaded-chip carrier. AD7371, $15.60; AD7341, $13.20 (1000).



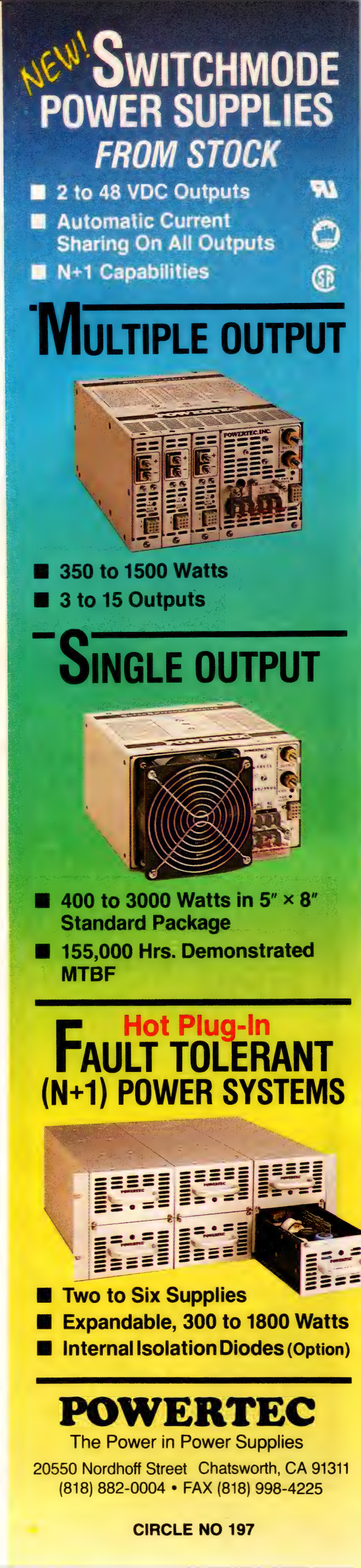
Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 658-9400.

Circle No. 404

Micropower CMOS Op Amps

- *Available in dual and quad versions*
- *Require only 40 μA/amplifier*

The LPC660 (quad) and LPC662 (dual) op amps offer a number of important features for low-power and battery-operated applications. These features include a supply-current requirement of only 40 μA/am-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CIRCLE NO 197

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Only two devices provide a complete 32-kilobyte memory solution. Plus they feature built-in address latches and directly interface with 80386 cache controllers, eliminating the need for off-chip logic and further reducing chip count. This means you save valuable board space and cost while increasing performance and reliability.

Micron cache SRAMs are also user configurable as an 8K × 16 or a dual 4K × 16 device to support direct mapped or 2-way set associative cache schemes. And like all Micron memory products, they're backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

So call us today at 1-208-386-3900, and start boosting your processor speed and efficiency with cold, hard cache.

Micron. Working to improve your memory.

Intel* 386™ Microprocessor	Micron MT56C0816 Cache Data SRAM*	
Clock Speed	Access Time	Max Output Enable Time
33 MHz	25ns	10ns
25 MHz	35ns	13ns

*All timing rated at 100 pF loads. The MT56C0816 is available in a 52-pin plastic leaded chip carrier (PLCC).

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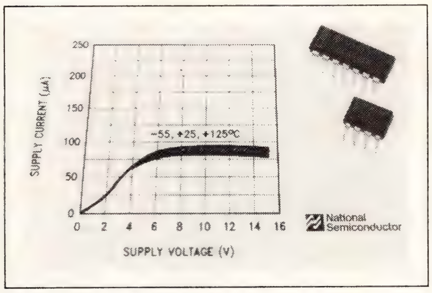
MICRON
TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 386-3900

CIRCLE NO 198



plifier, a rail-to-rail output swing, and a low input-bias current. Fabricated in the company's silicon-gate CMOS process, the op amps need only 40 femto-amps of input-bias current/amplifier. Moreover, the devices operate from a single supply of 5 to 15V and are characterized for use over the industrial temperature range of −40 to +85°C. The LP660 (14-pin DIP) and LP662 (8-pin DIP) cost $1.40 and $0.90, respectively (100).

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2281.

Circle No. 405

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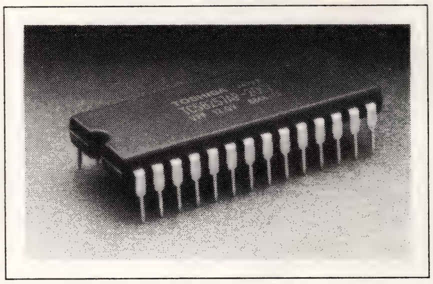
CIRCLE NO 199



256k-Bit EEPROM

- *Access time is 200 nsec*
- *Field reprogrammable via modem*

The TC58257AP is a 256k-bit flash EEPROM designed for remote downloadable applications such as point-of-sale terminals, printer fonts, memory cards, and telecommunications. The EEPROM is reprogrammable in circuit via a modem, thus avoiding costly on-site updates. The device, which electrically erases all prerecorded information, features an access time of 200 nsec, an operating current of 30 mA at 5.9 MHz, and a standby current of 100 µA. The TC58257AP comes in a 28-pin plastic DIP and is pin compatible with JEDEC-standard EPROMs, one-time-programmable devices, and ROMs. $10.95 (1000).

Toshiba Electronic Components, 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000.

Circle No. 406

1M-Bit Static RAM

- *Organized as 64k × 16 bits*
- *Access time is 55 nsec*

Fully compliant with MIL-STD-883C, the MEM-84002 is a 1M-bit static RAM characterized for operation over the military temperature

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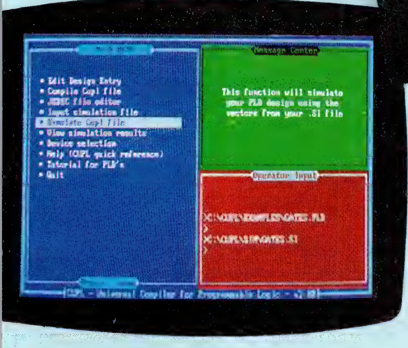

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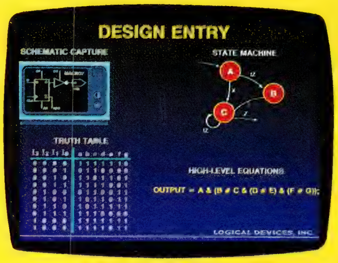
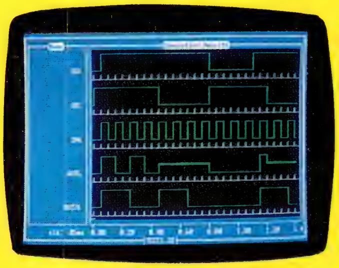


OUTPUT = A & (B # C & (D # E) & (F # G));

- ▲ ***Allows design entry with popular schematic capture packages from OrCAD, P-CAD, Wintek or Omation.***



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CIRCLE NO 200

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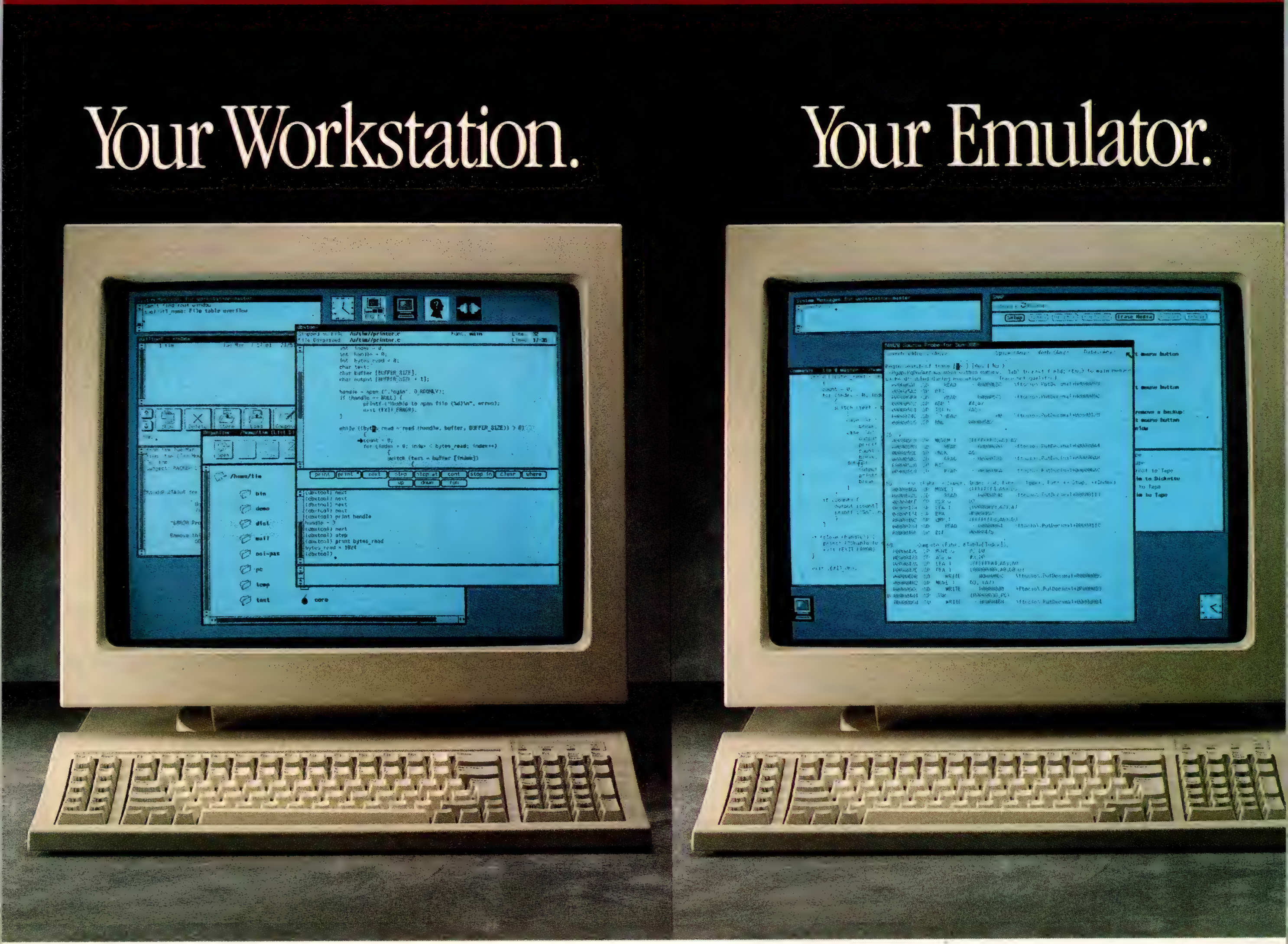

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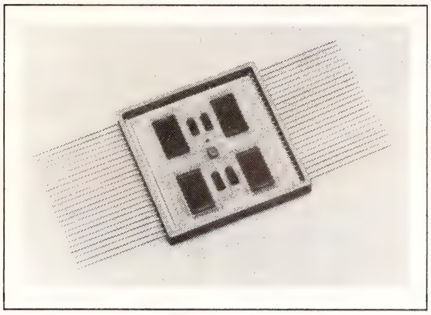

range of −55 to +125°C. Organized as 64k×16 bits, the MEM-84002 features a maximum access time of 55 nsec. The hybrid circuit contains four TTL-compatible, 32k×8-bit static RAM chips. Data transfers are made using 16 address lines; 16 data lines; and standard read, write, and enable lines. By using external decoding, the static RAMs are fully expandable to any memory width or depth. The MEM-84002 operates from a single 5V supply, and a battery backup as low as 2V will prevent data loss under conditions of power failure. The hybrid comes in a 46-pin quad flatpack. $898 (100).

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5678.

Circle No. 407

Wideband Op Amp

- *Bandwidth is 40 MHz*
- *Settling time is 90 nsec*

The unity-gain-stable SP2541 op amp combines high-performance ac operation with dc precision. Dynamic specs include a gain-bandwidth product of 40 MHz, a slew rate of 280V/μsec, and a 10V-step settling time of 90 nsec to 0.1% (175 nsec to 0.01%). The SP2541's dc specs include an input resistance of 100 kΩ, a bias current of 3 μA, and an offset voltage of 0.8 mV. Balance pins are provided for applications requiring tighter offset voltages. The op amp needs no external frequency compensation. The SP2541 is available in a 14-pin ceramic DIP or a TO-8 metal can. $5.75 for commercial parts; $11.49 for military parts (100).

Sipex Corp, 6 Fortune Dr, Billerica, MA 01821. Phone (508) 663-9691. **Circle No. 408**

Sampling A/D Converters

- *12-bit resolution*
- *100-kHz sampling rate*

According to the company, the MAX163/164/167 family of sampling A/D converters has built-in, track-and-hold (T/H) circuits that rival separate S/H amplifiers in performance. Specifications include full-power bandwidth of 6 MHz, acquisition time of 1 μsec, aperture delay of 25 nsec, and jitter of < 50 psec. The 100-kHz sampling rate of the ADCs allows conversion of time-

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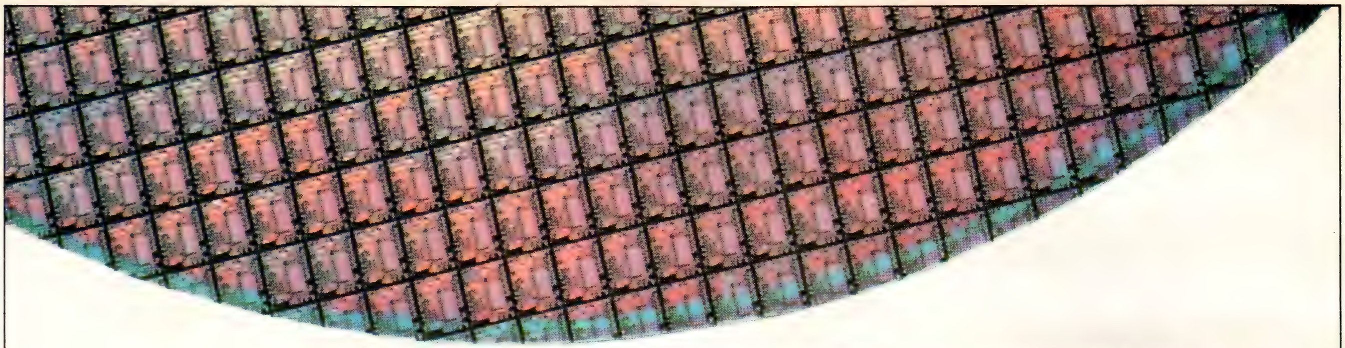

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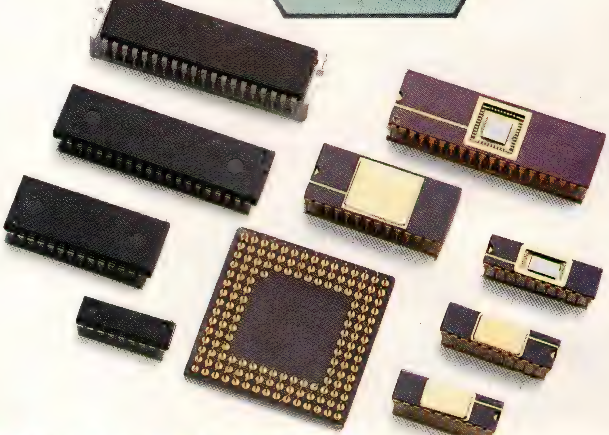
In order to maintain the good quality of production, Taicera is embarking on an aggressive plan to upgrade capabilities and improve the manufacturing. Currently, Taicera can provide interested customers with the following packages: Cerdip/ Sidebraze/Leadless Chip Carrier/Pin Grid Array/Flat Pack/Plastic Dip.



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CIRCLE NO 202

varying signals under 50 kHz at the Nyquist rate; and the 6-MHz bandwidth of the T/H circuit makes it possible to digitize signals to 6 MHz, using undersampling techniques. The three ADCs differ only in their analog-input range: The MAX163 accepts 0 to 5V inputs; the MAX164 accepts −5 to +5V inputs; and the MAX167 accepts −2.5 to +2.5V inputs. The devices use a standard μP interface and work with dual supplies of 5V and −12 to −15V. From $21.25 (100).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

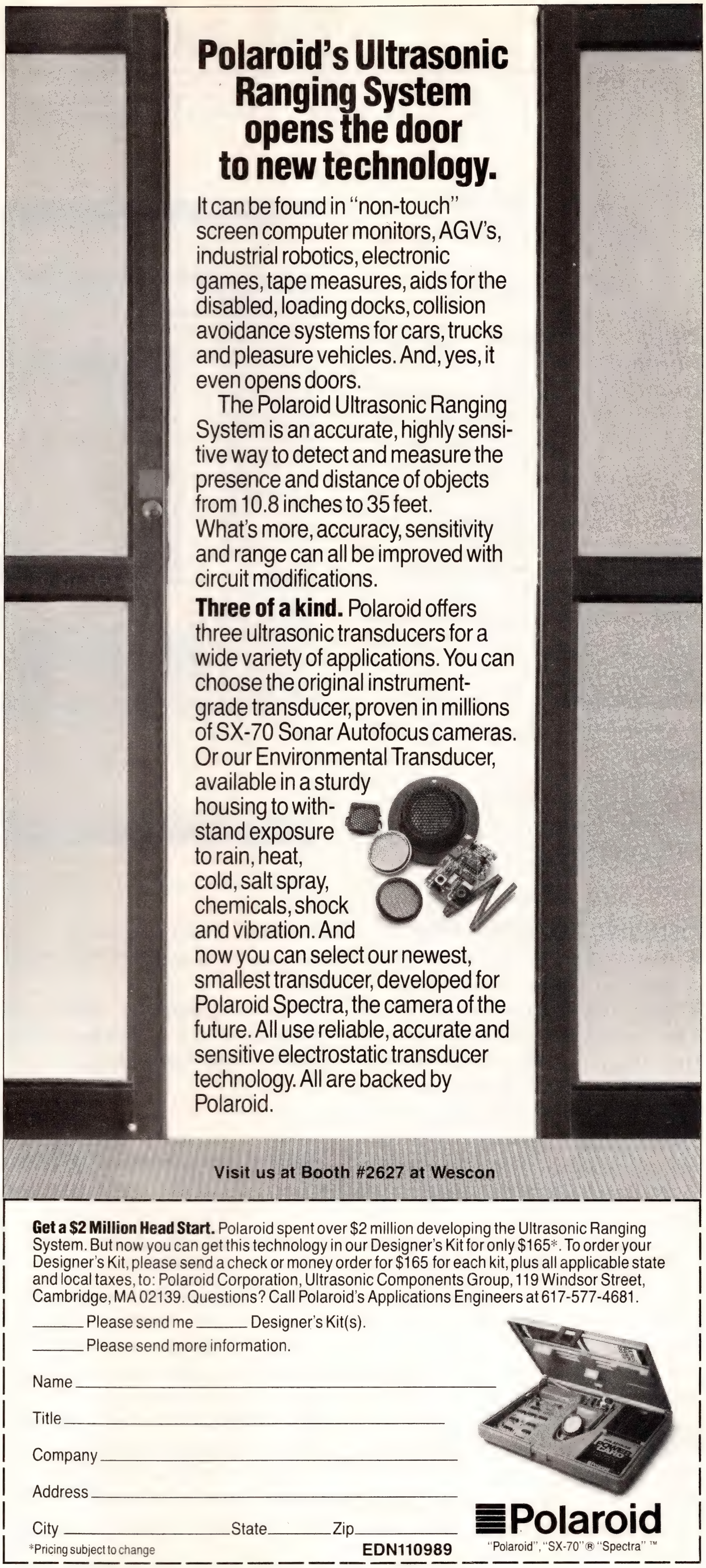
Circle No. 409

Single-Chip, Mass-Storage Controller

- *Works with the Micro Channel Architecture bus*
- *Provides interface for disk drives*

Fabricated in CMOS, the AIC-6190 handles the complex I/O interface between the Micro Channel Architecture bus and unintelligent mass-storage devices such as hard disks, floppy disks, tape drives, and optical drives. The device provides a single-chip answer to the problem of implementing multiple-chip data controllers in space-limited applications. The software-programmable AIC-6190 provides host bus control, buffer management, encode/decode, disk control, and data-format control functions. This high degree of integration eliminates the need for a separate disk-controller board and also provides cost and space savings in hard-disk applications. The AIC-6190, which allows two hard-disk cards or two embedded disk drives to be connected to the host bus, operates with NRZ data rates beyond 20M bps and a host data rate higher than 8M bytes/sec. The AIC-6190 is available in a 100-pin quad flatpack. $30 (OEM qty).

Adaptec, 691 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-8600. **Circle No. 410**



Polaroid's Ultrasonic Ranging System opens the door to new technology.

It can be found in "non-touch" screen computer monitors, AGV's, industrial robotics, electronic games, tape measures, aids for the disabled, loading docks, collision avoidance systems for cars, trucks and pleasure vehicles. And, yes, it even opens doors.

The Polaroid Ultrasonic Ranging System is an accurate, highly sensitive way to detect and measure the presence and distance of objects from 10.8 inches to 35 feet. What's more, accuracy, sensitivity and range can all be improved with circuit modifications.

Three of a kind. Polaroid offers three ultrasonic transducers for a wide variety of applications. You can choose the original instrument-grade transducer, proven in millions of SX-70 Sonar Autofocus cameras. Or our Environmental Transducer, available in a sturdy housing to withstand exposure to rain, heat, cold, salt spray, chemicals, shock and vibration. And now you can select our newest, smallest transducer, developed for Polaroid Spectra, the camera of the future. All use reliable, accurate and sensitive electrostatic transducer technology. All are backed by Polaroid.

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Get a $2 Million Head Start. Polaroid spent over $2 million developing the Ultrasonic Ranging System. But now you can get this technology in our Designer's Kit for only $165*. To order your Designer's Kit, please send a check or money order for $165 for each kit, plus all applicable state and local taxes, to: Polaroid Corporation, Ultrasonic Components Group, 119 Windsor Street, Cambridge, MA 02139. Questions? Call Polaroid's Applications Engineers at 617-577-4681.

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CIRCLE NO 203

NEW PRODUCTS

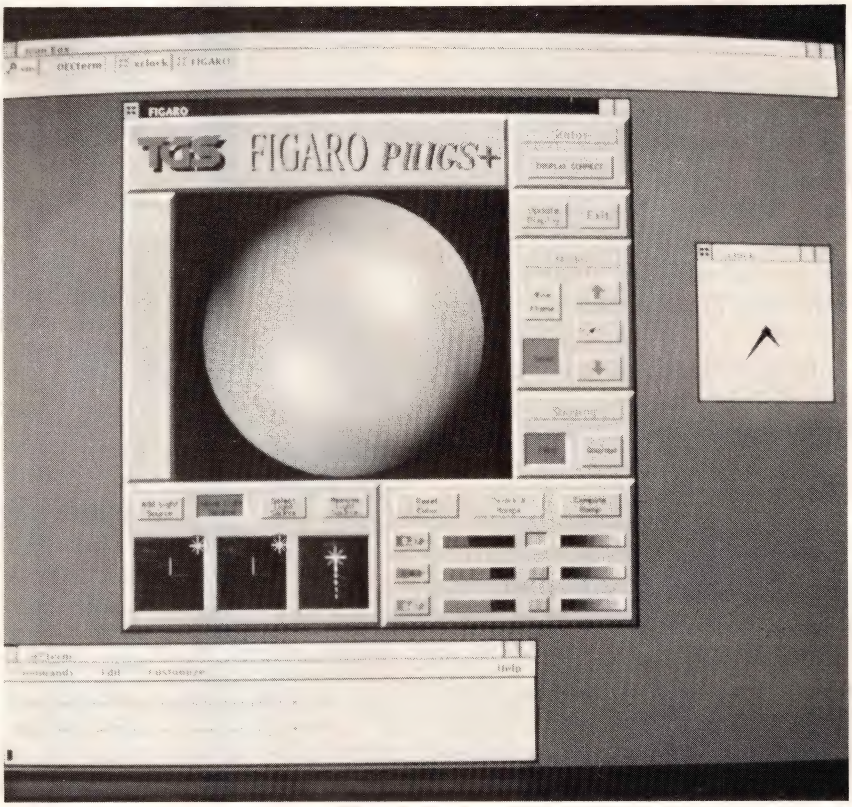
CAE & SOFTWARE DEVELOPMENT TOOLS

3-D Graphics For DEC

- *Implement the PHIGS graphical standard*
- *Run on DEC workstations under VMS or Ultrix*

Figaro+, a machine-independent implementation of PHIGS (Programmer's Hierarchical Interactive Graphics Standard), runs on a wide variety of computers and is now available for DEC workstations. It provides a library of graphical routines that run under DECwindows on systems that use either VMS or Ultrix operating systems. Figaro+ allows you to produce sophisticated 3-D CAD applications with lighting and shading features, geometric-modeling capability, and rapid display modification. From $3000 for workstations to $45,000 for supercomputers.

Template Graphics Software Inc, 9685 Scranton Rd, San Diego, CA 92121. Phone (619) 457-5359. FAX 619-452-2547. **Circle No. 362**



Parallelizing Ada Compiler

- *Automatically creates parallel/vector or nested parallel loops*
- *Tasks can run on multiple CPUs*

The Convex Ada compiler runs on the vendor's C200 series of supercomputers and analyzes Ada source code to find what portions of a problem can run in parallel. The compiler automatically creates parallel loops for problems that can run in parallel but cannot be vectorized; it creates parallel/vector loops when both parallelization and vectorization are possible; and it creates nested parallel loops when one of the outer loops can run in parallel, and the inner loops can be vectorized. The compiler has a task-spreading feature that allows Ada tasks to run on multiple CPUs. The Ada debugger has also been enhanced to simplify the debugging of both parallel and multitasking applications. From $30,000 for a C120 computer to $50,000 for a C240 machine.

Convex Computer Corp, 3000 Waterview Pkwy, Richardson, TX 75080. Phone (214) 497-4226. **Circle No. 363**

Worst-Case Stress Analyzer

- *Determines if a component will be overstressed in operation*
- *Accepts stress equations with as many as 200 characters*

SMA (Stress Margins Analyzer) is a worst-case analysis software package. It provides a worksheet format that lets you identify and analyze each component to determine whether it will be overstressed in its required range of operating conditions. The package can accept stress equations with as many as 200 characters and with 20 user-defined global variables that have min/max limits. The program solves for worst-case stress; if you change the global limits, SMA automatically updates the entire worksheet with the new limits. The package includes a derating library that lets you define deratings for each component type, style, and stress parameter. During worksheet data entry, you can display derating data via pop-up menus and then copy the data into the worksheet. The program provides extensive on-line help and works with any text printer. To run the program you'll need an IBM PC or compatible that has at least 320k bytes of memory and a graphics adapter card. $795.

Design/Analysis Consultants Inc, 2805 W Busch Blvd, Suite 202, Tampa, FL 33618. Phone (813) 933-0672. **Circle No. 364**

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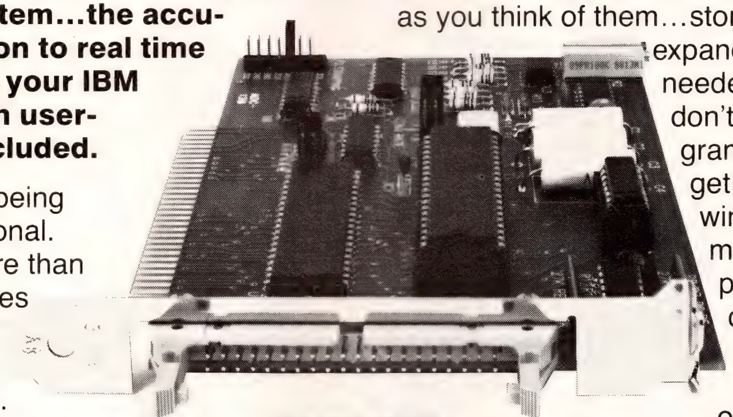

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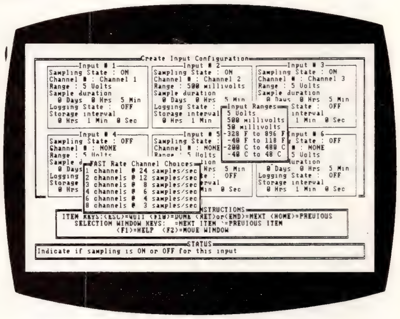

```
Create Input Configuration
Input # 1                    Input # 2                    Input # 3
Sampling State : ON          Sampling State : ON          Sampling State : ON
Channel # : Channel 1        Channel # : Channel 2        Channel # : Channel 3
Range : 5 Volts              Range : 500 millivolts       Range : 5 Volts
Sample duration              Sample duration              Sample duration
  0 Days  0 Hrs  5 Min         0 Days  0 Hrs  5 Min         0 Days  0 Hrs  5 Min
Logging State :  OFF         Logging State : Input Ranges State :  OFF
Storage interval             Storage interval 5 Volts     interval
  0 Hrs  1 Min  0 Sec          0 Hrs  1 Min   500 millivolts 1 Min  0 Sec
                                              50 millivolts
Input # 4                    Input # 5 -328 F to 896 F Input # 6
Sampling State : OFF         Sampling State   -40 F to 118 F State : OFF
Channel # : NONE             Channel # : NONE -200 C to 480 C # : NONE
Range : 5 Volts              Range : 5 Volts   -40 C to 48 C 5 Volts
Sample d FAST Rate Channel Choices  tion                 uration
  0 Days 1 channel  @ 24 samples/sec Hrs  5 Min         0 Days  0 Hrs  5 Min
Logging  2 channels @ 12 samples/sec te :  OFF         Logging State :  OFF
Storage  3 channels @  8 samples/sec rval              Storage interval
  0 Hrs  4 channels @  6 samples/sec Min  0 Sec          0 Hrs  1 Min  0 Sec
         6 channels @  4 samples/sec
         8 channels @  3 samples/sec INSTRUCTIONS
 ITEM KEYS:<ESC>=QUIT <F10>=DONE <RET>or<END>=NEXT <HOME>=PREVIOUS
    SELECTION WINDOW KEYS:  =NEXT ITEM `=PREVIOUS ITEM
            <F1>=HELP  <F2>=MOVE WINDOW
STATUS
Indicate if sampling is ON or OFF for this input
```

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A0012

CIRCLE NO 204

PC Data Security System

- *Encrypts all files in a protected directory*
- *Provides an audit trail of attempts to access protected data*

DataSentry II combines menu-driven software with an external, removable hardware key to provide multilevel security for sensitive files. The hardware key plugs into the printer port and is transparent to printer operations. The software lets you designate directories as protected, and automatically encrypts data that is written to any protected file. Provided that you log on with the correct user ID and password, the data is automatically decrypted when you access a protected file. You can also manually request encryption of a file before transmitting it via a modem; decryption at the receiving station requires a matched hardware key. The system can use either DES (Data Encryption Standard) encryption or the vendor's proprietary encryption algorithm, which is somewhat faster than the DES algorithm. When you store a file to a protected directory, the system automatically overwrites the memory space that held the file; likewise, when you delete a protected file from the disk, the system overwrites the disk sectors previously occupied by the file. These measures prevent any unauthorized attempt to recover sensitive data with the aid of "undelete" utility programs. Managerial hardware keys can override the action of user keys to allow reassignment of user IDs and passwords, and a master key can protect the system against unauthorized access attempts by means of a stolen hardware key. $195.

Rainbow Technologies, 18011-A Mitchell S, Irvine, CA 92714. Phone (714) 261-0228. FAX 714-261-0260.

Circle No. 365

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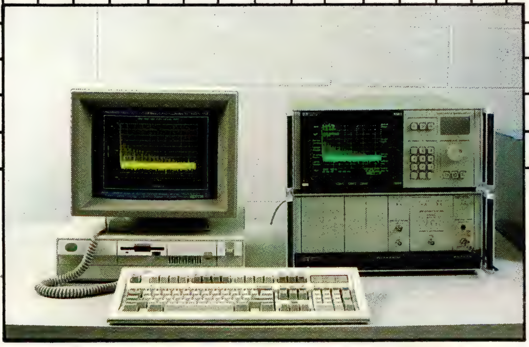
See us at Wescon/89 Booth 902
CIRCLE NO 205

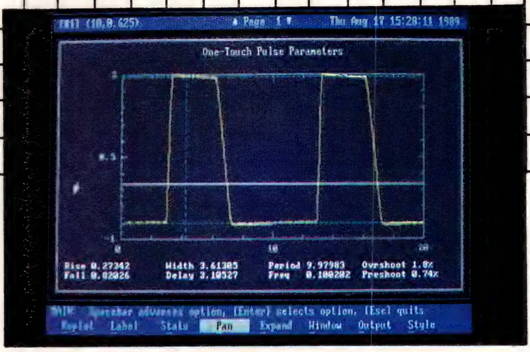
C++ Tool Set

- *Provides all features of AT&T's release 2.0*
- *Runs under SunOS*

Sun C++ 2.0, an object-oriented software-development system, includes all of the new features provided by AT&T's release 2.0 of the C++ language. The supporting tool kit includes a window-based debugger that shows you the C++ source code as well as the corresponding object code, the register contents, and other pertinent information. The package takes full advantage of SunOS features, such as dynamic linking and shared libraries, and includes additional libraries of routines to facilitate stream I/O,

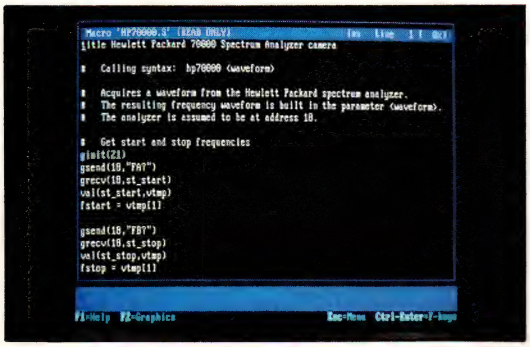


Integrated Data Acquisition



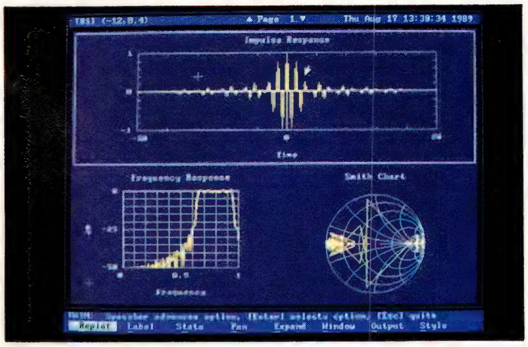
```
Rise 0.27342     Width 3.61305     Period 9.97983    Ovrshoot 1.8%
Fall 0.02026     Delay 3.10527     Freq   0.100202   Preshoot 0.74%
```

Data Analysis



```
title Hewlett Packard 70000 Spectrum Analyzer camera

#   Calling syntax:  hp70000 <waveform>

#   Acquires a waveform from the Hewlett Packard spectrum analyzer.
#   The resulting frequency waveform is built in the parameter <waveform>.
#   The analyzer is assumed to be at address 18.

#   Get start and stop frequencies
ginit(21)
gsend(18,"FA?")
grecv(18,st_start)
val(st_start,vtmp)
fstart = vtmp[1]

gsend(18,"FB?")
grecv(18,st_stop)
val(st_stop,vtmp)
fstop = vtmp[1]
```

Full Macro Capability



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CIRCLE NO 207

CAE & SOFTWARE DEVELOPMENT TOOLS

complex arithmetic, and tasking. The development system works with the vendor's Network Software Environment (NSE), a configuration-management system. $1200.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX 415-969-9131. **Circle No. 366**

Disk Diagnostic Program

- *Detects impending failures of a hard-disk drive*
- *Reduces access times by optimizing the interleave factor*

The Disk Technician diagnostic program detects bad sectors on a hard drive and corrects soft errors. According to the manufacturer, the program finds 100% of the bad sectors that are discovered by drive manufacturers' more elaborate factory test equipment. The program can optimize the interleave factor and thereby increase access speed by as much as five times. Disk Technician can also detect impending failures of the drive, drive motor, or controller board by detecting specific patterns of erratic operation. The Advanced version of the program is fully automatic and can test and repair two hard-disk drives with a single command; it stores the results in a file for future viewing by maintenance personnel. The Professional version provides manual operation for technical personnel who need more control over the testing process. Advanced version, $59.95; Professional version (including head-parking utility), $149.95.

Prime Solutions, 1940 Garnet Ave, San Diego, CA 92109. Phone (619) 274-5000. FAX 619-272-4008. **Circle No. 367**

Network Simulator

- *Lets you simulate and analyze networks*
- *Offers a user-extendable model library*

Bones (Block-Oriented Network Simulator) provides a graphical environment for the description and simulation of a wide range of communication networks such as local and wide-area networks, packet-switched networks, Integrated Services Digital Network, store-and-forward networks, and computer buses and architectures. You construct the model with the aid of building blocks from the model library; the specifications include network topology, traffic volume, data structures, and protocol functions. You can also write components of a network model in C and incorporate them into a Bones model. The simulator software

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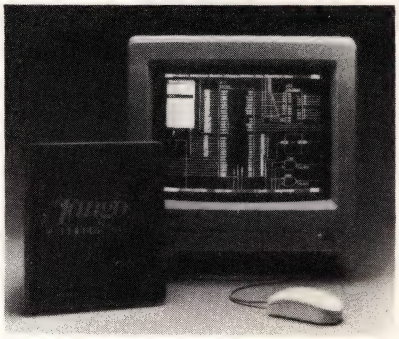
CIRCLE NO 208

translates the finished model into a C program, executes an event-driven Monte Carlo simulation, computes statistical measures of performance, and displays the results graphically. The hierarchical nature of the models allows the incremental compilation of simulation models, thereby eliminating long delays when you have to make changes. The simulator runs on Sun-3 and Sun-4 workstations under SunOS version 4.0.1. The vendor recommends at least 8M bytes of memory, 200M bytes of disk space, and an Apple or HP laser printer. From $20,000 to $25,000, depending on host configuration.

Comdisco Systems Inc, 919 E Hillsdale Blvd, Foster City, CA 94404. Phone (415) 421-1800. FAX 415-421-1800. **Circle No. 368**



Schematic-Capture Tool

- *Component libraries contain more than 5000 parts*
- *Library includes TTL, CMOS, ECL, PLDs, and linear ICs.*

Tango-Schematic Series II is a greatly enhanced version of the vendor's schematic-capture tool. The tool is completely compatible with the vendor's pc-board layout and autorouter products. It allows you to draw schematics on the screen, create new library components, perform design-rule checking, generate net lists, and output hard copy by means of a graphics printer or pen plotter. The enhanced component library contains more than 5000 parts in technologies such as TTL, CMOS, ECL, PLDs, linear ICs, and μPs. You can create flat drawings or hierarchical designs with as many as 99 sheets per level and with a large number of levels. The program displays a prompt line that gives brief instructions for the current operation; an on-line help feature provides more than 100 screens of context-sensitive information. The documentation includes a tutorial, examples, a command summary, and an index. $495.

Accel Technologies Inc, 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. FAX 619-554-1019. **Circle No. 369**

Switching Power Supplies 8w-600w

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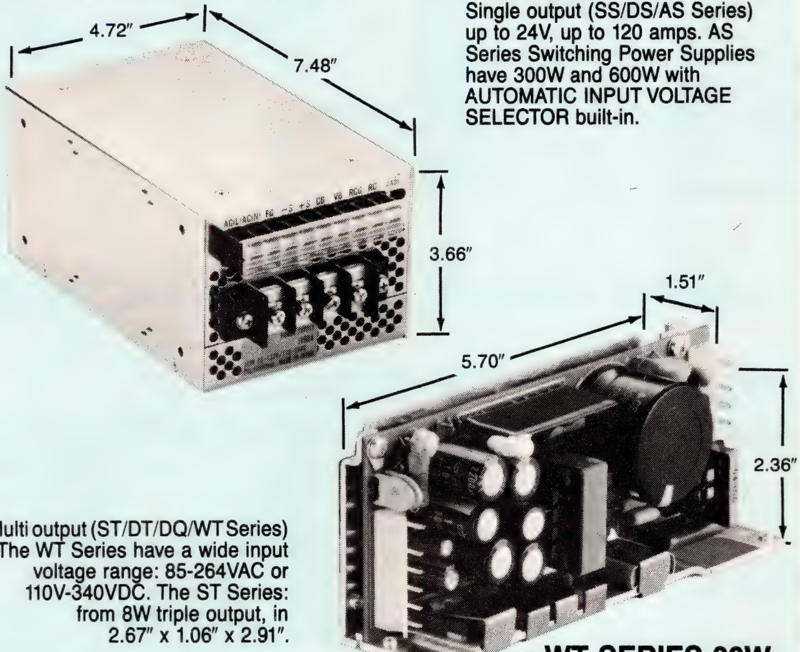

Multi output (ST/DT/DQ/WT Series) The WT Series have a wide input voltage range: 85-264VAC or 110V-340VDC. The ST Series: from 8W triple output, in 2.67″ x 1.06″ x 2.91″.

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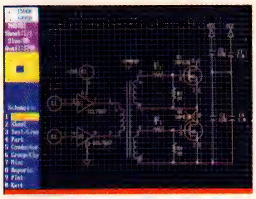
CIRCLE NO 209

NEW GENERATION OF LOGIC CAPTURE SOFTWARE

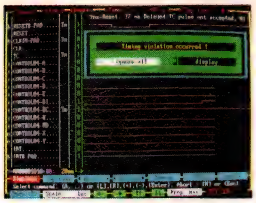


A New Generation of Logic Capture, PADS-LOGIC, is now available from CAD Software, Inc. PADS-LOGIC has a true multi-sheet, design oriented database which provides a very high level of performance for Electronic Engineers. Some of the systems features include: Automatic Reference Designations, Automatic Gating, powerful Macro Commands, interfaces to Logic Simulation, Circuit Analysis, and most CAD systems. Large circuit (250 sheets), and 100 layer level Hierarchical capability, enables the Logic Capturing of any size design. An Engineering Change Order (ECO) feature forwards changes made to the schematic to automatically update the PCB design; changes in the board layout, including Automatic Gate and Pin Swapping, and Component Renaming, are automatically backward incorporated to the original schematic.

A security key is not required. The software cost is $450.00.

Contact CAD Software, Inc., Littleton, MA
Inside MA: (508) 486-8929 or Outside MA: (800) 255-7814

PC-BASED ELECTRONIC DESIGN VERIFICATION



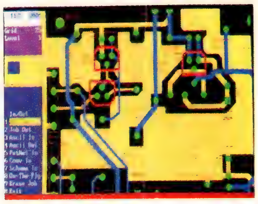
Engineers can verify their designs, and reduce Hardware breadboarding, through the use of CAD Software, Inc.'s, Logic Simulation and Circuit Analysis Programs.

PADS-SUSIE, is a Digital Simulator with Timing, Functional & Glitch Mode verification modes. Simulation passes can be made at either this Board Level, or the Hierarchical Level.

PADS CIRCUIT ANALYSIS, for Analog Circuit Analysis, is based upon Microsim Corporation's highly successful version P-Spice, and includes a tightly coupled Analog and Digital Mixed Mode Simulator.

Contact CAD Software, Inc., Littleton, MA
Inside MA: (508) 486-8929 or Outside MA: (800) 255-7814

PADS-PCB VERSION 3.13 NOW SHIPPING



Version 3.13 of PADS-PCB, the highly popular PCB CAD System, is now being shipped. The Personal Computer-Based PADS—PCB System has a Very Large Board, (450 Equivalent per ICs) Capability, with up to 30 layers. All technologies, including Digital, Analog, Multilayer and SMT, are supported. Both Automatic & Interactive Placement and Routing Algorithms are available. Automatic Design Rules Checking is included. ($975.00)

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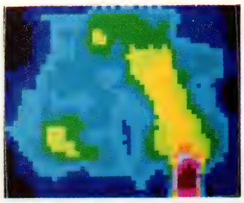
PADS-THERMAL SOFTWARE



A Printed Circuit Board Thermal Analysis software package is available from CAD Software of Littleton, MA. This software, (PADS-THERMAL), is used to evaluate the Thermal effects on a board, while operating in various packaging environments, including closed containers with variable airflows, open containers, components on top and bottom layer of boards, and other constraints.

A unique feature allows the relocation of the Parts on the board, in order that different locations of heat generating parts can be evaluated.

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PADS-PUSH N' SHOVE (New), has been configured for those Engineers and Designers that have critical circuits on their boards, such as high speed circuits, ECL, Bus lines, or Analog Boards, where the designer wants precise control over the track position, yet wants the power of an autorouter to quickly route the connections. ($1,495.00)

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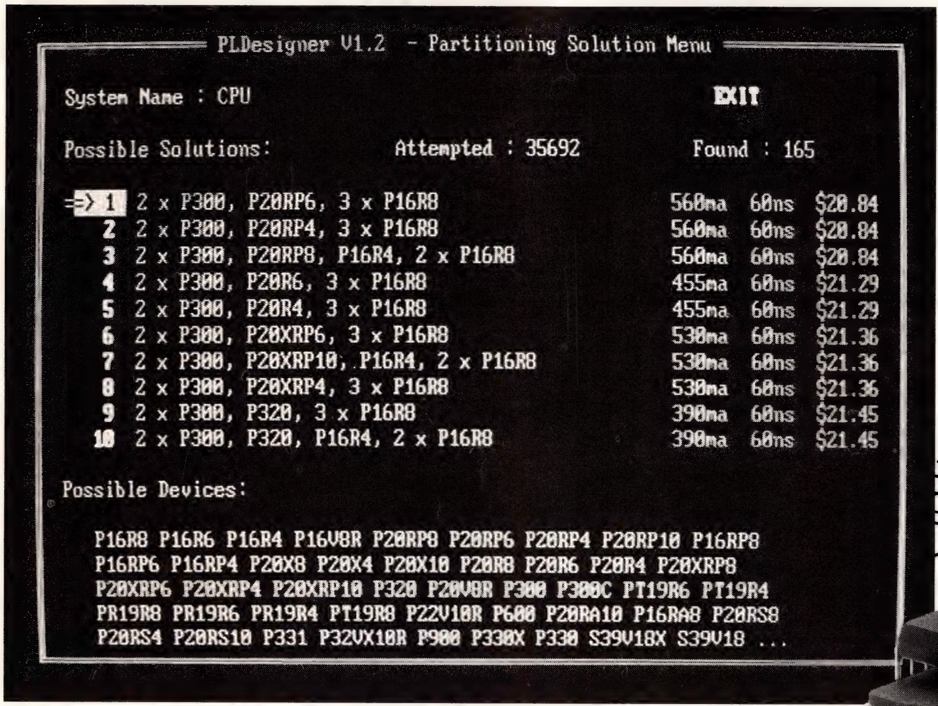
Debugger For TI34010

- *Fully compatible with TI's SDB340 debugger*
- *Symbolic debugging facilities for TI34010-based graphics software*

GSpot (Graphics System Processor Operating Tool) is a window-oriented, symbolic debugger for programs written in C or assembly language that run on a TI34010 graphics processor. The source-code window shares the screen with a command-line window and, if watchpoints are defined, with a watch window. You can modify registers by means of a command line or a cursor-controlled editor. GSpot can access global symbols via the COFF (Common Object File Format) executable file, and it lets you refer to these symbols in your commands. The tool provides full source-level debugging facilities that allow you to step through programs written in C, in a mix of C and assembly language, or in assembly language only. Another feature is GSpot's ability to run as a TSR (Terminate and Stay Resident) program so you can switch back and forth between GSpot and another debugger such as CodeView. GSpot fully complies with the Texas Instruments Graphics Architecture (TIGA) standard. To run the program, you'll need an IBM PC or compatible that has 58k bytes (with expanded memory) or 100k bytes (without expanded memory) of free memory, a hard disk, and MS-DOS 3.0 or later version. $995.

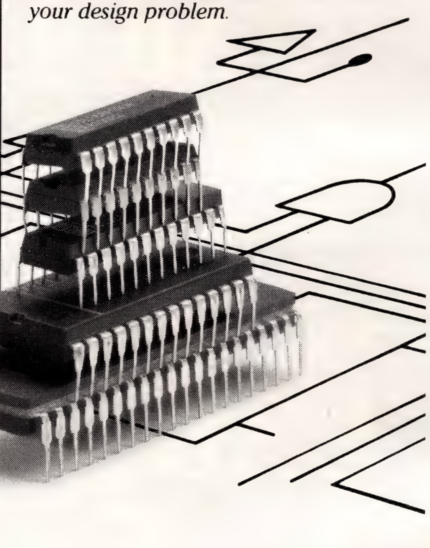
Pixelab Inc, 4513 Lincoln Ave, Suite 105, Lisle, IL 60532. Phone (312) 960-9339. FAX 312-960-9396.

Circle No. 370



```
PLDesigner V1.2  - Partitioning Solution Menu

System Name : CPU                                      EXIT

Possible Solutions:          Attempted : 35692        Found : 165

=> 1  2 x P300, P20RP6, 3 x P16R8                  560ma  60ns  $20.84
   2  2 x P300, P20RP4, 3 x P16R8                  560ma  60ns  $20.84
   3  2 x P300, P20RP8, P16R4, 2 x P16R8           560ma  60ns  $20.84
   4  2 x P300, P20R6, 3 x P16R8                   455ma  60ns  $21.29
   5  2 x P300, P20R4, 3 x P16R8                   455ma  60ns  $21.29
   6  2 x P300, P20XRP6, 3 x P16R8                 530ma  60ns  $21.36
   7  2 x P300, P20XRP10, P16R4, 2 x P16R8         530ma  60ns  $21.36
   8  2 x P300, P20XRP4, 3 x P16R8                 530ma  60ns  $21.36
   9  2 x P300, P320, 3 x P16R8                    390ma  60ns  $21.45
  10  2 x P300, P320, P16R4, 2 x P16R8             390ma  60ns  $21.45

Possible Devices:

  P16R8 P16R6 P16R4 P16V8R P20RP8 P20RP6 P20RP4 P20RP10 P16RP8
  P16RP6 P16RP4 P20X8 P20X4 P20X10 P20R8 P20R6 P20R4 P20XRP8
  P20XRP6 P20XRP4 P20XRP10 P320 P20V8R P300 P300C PT19R6 PT19R4
  PR19R8 PR19R6 PR19R4 PT19R8 P22V10R P600 P20RA10 P16RA8 P20RS8
  P20RS4 P20RS10 P331 P32VX10R P900 P330X P330 S39V18X S39V18 ...
```

PLDesigner uses your design philosophy when scanning its library of over 2500 different parts. Possible devices have architectures appropriate to implement the design. Attempted solutions are the combinations of possible devices. Of these combinations, 165 viable solutions were found. You can then choose from the top ten implementations displayed. Power consumption, propagation delay and estimated cost given for each solution ensure that the final implementation you select is the most rigorous solution for your design problem.



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The intelligence of PLDesigner lets you concentrate on your design, without becoming an expert on hundreds of device architectures.

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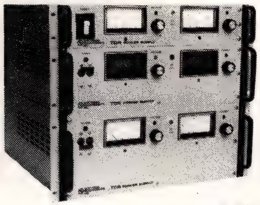

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- DC outputs variable over full range of 0 to 7.5 V DC through 0 to 2,500 V DC
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- Complies with VDE 875-N and VDE 871-A
- 5-year warranty

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- 3 power ranges 2,500 W- 5,000 W - 10,000 W
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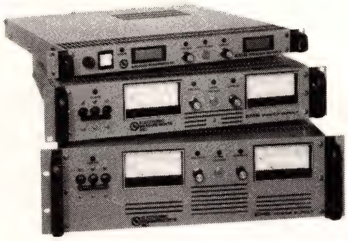

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CIRCLE NO 213

CAE & SOFTWARE DEVELOPMENT TOOLS

VHDL Simulator

- *Runs on a variety of workstations*
- *Lets you monitor simulator action and make quick fixes*

Zycad System VHDL (VHSIC Hardware Description Language), a software simulator that runs on workstations such as Apollo, DEC, and Sun computers, compiles VHDL specifications in an executable model. Because the simulator is interactive, you can monitor the action inside the model, stop the simulation at any time, and make changes to the model before continuing (or restarting) the simulation. The package includes a source-level debugger that provides line-by-line control over simulation runs. The postprocessor can automatically compare results from different simulation runs, examine the number of contentions that occur on a bus, or analyze the time spent in executing specified instructions. An optional developer kit includes a syntax-directed editor that provides on-line help, syntax templates, and pull-down menus. Zycad System VHDL, $40,000; VHDL developer option, $10,000.

Zycad Corp, 1380 Willow Rd, Menlo Park, CA 94025. Phone (415) 688-7400. FAX 415-688-7550.

Circle No. 371

Comprehensive CASE Tool

- *Multiuser, multiproject design tool for graphic workstations*
- *Uses vendor's Structured Method and generates Ada, C, or Pascal*

Cradle (Controlled Requirements for Analysis and Design with Logistic Execution) is a comprehensive CASE (computer-aided software engineering) tool for the design of real-time and commercial software systems. It runs on Apollo workstations under Unix, and it automatically generates code in Ada, C, or Pascal from structure diagrams, module specifications, and data-dictionary entities. The system provides users with access to past and current projects, and it ensures data integrity by preventing simultaneous file updating by multiple users. Further, a system of encrypted passwords and authorization levels defines each team member's access rights. The graphics editor has a built-in syntax-checking feature so that generating a syntactically incorrect diagram is impossible; cross checking ensures the consistency of the total system. The package also includes a configullration-management feature that handles change requests in a controlled manner and ensures that changes are reflected in all of the pertinent files and databases. From $12,500 for a 3-user version.

Yourdon Inc, 1501 Broadway, New York, NY 10036. Phone (212) 391-2828. FAX 212-869-5826.

Circle No. 372

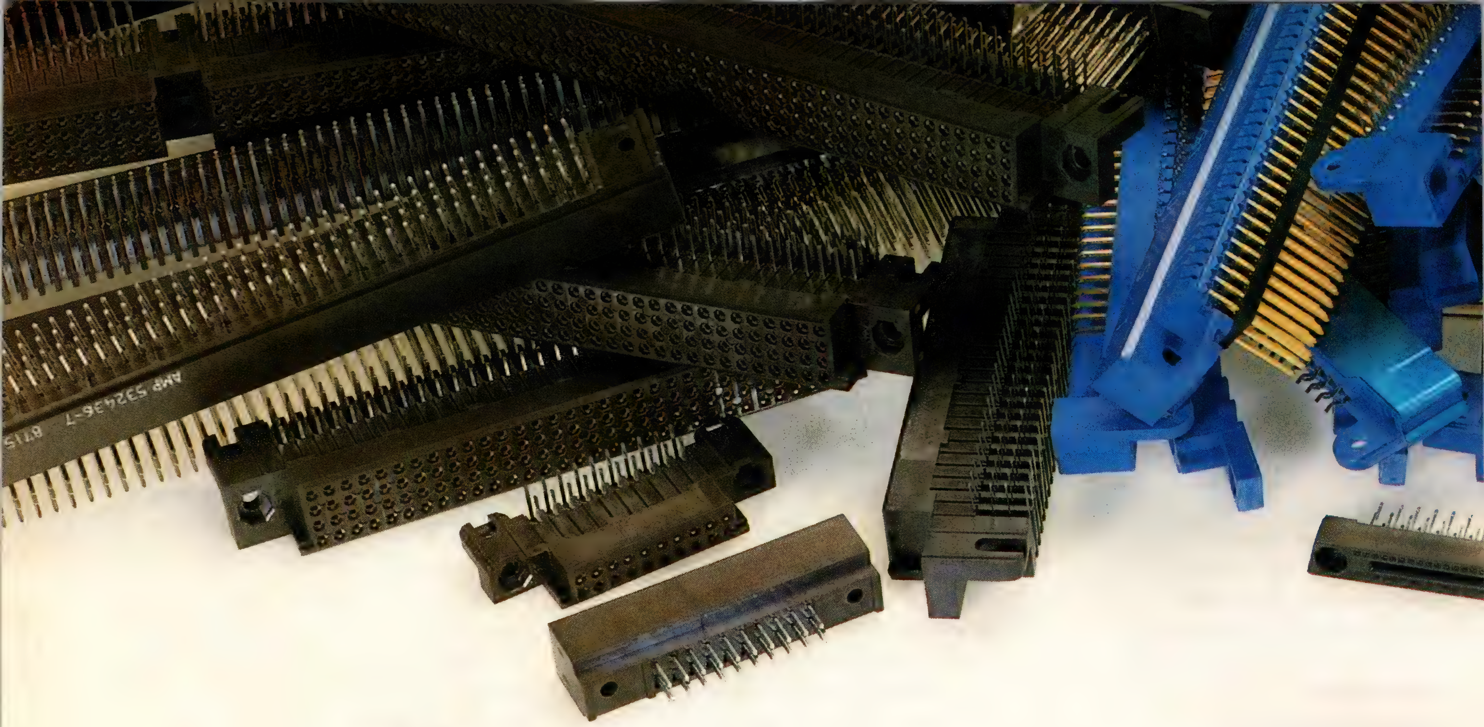
Graphics Interface

- *Allows character-based programs to generate windows*
- *Works with Macintosh and OS/2 machines*

A new version of XVT (Extensible Virtual Toolkit) allows designers of character-based applications to provide windowing, pull-down menus, dialog boxes, scroll bars, and other graphical-interface features. The same application source code works with Windows, Presentation Manager, and Macintosh graphical interfaces. Because XVT can handle many programming details and can make an XVT application look like a Macintosh, Windows, or Presentation Manager application, a single version of your source code is portable to any of these operating environments. The Windows, Presentation Manager, Macintosh, and character-based versions of XVT cost $595 each.

Graphic Software Systems Inc, 9590 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 641-2200. FAX 503-643-8642.

Circle No. 373



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It takes a lot to keep our two-piece connector customers happy. Reliability. Quality. Availability.

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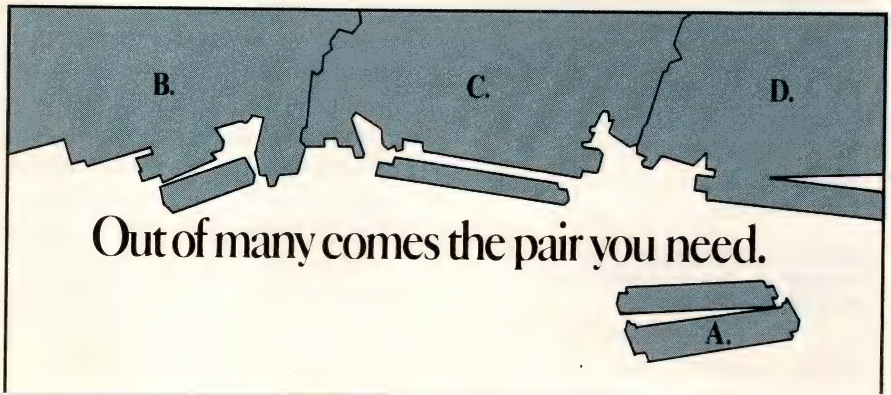
B.
C.
D.
Out of many comes the pair you need.
A.

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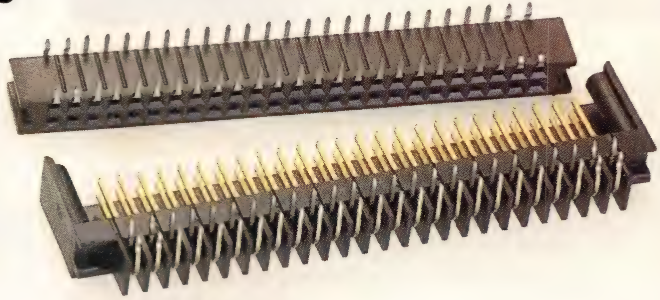
the pair you need.



very forgiving of pin angle during mating. Very reliable. And available on 0.100″, 0.075″, and 0.050″ CLs, with microminiature coax. MIL-C-55302s available as well.

D. And Eurocards, compatible with DIN 41612 types, available in 1/2s, reverses, expanded 2 and 3 row specials to 150 positions. Made worldwide by AMP, available nearby.

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For information on AMPMODU Two-Piece Connectors or others in our lineup, call the AMP Information Center, 1-800-522-6752. For characterized backplane assemblies, contact AMP Packaging Systems Inc., P.O. Box 9400, Austin, Texas 78766, (512) 244-5100, or your AMP Sales Engineer. AMP Incorporated, Harrisburg, PA 17105-3608.

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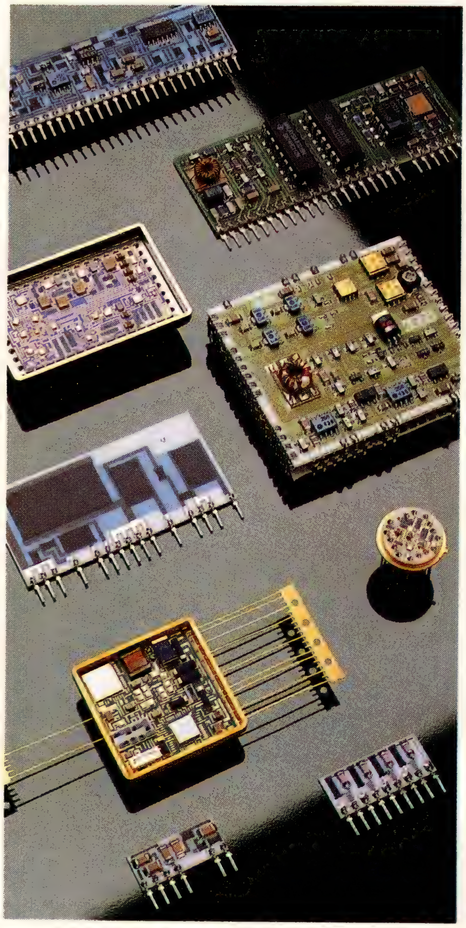

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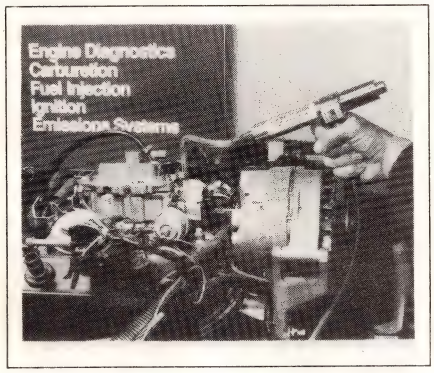


Probe That Supplies Hot And Cold Air

- *Operates from standard-shop, compressed-air supply*
- *Instantly produces air at 0 and 160°F*

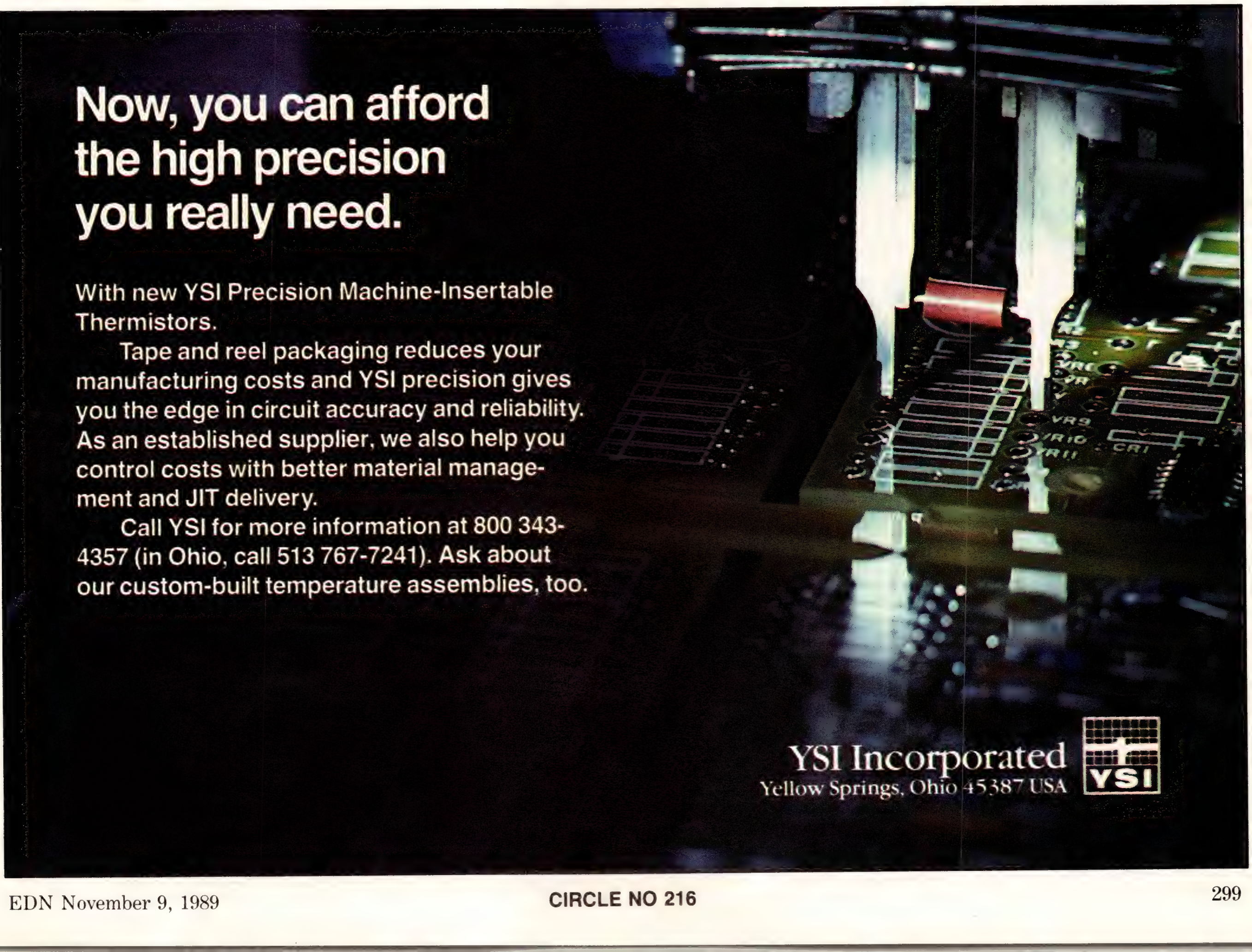
Although intended to test controls for internal-combustion engines (for example, automatic chokes), the Model 351-60 temperature sensor/choke tester will find use in testing purely electronic products. The handheld unit can deliver a blast of 0 or 160°F air using only a standard-shop air supply of 15 cfm at a gauge pressure of 80 to 100 psi. The hot and cold air is available instantly. $92.50, including a fitting and tubing.

Vortec Corp, 10125 Carver Rd, Cincinnati, OH 45242. Phone (800) 441-7475. **Circle No. 351**

MIL-STD-1553 Bus Analyzer

- *Complies with MIL-T-28800D for flightline operation*
- *Allows complete remote-terminal testing of the 1553 bus*

The ABA 503 bus analyzer meets the environmental requirements of MIL-STD-28800D Class 2, qualifying it for use in flightline testing of MIL-STD-1553 systems. The analyzer, which is based on the vendor's bench and production-test 1553 analyzers (ABA 500, 501, and 502), allows complete remote-terminal testing of the 1553 bus. The unit provides two methods of storing large amounts of data: a 360k-byte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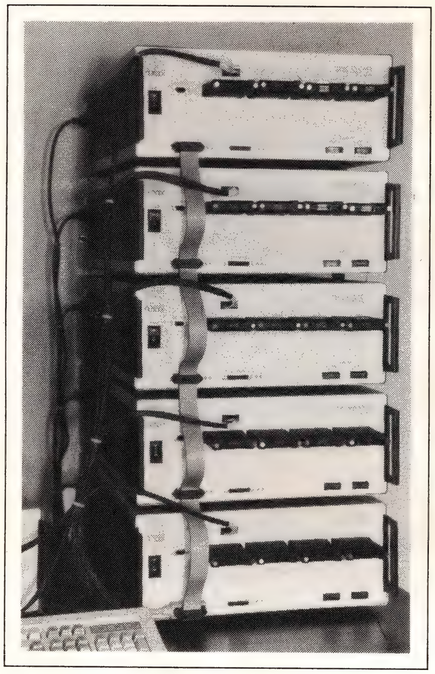
CIRCLE NO 216

RAM pack, which emulates an MS-DOS floppy-disk drive, and a ruggedized 20M-byte hard disk. $40,000 to $54,000. Delivery, 12 weeks ARO.

Interface Technology, 2100 E Alosta Ave, Glendora, CA 91740. Phone (818) 914-2741. FAX 818-335-8346. **Circle No. 352**

1-GHz Logic-Timing Analyzers

- *Expandable to 448 channels*
- *Use IBM PC/AT-compatible computer as host*



The T-132W and T-132EM are very high-speed logic-timing analyzers. The T-132W allows measurements with 4-nsec resolution on 32 channels with 4k words of memory, measurements with 2-nsec resolution on 16 channels with 8k words of memory, and measurements with 2-nsec resolution on eight channels with 16k words of memory. The T-132EM has 500 times the memory depth of the T-132W and in addition, allows 1-GHz acquisition on eight channels with 8M words of memory. You can add synchronized units triggering at 200 MHz to a maximum of 448 channels with 8M words of memory. T-132W, $22,750; T-132EM, $90,000; 8-channel probe sets, $1450.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479. **Circle No. 353**

ASIC Verifier

- *Stores 592k vectors for 128 pins*
- *Operates to more than 100 MHz*

The Topaz-V_A ASIC-verification system can store very large sets of test vectors for high pin-count devices. For a 128-pin device, the vector set can contain 592k vectors; for a 64-pin device, the vector set can contain more than 1 million vectors. The system also incorporates a high-performance parametric meas-

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CIRCLE NO 219

urement unit, the inclusion of which does not compromise other specifications. Maximum test rate is 110 MHz. Pin-to-pin timing skew is ±500 psec, and driver slew rate is 1.5V/nsec. The unit supports the IEEE P1149.1 testability specification, which allows the unit to test devices containing scannable latches. A 32-pin configuration sells for $101,000; a 320-pin system sells for $472,000.

Hilevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (800) 541-2742. FAX 714-727-2101.

Circle No. 354

IEEE-488 Interfaces For Macintoshes

- *Support 800k-byte/sec transfers on Mac II*
- *Include desk-accessory software*

The MacAdios 488s is an IEEE-488 interface that connects to the SCSI port of an Apple Macintosh Plus, SE, or II personal computer. The MacAdios 488n plugs into the Nubus of "slotted" Macintoshes. The SCSI interface supports 150k-byte/sec transfers; the Nubus unit supports transfers at 800k bytes/sec. Desk-accessory software enables you to control IEEE-488 instruments without additional software. It also permits you to record instrument-control "scripts" and save them to disk. A set of high-level-language-compatible drivers, MacDriver488, lets you incorporate instrument-control sequences in your own programs, even ones written in Hypertalk. MacAdios 488s, $795; MacAdios 488n, $595.

GW Instruments Inc, 35 Medford St, Somerville, MA 02143. Phone (617) 625-4096. FAX 617-625-1322.

Circle No. 355

5-Slot, C-Size VXIbus Mainframe

- *Has removable top to facilitate probing*
- *Provides 50W/slot; supplies forced air for cooling*

The VXI-1000 is a 5-slot mainframe for vertically or horizontally oriented, C-size VXIbus cards. The 7-in.-high, 28-lb chassis also accommodates A- and B-size cards. The top cover is removable, permitting

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The oceans present some of this planet's most hostile environments. Hence, installations of the U.S. Navy's advanced shipboard Aegis System's instrumentation require special slide devices which protect electronic circuitry against the extremes of shock and vibration, while providing easy access for periodic trouble-shooting and maintenance. Jonathan's response to this problem was a unique aluminum slide specially designed for the system's vertical installations. With load capacities to 400 lbs., the foot-actuated slide features special shock block protective devices. A novel reliable locking mechanism also secures the slide in both the open and closed positions. ■ If your packaging problem involves access to electronic instrumentation in rugged, hostile environments, call Jonathan — our Application Engineering Group can design a dependable solution for you . . . at a very competitive price.

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The table below helps you select the connector best suited for your application.

Performance Class	Min. Plating Thickness	Mating Cycles	Harsh Environment Testing
III	8 Microinch	50	None
II	15 Microinch	400	4 Days
I	Consult Factory	500	21 Days

PANDUIT Eurocard *DIN* connectors are fully intermateable to *DIN* 41612, MIL-C-55302, BSI9525 and IEC 603-2 specifications. They provide compatibility with VMEbus, NUBUS, STEbus, MULTIBUS II, FUTUREBUS or CIMBUS. Panduit also offers:

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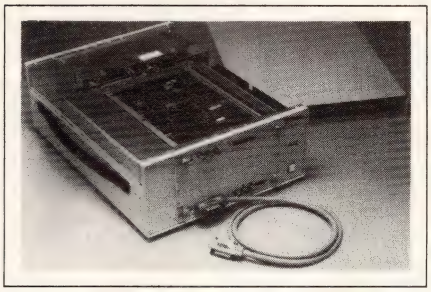
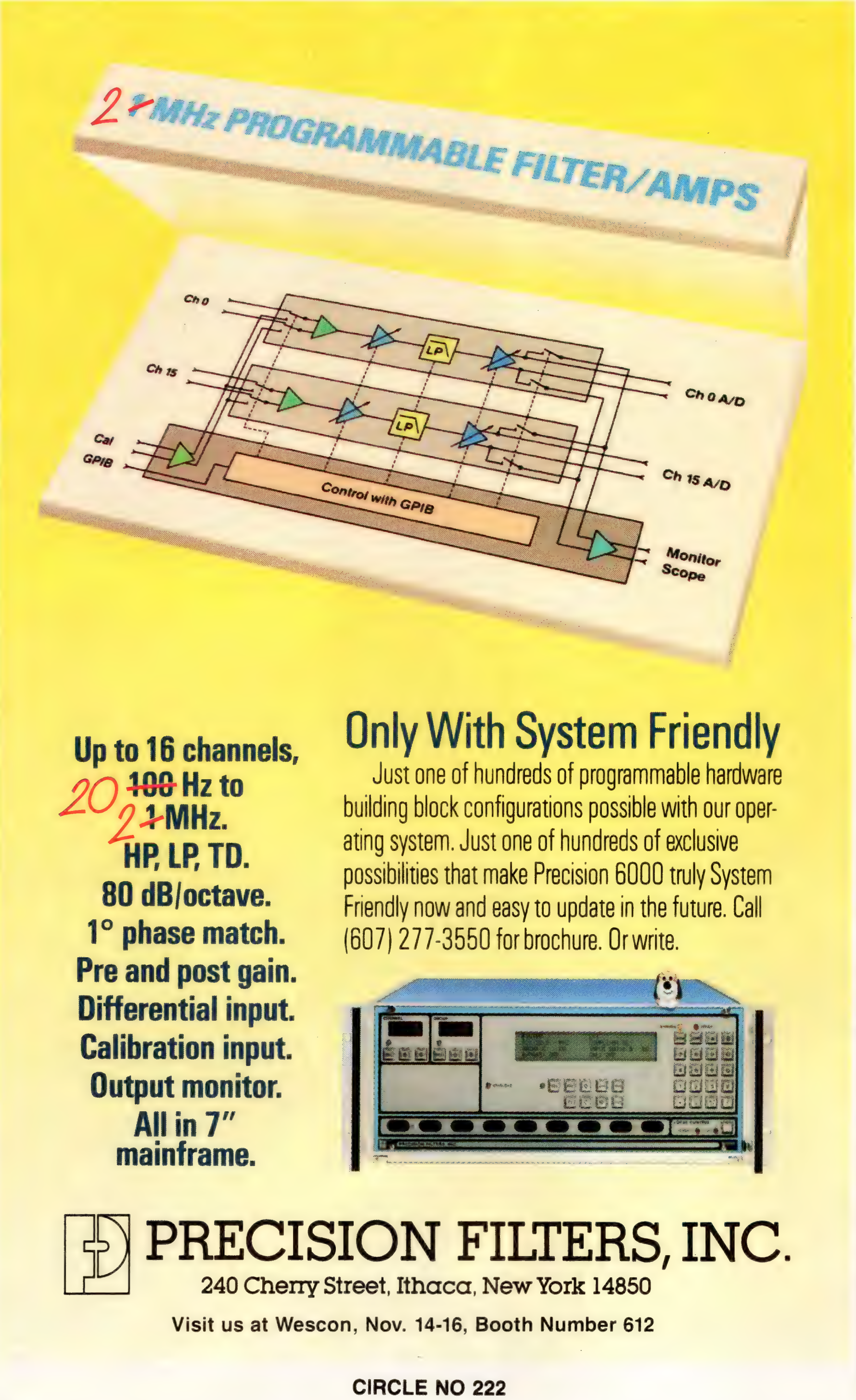
CIRCLE NO 221



probe access to one card plugged directly into the backplane—without an extender or the removal of any other cards. The unit's power supply provides 50W/card slot. The 5V bus is fused. Fans with self-adjusting variable speed furnish forced air for cooling while minimizing noise. A carrying handle makes the unit easy to move. The VXI-AT2000 interface kit lets you control the VXIbus from an IBM PC/AT-compatible computer. In addition to hardware for the PC/AT bus and the VXIbus, the kit includes the vendor's LabWindows instrument-control software. VXI-1000, $3600; VXI-AT2000, $3800.

National Instruments Inc, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488. FAX 512-250-9319. **Circle No. 356**



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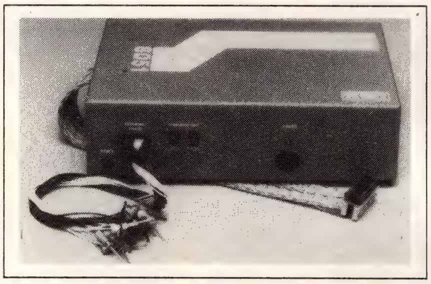

In-Circuit Emulator For DS5000 μC

- *Two trace buffers store time-tag data and external trace bits*
- *Allows 1M byte of emulation memory*

The HMI-200-8051 in-circuit emulator with support for Dallas Semiconductor's DS5000 μC allows development and debugging of programs for the unusual chip. The IC is available in versions that include 8k and 32k bytes of nonvolatile RAM. The emulator has two 4k-frame-deep, 88-bit-wide trace buffers that store 32 bits of time-tag data and 16 external trace bits. The emulator includes 128k bytes of bank-selectable emulation memory, which you can expand to 1M byte. The vendor's Sourcegate high-level-language debugger has a windowed interface and works with C, Pascal, and PL/M compilers from many vendors. Emulator, $5390; debugger, $1500 for MS-DOS. $3000 for Sun and Apollo workstations.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX 205-882-6701. **Circle No. 357**

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Two PC-Based Spectrum/ Network Analyzers

- *Cover 12.8 kHz and 102.4 kHz*
- *Use an IBM PC/AT-compatible computer and MS Windows*

The HP 3566A is an 8-channel spectrum/network analyzer; the HP 3567A is a 2-channel unit. Both are based on an IBM PC/AT-compatible computer that you must supply. The 3566A operates to 12.8 kHz; the 3567A operates to 102.4 kHz. The included software runs under Microsoft Windows and allows you to control the measurement process. The software also allows you to create your own control and analysis programs in a variety of languages supported by Microsoft. Measurement and computational capabilities include transient-time capture, harmonic-order tracking, auto- and cross-correlation, and ⅓-octave filtering with A weighting. The output data formats include multichannel power spectra, frequency-response curves, and waterfall displays. 3566A, from $22,000; 3567A, from $18,000. Delivery, eight weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 358

2-Channel, 10-MHz FFT Spectrum Analyzer

- *Includes IBM PC/XT-compatible computer*
- *Provides 128k bytes of waveform memory for each channel*

The R375 is a 2-channel, 10-MHz FFT spectrum analyzer that includes an IBM PC/XT-compatible computer with a 20M-byte hard disk, a 3½-in. floppy-disk drive, an IBM EGA display, a mouse, and 640k bytes of memory. The unit, which backs each channel with 128k bytes of waveform memory, has a hardware DSP "engine" that supports FFT averaging and windowing. Dynamic range exceeds 65 dB. You can select full-scale input sensitivities from 256 mV to 512V p-p under software control, and you can switch between 50Ω and 1-MΩ inputs. $6995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX 206-548-0322.

Circle No. 359

Test System For Smart-Power ICs

- *Supplies 2 kV and 100A*
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The A510-SP is a device test system for smart-power ICs. It provides engineers who are developing test programs with the same graphical interface as do other members of

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CIRCLE NO 224

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1. Names and complete addresses of the Publisher, Editor and Managing Editor are:
   Vice President and Publisher, Peter D. Coley, 275 Washington Street, Newton, MA 02158.
   Editor, Jonathan Titus, 275 Washington Street, Newton, MA 02158.
   Managing Editor, John S. Haystead, 275 Washington Street, Boston, MA 02158.
2. The owner is Cahners Publishing Co., a Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158.
3. The known bondholders, mortgages, and other security holders owning or holding 1 percent or more of total amount of bonds, mortgages, or other security are: None.

Extent and Nature of Circulation

	Average No. Copies Each Issue During Preceding 12 Months	Actual No. Copies of Single Issue Published Nearest to Filing Date
A. Total No. Copies (Net Press Run)	143,797	146,883
B. Paid and/or Requested Circulation		
1. Sales through dealers & carriers, street vendors and counter sales	None	None
2. Mail Subscriptions (Paid and/or Requested)	134,424	140,812
C. Total Paid and/or Requested Circulation	134,424	140,812
D. Free distribution by mail, carrier, or other means samples, complimentary, and other free copies	7,520	4,461
E. Total Distribution (Sum of C & D)	141,944	145,273
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1. Office use, left over, unaccounted, spoiled after printing	1,853	1,610
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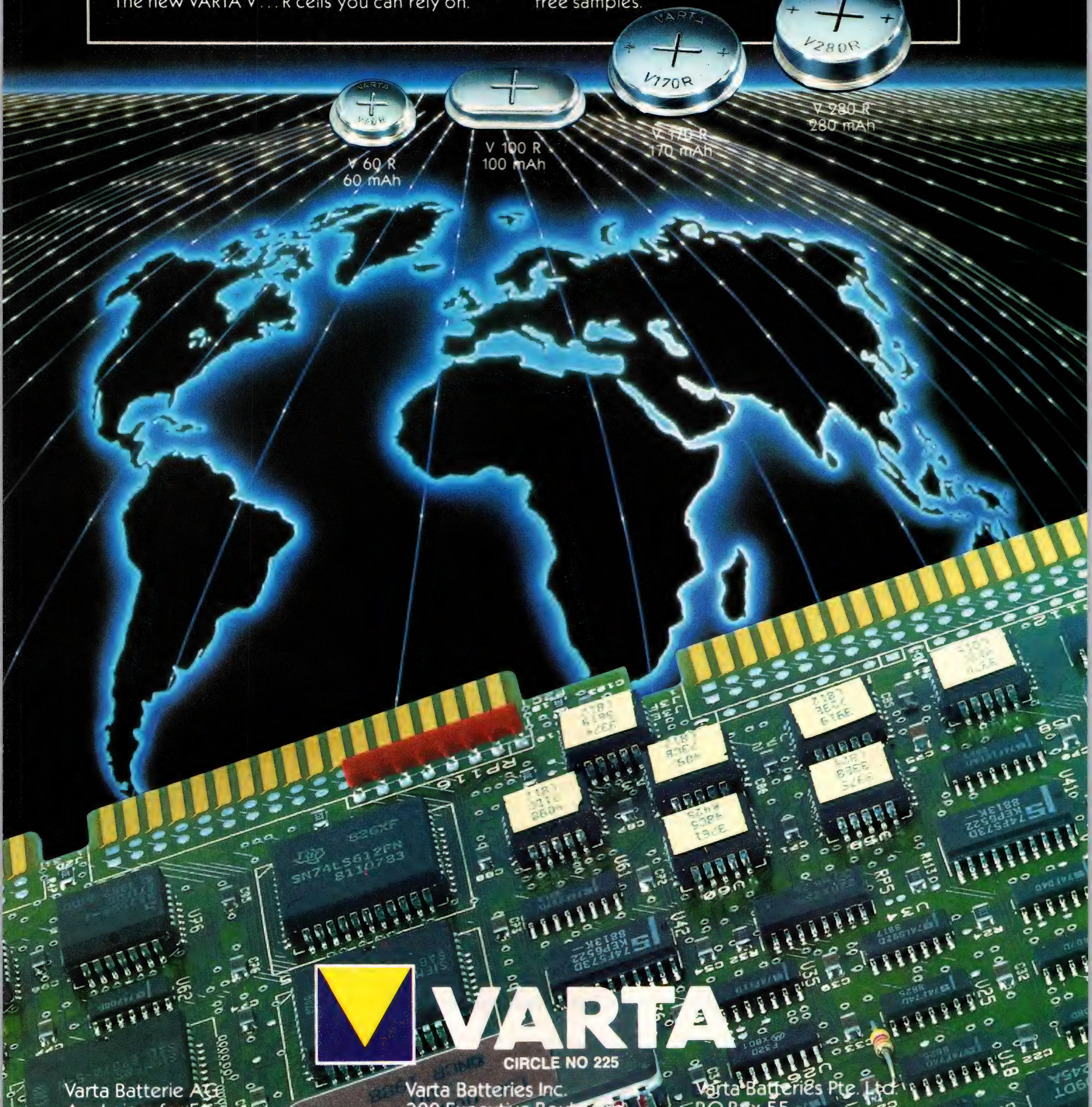

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CIRCLE NO 226

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- *Covers 1 to 100 MHz*
- *Has sensitivity of 100 μV ±3 dB at 50 MHz*

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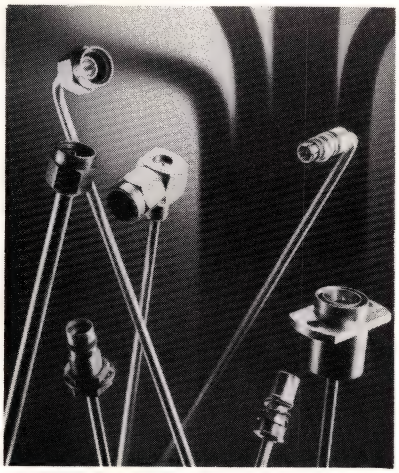
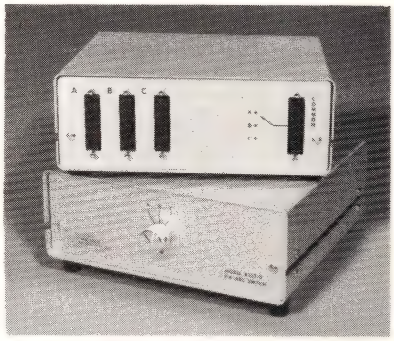


Coaxial Connectors

- *Terminate 50Ω cables*
- *Accommodate frequencies as high as 26 GHz*

These SMA and 3.5-mm blindmate coaxial connectors terminate RG-405/U and RG-402/U semirigid cable with a 50Ω nominal impedance. The SMA devices are available as completely preassembled plugs and jacks in performance ranges of 0 to 18 and 0 to 26 GHz, qualified to MIL-C-39012. Using a bench-mounted, semiautomatic pneumatic tool, you can terminate the units in less than 60 sec. The 3.5-mm blindmate connectors offer a frequency range of 0 to 26 GHz, solid telescoping alignment, and a shielded outer contact. Bulkhead plugs and jacks and a 2-hole panel plug are available. Right angle versions are optional. You can crimp terminate the 3.5-mm units using a standard military hand tool. SMA connectors, $3.15; 3.5-mm blindmate connectors, $10 (1000). Delivery is 12 and 14 weeks ARO, respectively.

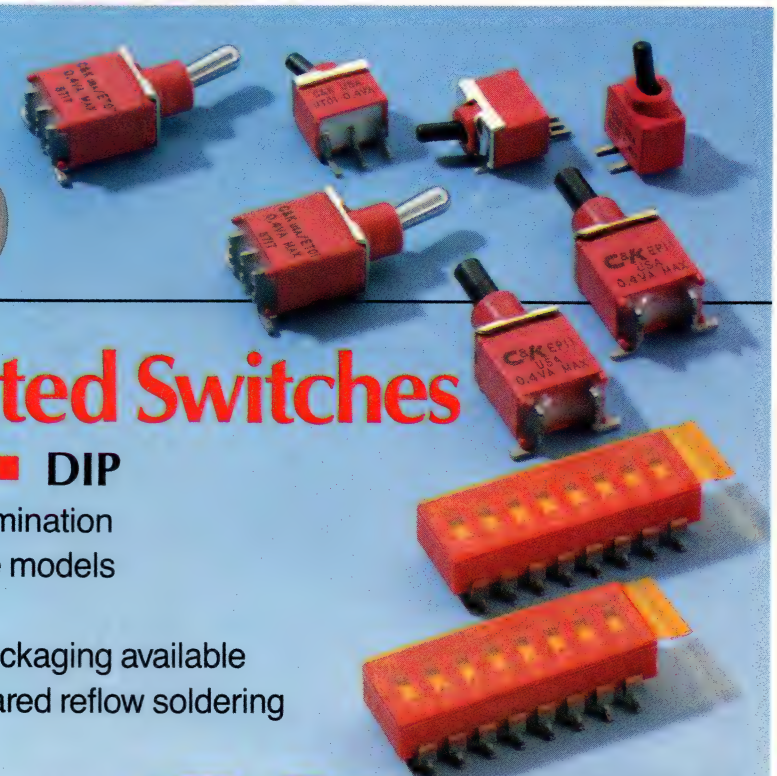
AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (717) 564-0100. FAX 717-561-6179. **Circle No. 389**



Port-Sharing Switches

- *Designed to improve computer-room efficiency*
- *Have speed and code transparency*

Models 8351-D and 8352-D port-sharing switches are designed to improve computer-room efficiency. They allow three terminals to share one computer I/O port, three CPUs to share one printer, or three terminals to share one modem. The 8351-



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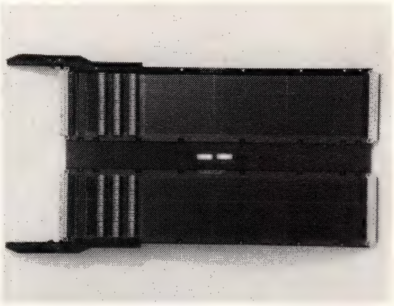
CIRCLE NO 234

D switches 12 of the most required EIA RS-232 interface signals; the 8352-D switches all signals at the RS-232 interface. All connections are made via four female, 25-pin connectors (A, B, C, common) on the rear panel of the desktop unit. A flick of the front-panel switch routes signals from the common connection to the appropriate signal connector. The switches are speed and code transparent and require no power. Model 8351-D, $151; Model 8352-D, $175.

Electro Standards Laboratory Inc, Box 9144, Providence, RI 02940. Phone (401) 943-1164.

Circle No. 390



Extender Card

- *Features readily accessible signal lines*
- *Gold plating minimizes test-point resistance*

The Model 031-076-01 J1/J2 extender card is fully compatible with all VME-standard hardware. Each signal line from the backplane is connected to a square post in front of an on/off switch. The test-board side of the card is similarly accessible. All the test points are gold plated to minimize connection resistance, and the ones at the card's top end are marked with standard VME signal codes. Signal paths employ a transmission-line geometry that virtually eliminates signal distortion and adjacent-line crosstalk. Plastic guides, which hold the card firmly in place, have a side-action inserter/extractor mechanism that positively seats and extracts the card under test. $479.

Hybricon Corp, 12 Willow Rd, Ayer, MA 01432. Phone (508) 772-5422. FAX 508-772-2963.

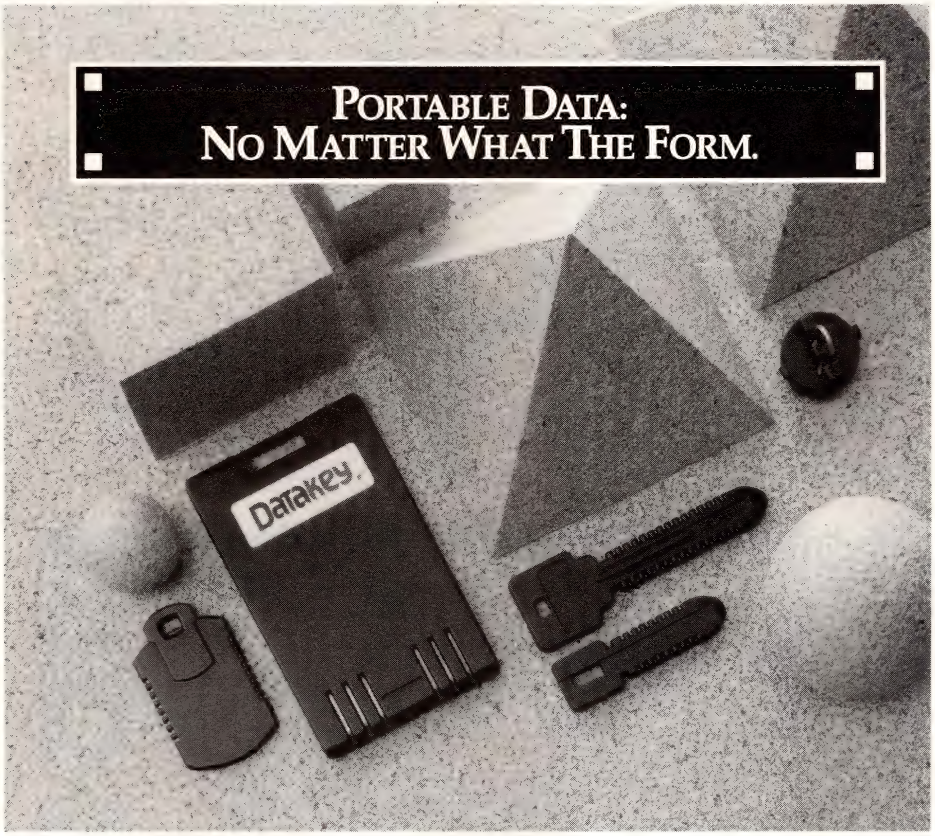
Circle No. 391

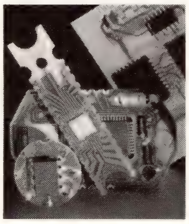
Solid-State Timers

- *Function as a time delay or a relay*
- *Offer either ac or dc outputs*

These potentiometer-adjustable solid-state timers can function either as time-delay output modules or as stand-alone, pc-board-mountable relays. Available with either a delay-on-operate or an interval-on-timing function, the units are available with ac output (OAT Series) or dc

Text continued on pg 318





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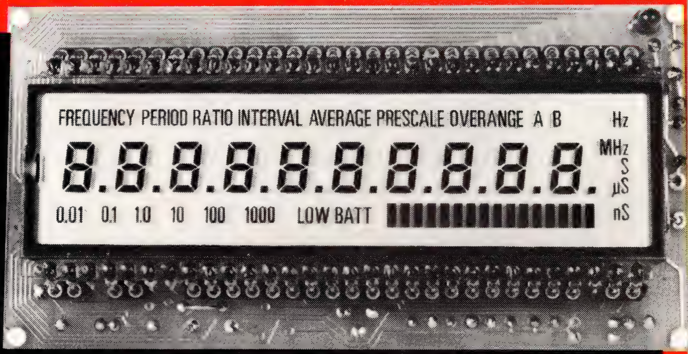
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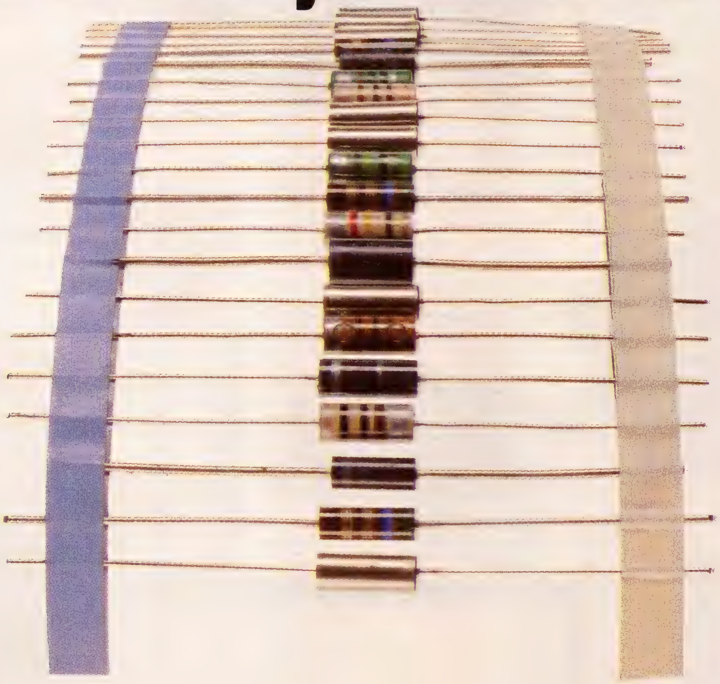

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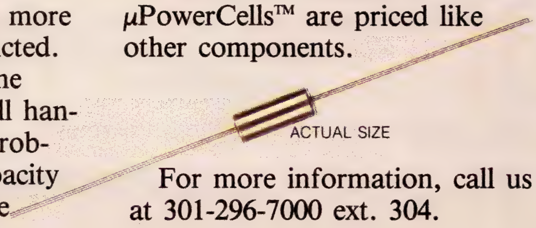

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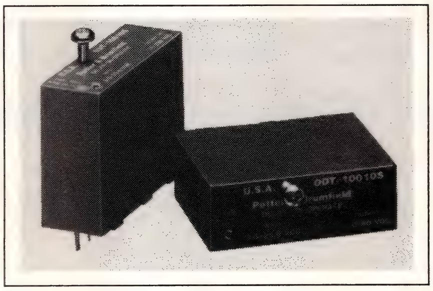

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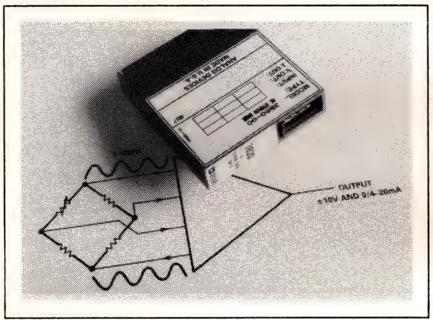

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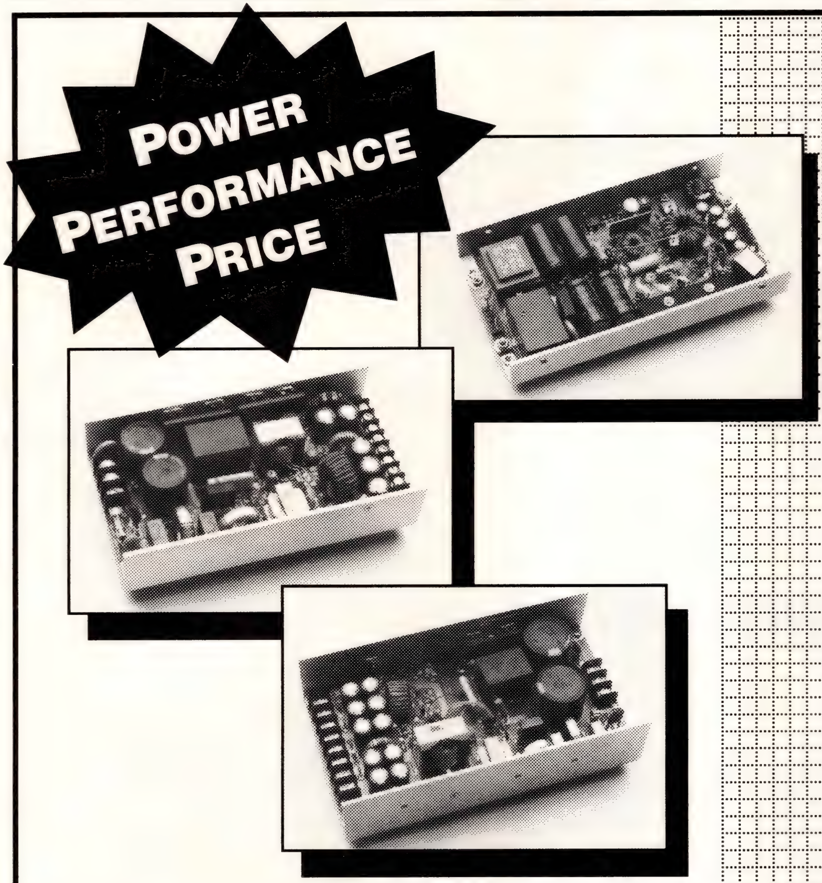

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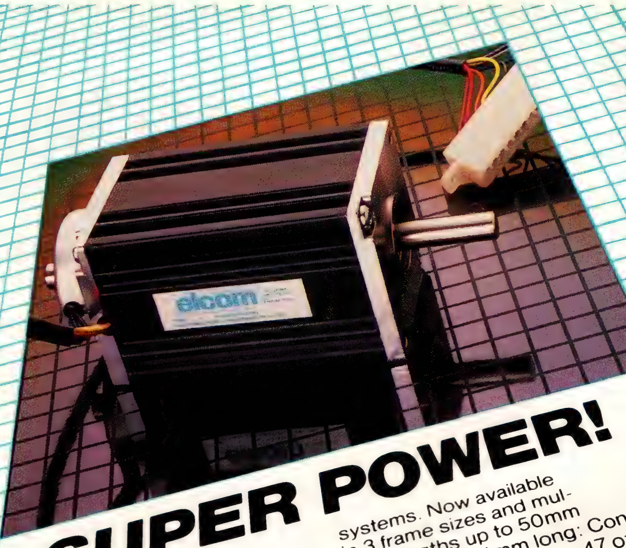

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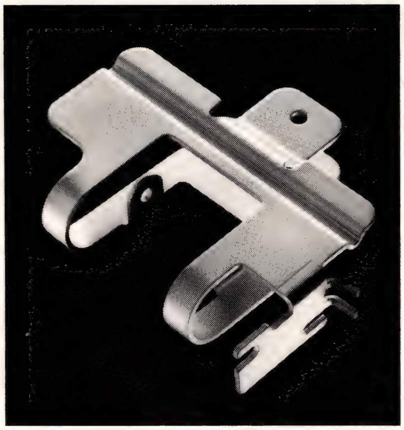

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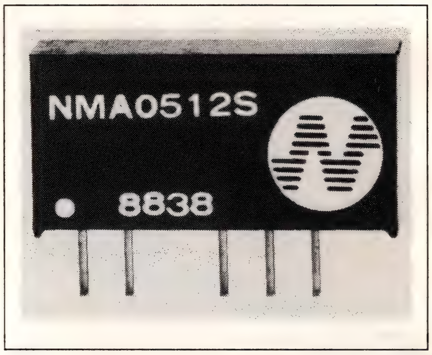

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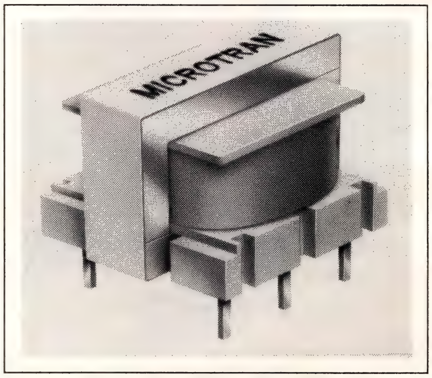
International Power Sources Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7434. FAX 508-879-8669. **Circle No. 394**



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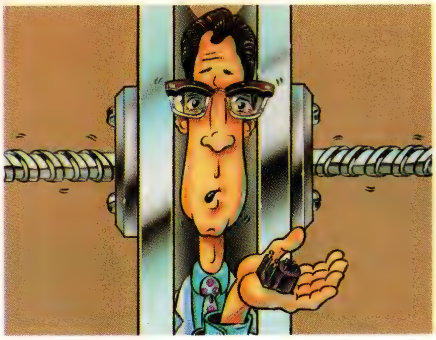

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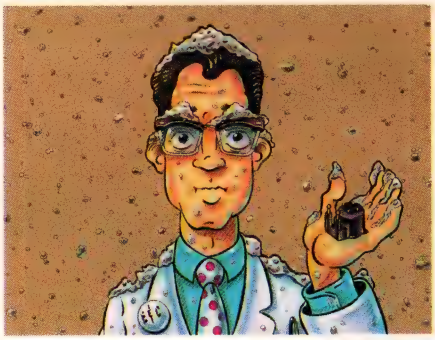

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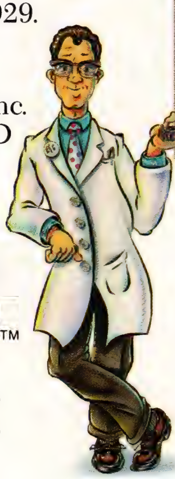

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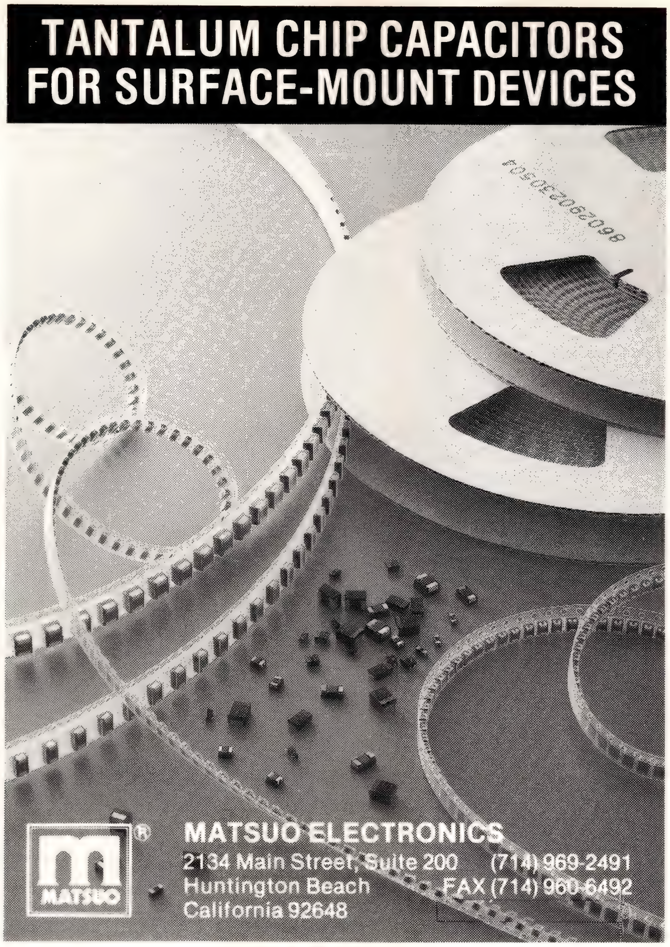

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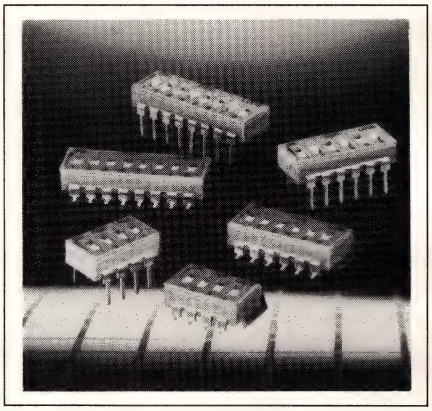

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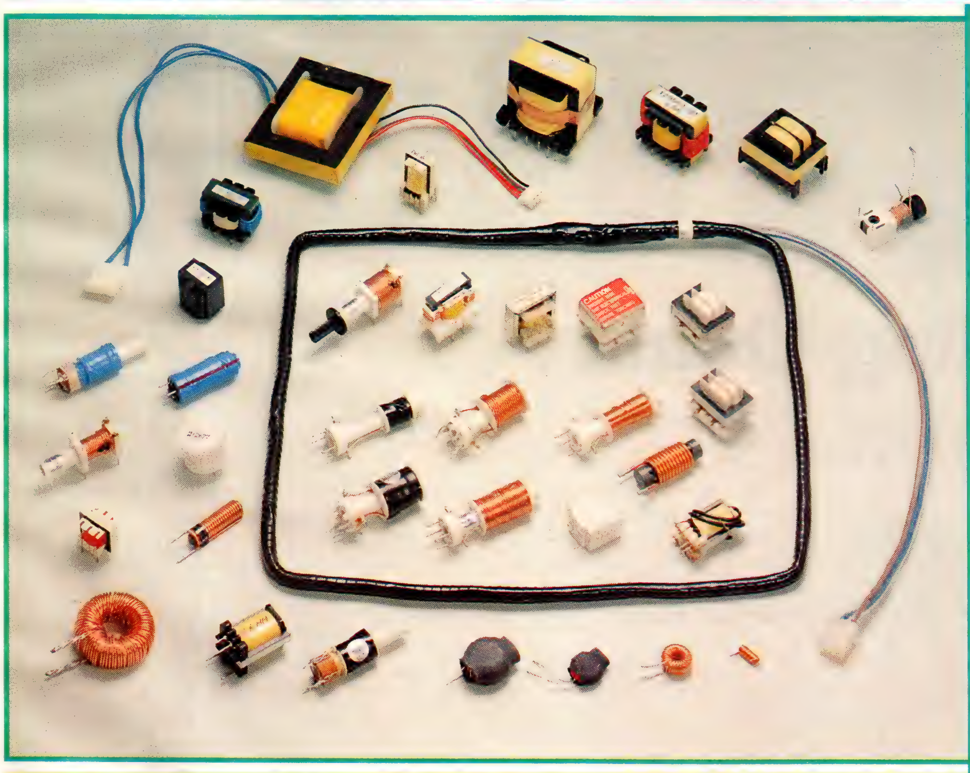

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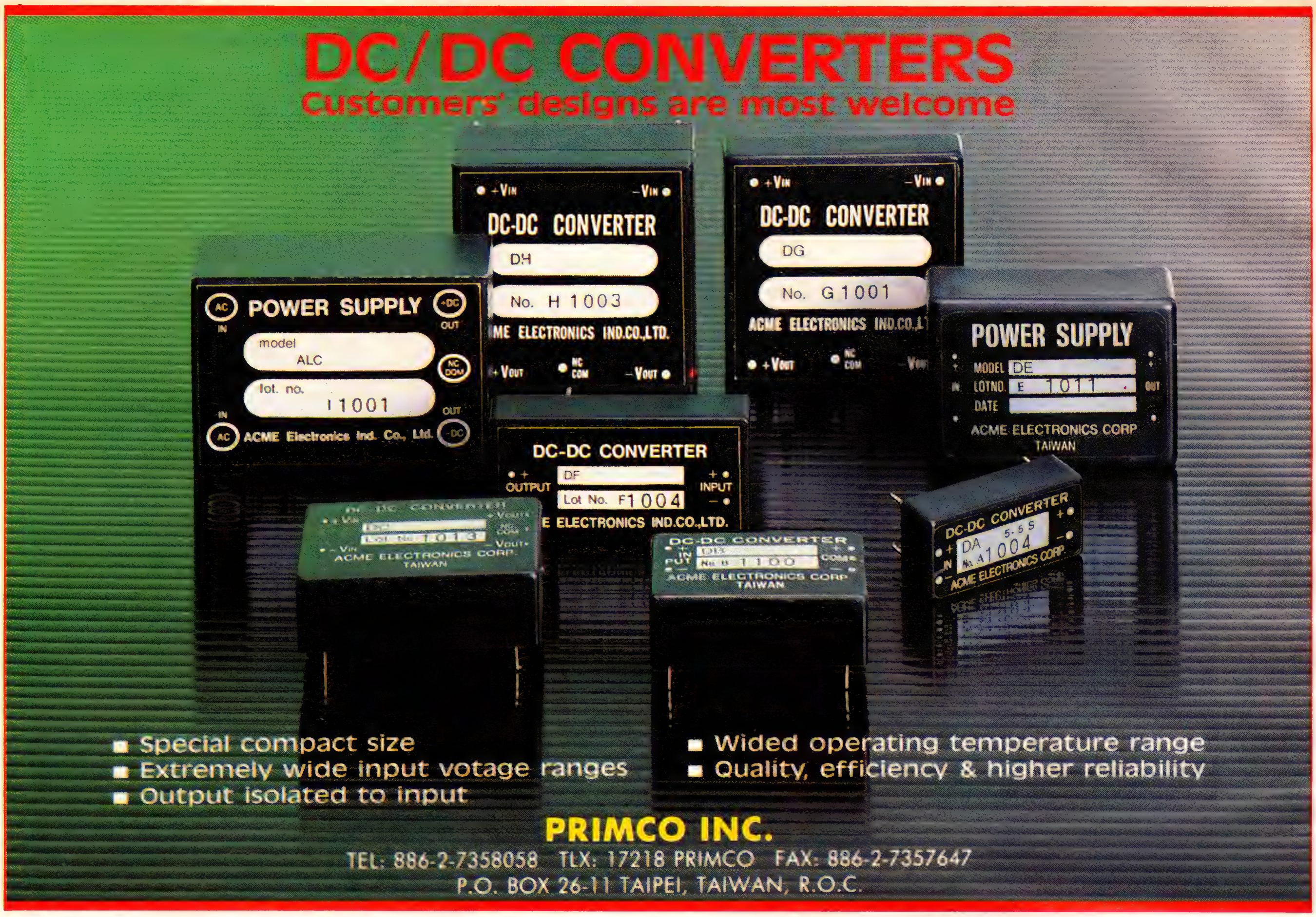

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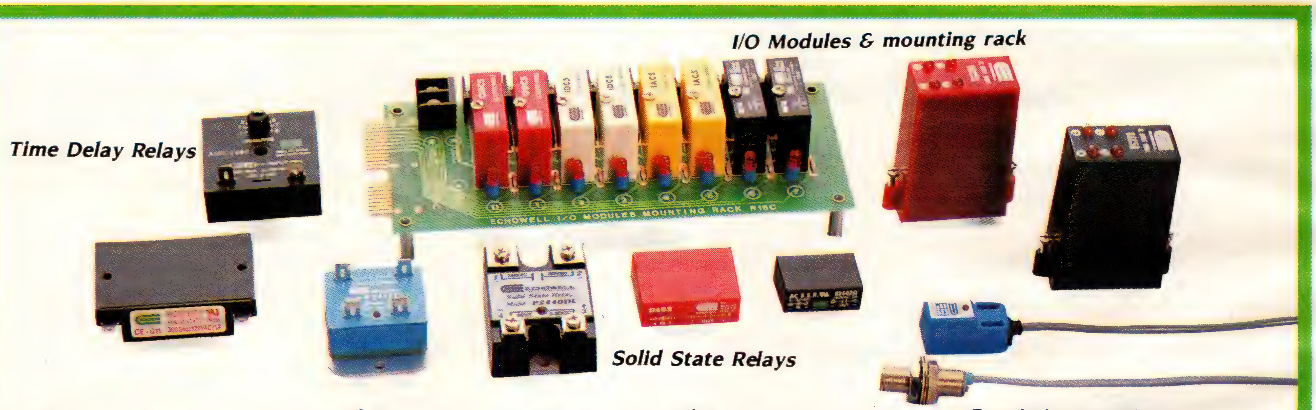
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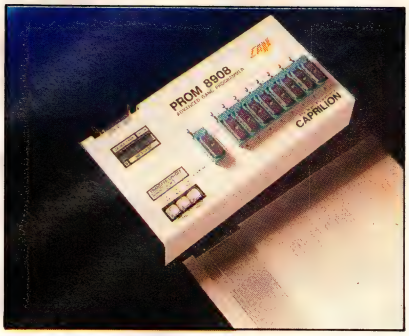

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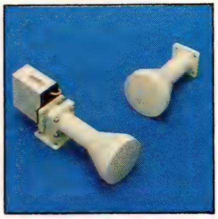

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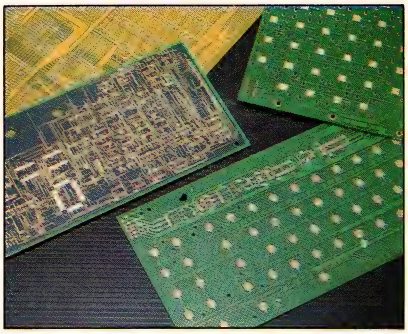

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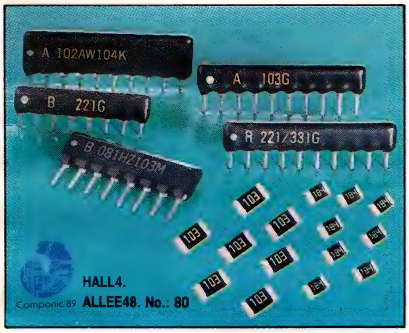

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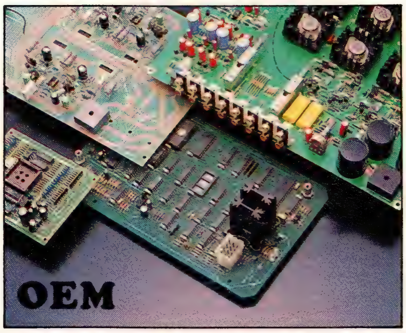

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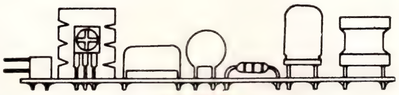

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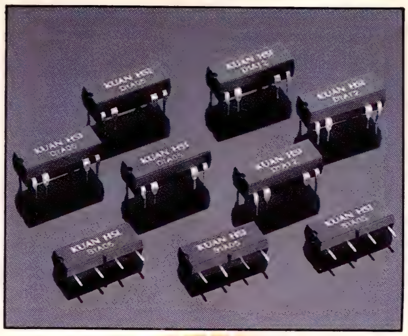

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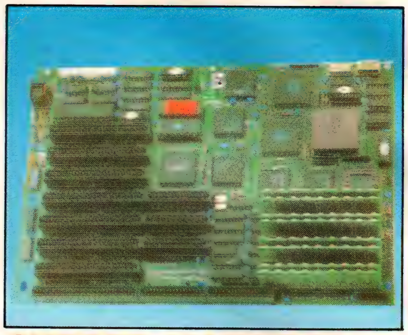

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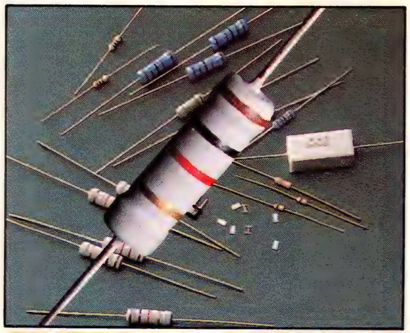

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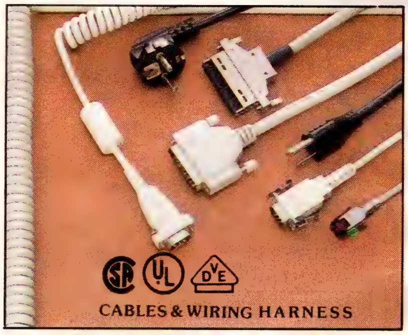

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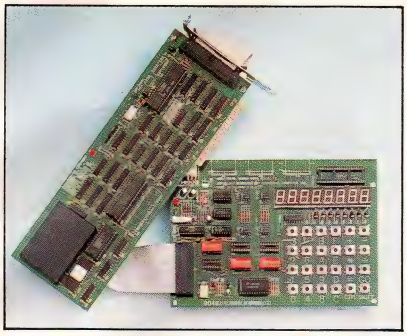

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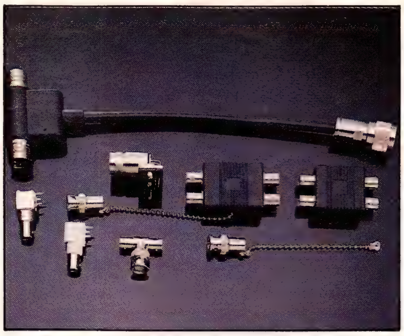

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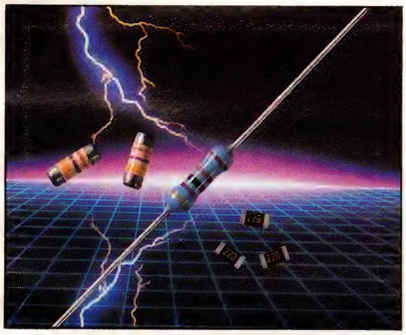

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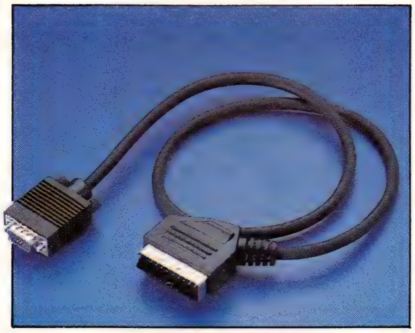

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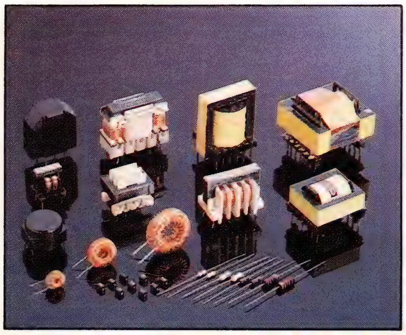

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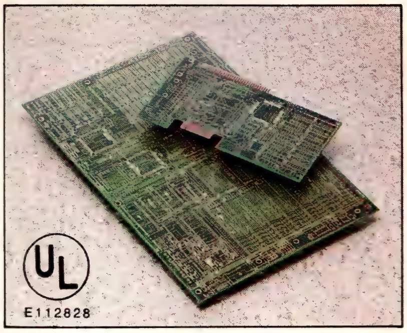

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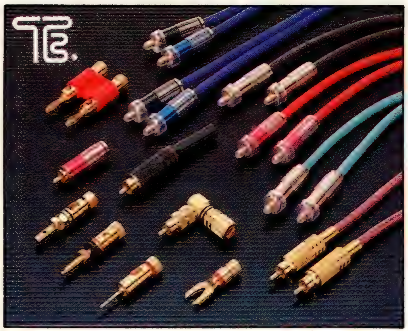

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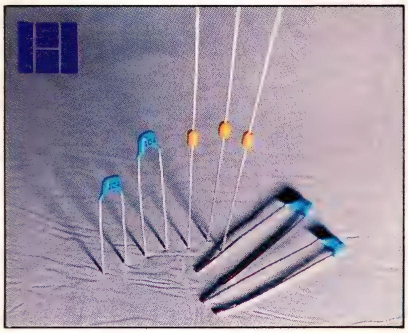

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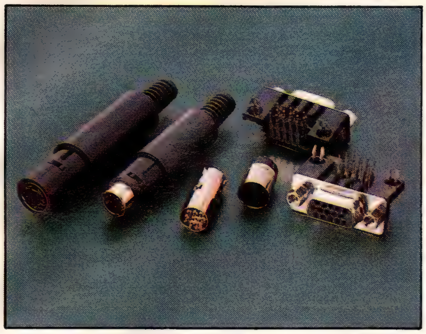

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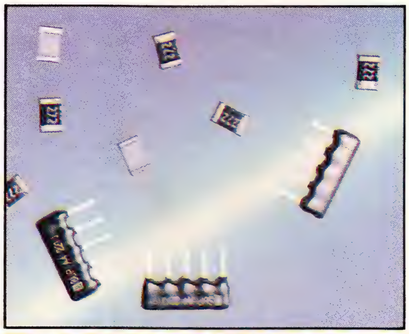

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CIRCLE NO 286

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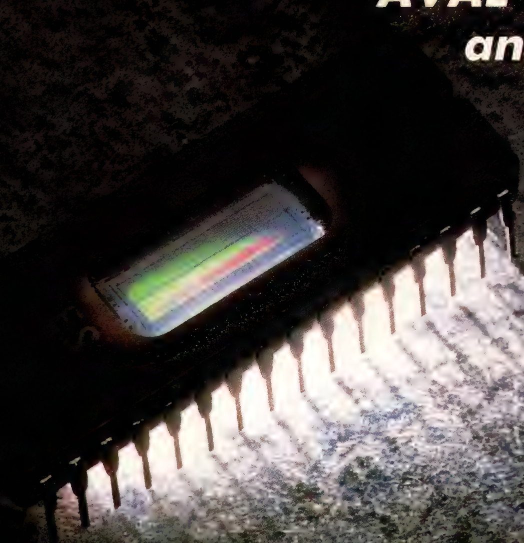

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AVAL·PLUS

THE SYSTEM PROGRAMMER

The AVAL-PLUS incorporates state of the art technology to support the broadest range of programming requirements. Programmable pin drivers, customised firmware and 16-Bit processing combine to eliminate overhead and ensure support for the fastest programming algorithms. With a choice of generic adapters, you can add device support as you need it. Options are available to program MOS Memories (EPROMs, EEPROMs, Microcontrollers and CMOS PROMs), Bipolar fusible PROMs and PLDs (PAL, EPAL, IFL, PLA, GAL etc.). As production and development tools, the powerful Multi-Set gang adapter and flexible ROM emulator options further enhance the profile of the AVAL-PLUS.

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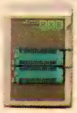

CMOS PROM
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RX 3

EPLD
ADAPTER
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ADAPTER
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PROGRAMMER

MOS
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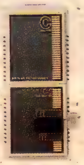
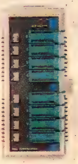
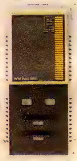


GANG SET
PROGRAMMER



MEGABIT ROM
EMULATOR



PCMODE SOFTWARE

PCMODE

PC-MODE software provides a user-friendly interface to your personal computer. A menu driven command structure and on-screen status simplify the task of programmer setup and file management. For design changes, the PC-MODE screen editor gives you direct access to your program code. It will also convert and output program files to your PC printer port in "AVAL Binary Format". In this format, Megabit data files can be transferred in under 25sec.

LOG/iC SYNTHESIS

LOG/iC, the multipurpose design tool for universal logic synthesis, is available on most mini-and microcomputer systems. It lets you describe your design with an arbitrary mix of Equations, Truth Tables and State Machine Syntax. When you want to use graphic designs, LOG/iC's "Schematic Macro Library" supports input of netlists from third party schematic editors-such as OrCad. A Block orientated design syntax lets you define independent Macros and link them with these graphic blocks. LOG/iC's Functional Verifier then lets you simulate your design interactively on screen. The same input syntax can be optimised for different physical implementations.

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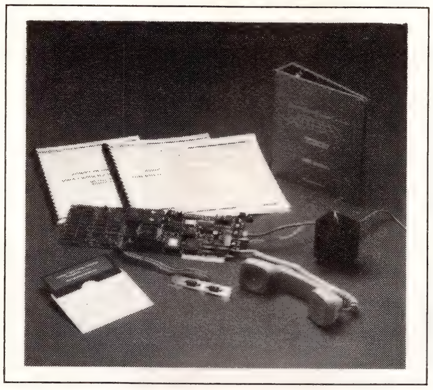
CIRCLE NO 289

ISDN Boards

- *Let users develop layer 2 and layer 3 software*
- *Allow PC/XT boards to interface with 5ESS Central Office Switch*



The MC145490EVK and the MC145491EVK are Integrated Services Digital Network (ISDN) development boards for the IBM PC/XT and compatible computers. The boards contain the company's ISDN ICs and layer 2 (Q.921) and layer 3 (Q.931) software. They come with a headset and connection cables. Users can develop application-specific ISDN software based on its resident layer 2 and layer 3 software. The boards can interface with Northern Telecom's DMS100 or AT&T's 5ESS Central Office Switch. Demonstration software, application notes, and IC data sheets are included. The boards differ in their codec compatibility; the MC145490EVK uses a Mu-law codec, and the MC145491EVK uses an A-law codec. Both boards operate in either Network Termination or Terminal Equipment mode. Each board contains 512k bytes of RAM (expandable to 1M byte), 2k bytes of dual-port RAM, 128k bytes of EPROM, and two audio interfaces. Demonstration software allows call setup for either voice or data over the B channels. $2500.

Motorola Inc, Technical Info Center, Box 52073, Phoenix, AZ 85072. Phone (512) 928-6880.

Circle No. 382

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- *For IBM PCs that use SC32 µP*
- *Operates with optimized Forth language*

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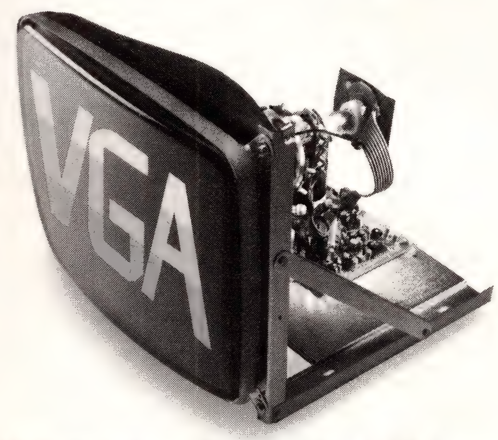

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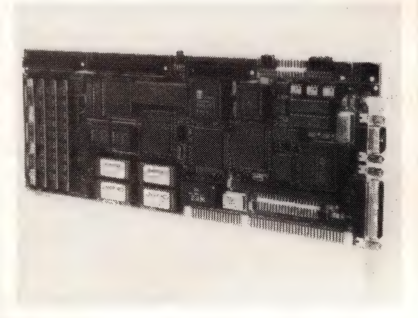
a burst mode. Communication between the board and the host takes place through 16k bytes of shared memory, which can be positioned anywhere in the PC's memory locations. The host PC provides power, screen, keyboard, and disk services for the PCS32. Therefore, when the PCS32 doesn't require host service, it can operate in the background to free the host for other tasks. The board operates with SC/Forth32, an interactive Forth language. Based on the Forth-83 standard, the SC/Forth32 optimizes multiple Forth words into single instructions for the µP that executes in 1 clock cycle. The software can handle both Forth block and ASCII text files, allowing you to develop programs on its onboard block editor or an MS-DOS editor. $1995.

Silicon Composers, 208 California Ave, Palo Alto, CA 94306. Phone (415) 322-8763.

Circle No. 383



ISA 1-Board Computer

- *Uses an 80C286 µP for passive backplanes*
- *Has as much as 4M bytes of RAM*

The Slot Board/286 single-board computer for IBM PC/AT-compatible passive backplanes integrates either a 12- or a 16-MHz 80C286 µP with as much as 4M bytes of RAM. The device features a SCSI port and a floppy-disk- and a hard-disk-drive controller. You can configure its primary serial port as either a 2- or a 4-wire RS-422 port with RTS/CTS (request to send/clear to send) handshaking, an RS-232C port, or a bidirectional RS-485 port with multidrop capability. Onboard byte-wide memory sockets let you install either 32k bytes of EPROM or nonvolatile RAM. You can plug any of the company's Mini-Modules into the board to provide video controllers, LCD flat-panel display controllers, and a 2400-baud modem. The board measures 4.75×13.33×0.75 in. and consumes 8W. From $737 (100).

Ampro Computers Inc, 1130 Mountain View/Alviso Rd, Sunnyvale, CA 94089. Phone (408) 734-2800. FAX 408-734-2939. TLX 4940302.

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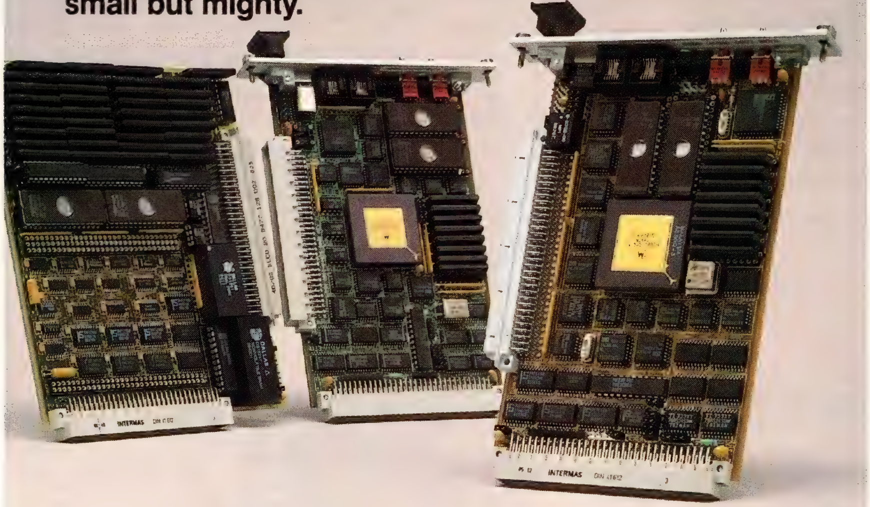

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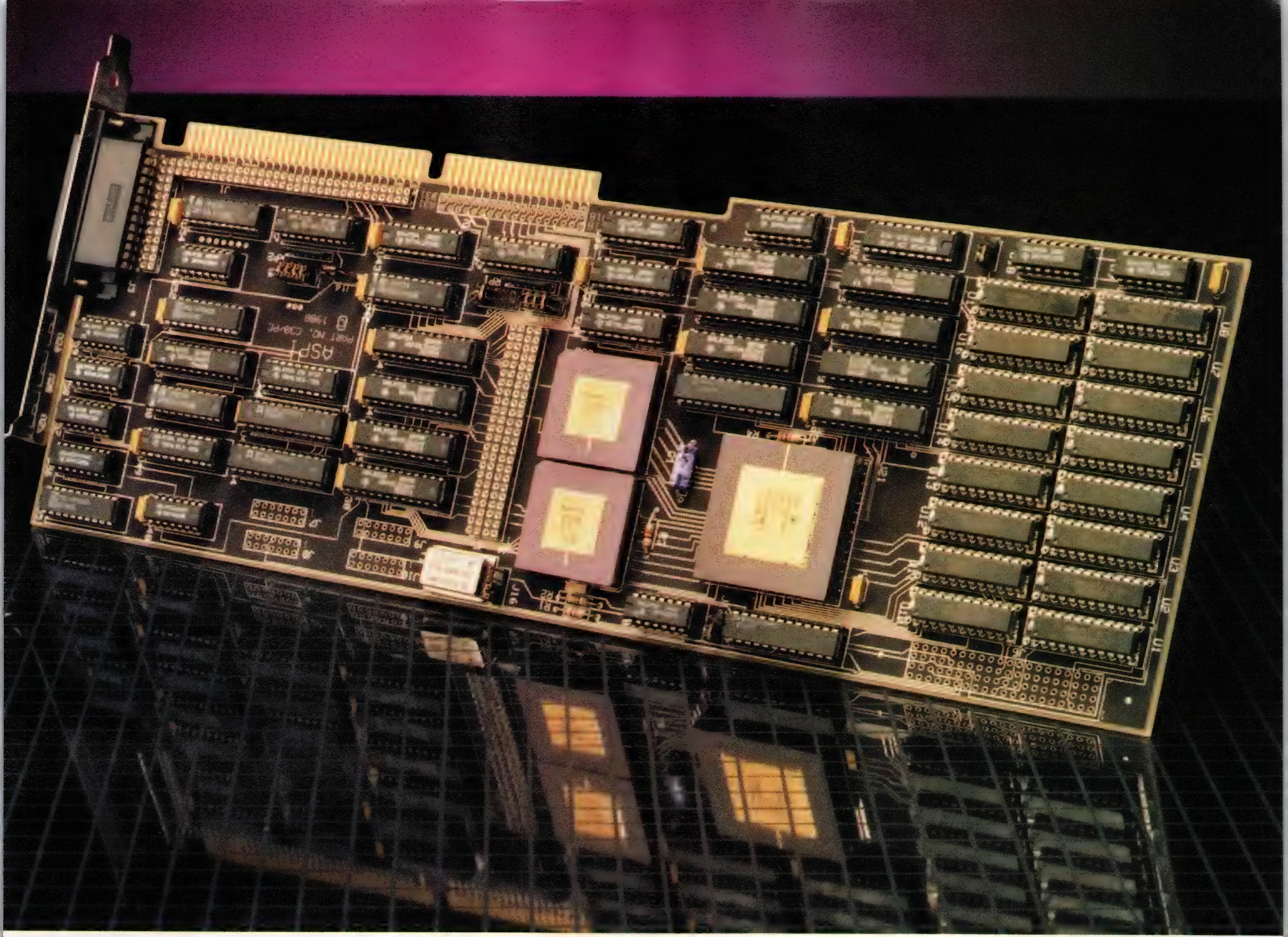

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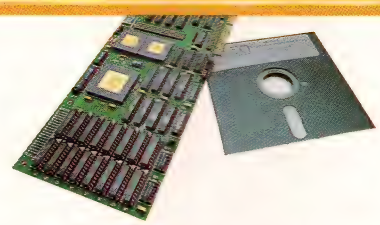
Other options include a wirewrap board for your custom hardware applications; a 16-bit, dual-channel, 200 kHz A/D-D/A daughter board; a multiprocessor board and a host of other daughter boards under development.

Banshee also provides a sophisticated, user-friendly software environment. The basic system includes SPOX™ (a C30 operating system), a program for loading and linking C30 code on the AT host, a full-featured C30 program debugger, and a proprietary shell program to make it all easy.

For detailed specifications and prices, contact Atlanta Signal Processors, Inc., 770 Spring St., Atlanta, GA 30308. Telephone 404/892-7265.

Banshee™



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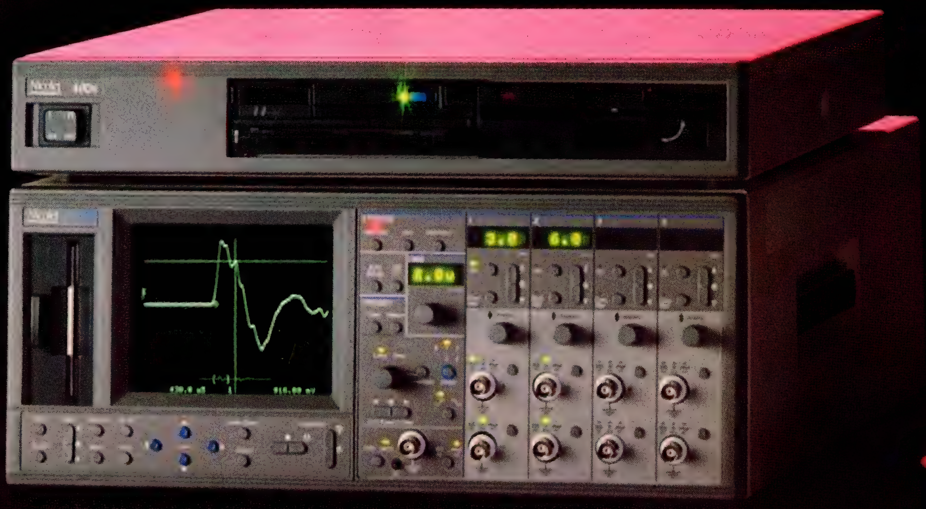
THE SHAPE OF THE FUTURE



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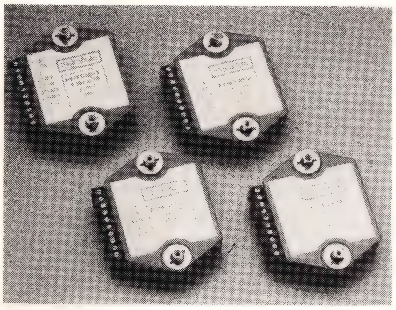
INSTRUMENTS OF DISCOVERY

CIRCLE NO 248



Analog Modules

- *Communicate with a computer via an RS-232C/485 interface*
- *Users can program units to set high- and low-output levels*

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Metrabyte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX 508-880-0179. **Circle No. 385**

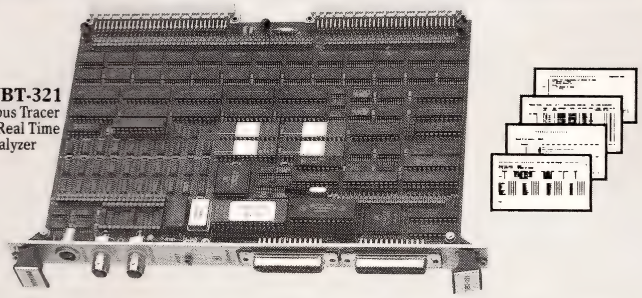
386 Computer

- *Operates at 33 MHz and has 32-bit cache controller*
- *Features a 128k-byte cache RAM and operates at 7.5 MIPS*

The Power 386-33 computer employs a 33-MHz 80386 μP and has an intelligent 32-bit cache controller that uses an Intel AT/32-bit bus and a SCSI peripheral bus. The controller uses an 80376 μP that provides DMA control and control over as much as 4M bytes of cache RAM. The unit comes with 128k bytes of cache RAM and delivers 7.5 MIPS. The company's benchmarks indicate that the computer has a data-transfer rate of 104M bytes/sec. The computer loads system and video BIOS from ROM into shadow RAM, which provides faster BIOS execution. The standard configuration supports DOS, OS/2, and Xenix operating systems, as well as Novell and interactive-Unix version 3.2 network software. Options include

VMEbugs

Are VMEbugs Eating Up Your Projects?



VMETRO VBT-321
Advanced VMEbus Tracer
Logic State and Real Time
Performance Analyzer

Don't let VMEbugs eat up your project time and budget. VMETRO offers a third generation single board Advanced VMEbus Tracer that enables you to control costs and meet your deadlines. By providing instantaneous debugging and performance analysis after mere seconds of installation, the VBT-321 will pay for itself time and again. Operated from a remote or on-site ASCII terminal, the VMETRO advanced VMEbus Tracer VBT-321 is the ultimate tool for VMEbus development, integration and system tuning. The Advanced VBT-321 is flexible and easy to use with the following new capabilities:

Triggering: Logic state analysis with complex user-defined trigger sequences of up to four events give the user complete control over the data to be analyzed. **Filtering:** Store Qualifiers on any combination of all signals and events enable buffering of useful information only. **Performance Analysis:** VMEbus Utilization, Bus Level Distribution and Event count histograms are based on a 100% capture ratio of the data stream and not just a snapshot common in less capable and more expensive instruments.

FEATURES:

NEW
- Four Trigger/Qualifier/Performance Analysis events, each covering 94 VMEbus signals.
- Four Sequence levels, or events can be And'ed/Or'ed.
- Occurence Counter for delayed triggering/filtering.
- Performance analysis and Bus Utilisation based on a 100% capture ratio.
- Histograms for Bus Transfer Rate & Interrupt Level Activity.
- Hardware handshake on RS232 for Modem Control enable long distance Service and Diagnostics over the phone.
- Up to 30 complex setups may be stored in Battery Backup.
- Power supply from VMEbus backplane or via External Power Supply for debugging in Power On/Off sequence.
- External Signal Input and Trigger Output on BNC connectors provides an interactive interfacing.
- Special clocking of Bus Levels, Read-Modify-Write and Block Transfers.
- Filtering/Triggering on combinations of Hex and Binary values of any Address and Data byte.
- 25MHz Asynchronous Sampling for accurate time tagging.
- Piggyback provisions for future VSB/VMEbus enhancements.

GENERAL
- 96 channels of data buffered in 2K Trace.
- Time Tags for Relative Time between samples and Absolute Time from trigger.
- Histograms for Address Range Distribution for software and system tuning.
- 16MHz synchronous sampling captures all traffic in even the fastest VMEbus systems.
- Search or select any data presented in 2K Trace Buffer.
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CIRCLE NO 249

a 5G-byte hard-disk drive, an IBM VGA with 1024×768-pixel resolution, as many as 96 serial ports, one 2.2G-byte tape-storage unit, and a 32-bit Ethernet card. $9995.

Micro 1 Inc, 557 Howard St, San Francisco, CA 94105. Phone (800) 338-4061; in CA, (415) 974-5439.

Circle No. 386

Node Controller

- *Provides a 100M-bps FDDI port for VMEbus*
- *Custom DMA chip moves data in its 256k-byte memory buffer*

The V/FDDI 3211 6U node-controller board for the VMEbus provides a Fiber Distributed Data Interface (FDDI) for a 100M-bps fiber-optic network. Its custom DMA chip transfers data to and from its 256k-byte memory buffer. The controller can transfer data over the VMEbus at 100M bytes/sec. Arranged in a 64k-byte memory of 32-bit words, the dual-port buffer has an access time of 70 nsec. The board functions as a single FDDI attachment. Two boards can operate as a dual-attachment station that provides a degree of fault tolerance in an FDDI network. The board conforms to ANSI and the US Navy's Safenet II specifications. $8000.

Interphase Corp, 2925 Merrell Rd, Dallas, TX 75229. Phone (214) 350-9000. TWX 910-997-6245.

Circle No. 387

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CIRCLE NO 250

VME CPU Board

- *Uses a 68020 μP and operates as a bus master*
- *Has 16M bytes of RAM dual ported to VME and local buses*

The 68-26 CPU board for VMEbus systems employs a 68020 μP operating at 16 or 25 MHz. The board can operate as a bus master and provides 16M bytes of RAM that's dual ported to the VMEbus and a local bus. The board can handle block transfers and either byte, word, triple word, or long-word transfers on aligned or nonaligned boundaries. You can configure the parity-checking logic to generate either a local or a VMEbus error signal when a parity-memory error occurs. The 32-bit advanced processor extension bus (APEX) lets the user select from an array of company modules including Ethernet, SCSI, floppy-controller, IEEE-488-controller, and parallel I/O modules. An address-mapping RAM allows the board to operate with any mix of slaves with different address- and data-width requirements. $2190.

Radstone Technology, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; in NJ, (201) 391-2700.

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ZPS-150	150	4.75/5.25	2.0/20.0	10.0-15.0	0.3/3.0 PK 4.5	10.0-15.0	0.3/3.0 PK 4.5	4.75/5.25	0.2/2.0
ZPS-175	175	4.75/5.25	2.5/25.0	10.0-15.0	0.3/3.5 PK 5.3	10.0-15.0	0.3/3.5 PK 5.3	4.75/5.25	0.2/2.0
ZPS-200	200	4.75/5.25	3.0/30.0	10.0-15.0	0.4/4.0 PK 6.0	10.0-15.0	0.4/4.0 PK 6.0	4.75/5.25	0.2/2.0
ZPS-250A	250	4.75/5.25	3.5/35.0	11.5-26.0	0.4/4.0 PK 6.0	4.75-16.0	0.4/4.0 PK 6.0	4.75-16.0	0.3/3.0 PK 4.5
ZPS-300A	300	4.75/5.25	4.5/45.0	11.5-26.0	0.6/6.0 PK 9.0	4.75-16.0	0.8/8.0 PK 12	4.75-16.0	0.4/4.0 PK 6.0
ZPS-400A	400	4.75/5.25	5.5/55.0	11.5-26.0	0.7/7.0 PK 10.5	4.75-16.0	1.0/10.0 PK 15.0	4.75-16.0	0.6/6.0 PK 9.0

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5	12	12	12
5	15	15	5
5	24	12	5
5	24	12	12
5	24	15	15

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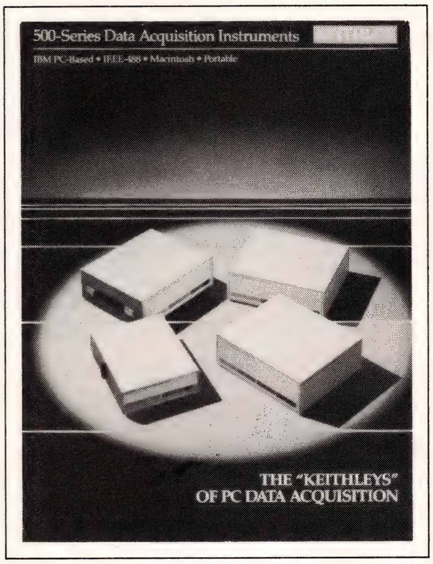
CIRCLE NO 251

LITERATURE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Pamphlet surveys data-acquisition mainframes

An 8-pg brochure describes four data-acquisition mainframes, 25 function modules that provide 16-bit, 50-kHz A/D measurement capabilities, and modules for digital input/output, stepper-motor control, pulse/even counting, linear-variable-differential transformers, and power control. The software selector guide sums up five different data-acquisition software packages and describes device-driver and desk-accessory packages that are compatible with the company's equipment.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. **Circle No. 411**

Publication profiles GaAs digital ICs

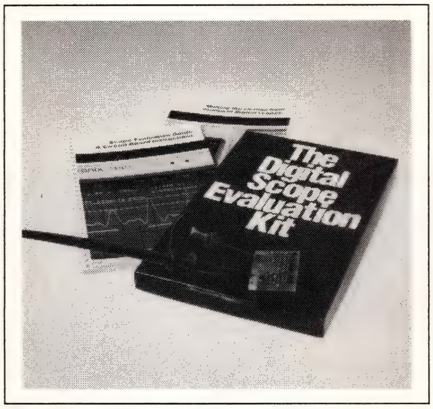
The vendor's *1989 Product Data Book* is devoted to its complete line of high-performance GaAs digital ICs. The book covers specifications for all of the standard products, including fast static RAMs, bit-slice μPs, and telecommunications ICs; ASICs, including gate arrays and standard cells; and full custom capabilities. In addition to complete product coverage, the 200-pg book provides application notes about pc boards, interfacing GaAs ICs with ECL and TTL systems, the synchronous optical network (SONET) standard, and GaAs ASIC design.

Vitesse Semiconductor Corp, 741 Calle Plano, Camarillo, CA 93010. **Circle No. 412**

Guide to MIL-STD and semicustom ICs

This 28-pg directory describes the company's military-standard and semicustom ICs and its radiation-hardened capabilities for the high-reliability and aerospace markets. In addition to MIL-STD-1553 and MIL-STD-1750 products, the book contains monolithic bus-transceiver products and DSP products. Block diagrams, product descriptions, and specifications complete the publication.

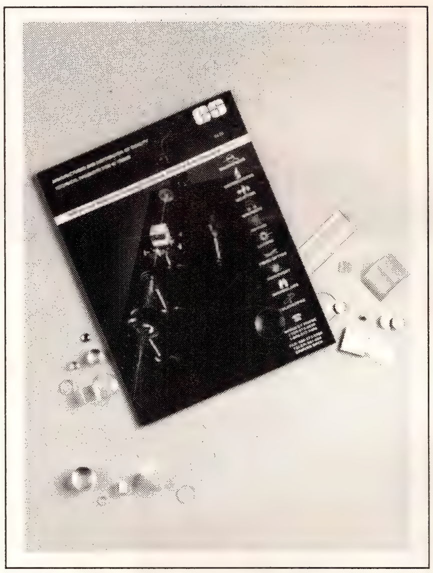
United Technologies Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907. **Circle No. 413**



Test kit helps you select optimal scope

This scope-evaluation kit helps you choose the best digitizing scope for your particular needs. The package consists of a surface-mount circuit board, an instruction manual, and a battery to run the test-generation circuitry. The test kit should answer three important questions about scope measurement: Will the scope miss any important events? Will it accurately capture and measure the signals? Will it trigger the desired signals? The kit also provides the standards to consider when changing from an analog to a digital scope.

Tektronix Inc, Box 500, Beaverton, OR 97077. **Circle No. 414**



Catalog displays optical and industrial products

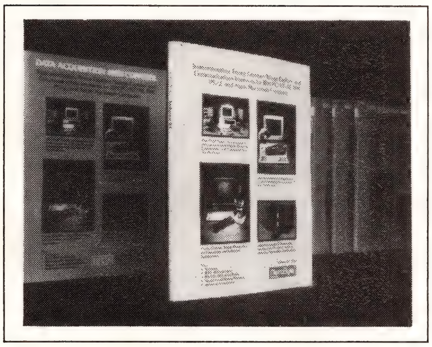
The *1989 Annual Reference Catalog for Optics, Science, and Education* presents more than 5000 optical and industrial products. The 172-pg publication focuses on an expanded line of optics for the OEM market and describes PCX (plano convex) and DCX (double convex) lenses; prisms; achromats, which consist of two lenses put together to form one lense that corrects any color anomaly; beam splitters; and reflectors. Other items include a complete line of microscopes, lasers, fiber optics, and telescopes.

Edmund Scientific Co, Edscorp Bldg, 101 E Gloucester Pike, Barrington, NJ 08007. **Circle No. 415**

Booklet on connectors

This 8-pg brochure introduces the latest addition to the MIL-C-38999 connector series—the 1760 Lanyard release connector. The booklet summarizes the connector's 51-mm-diameter plug design used in avionics applications. Also detailed are the Lanyard Wall Mount, the Jam Nut Receptacle, and the Straight Plug configurations. Finally, the publication describes the Missile Umbilical connector system and the Frangible Missile Umbilical Receptacle, both MIL-STD-1760 connectors.

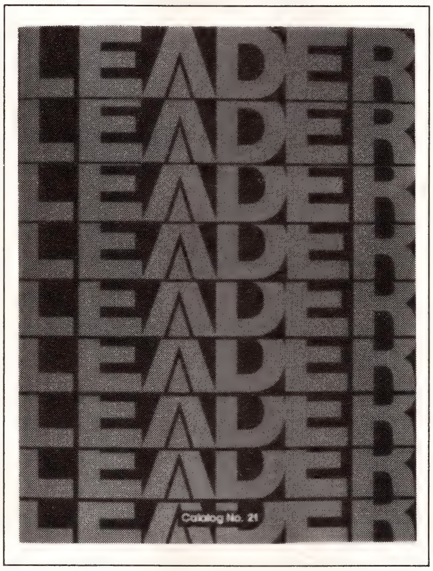
ITT Cannon, Box 3500, Santa Ana, CA 92705. **Circle No. 416**



Handbook depicts data-acquisition products

This product handbook (Volume 21) covers a complete line of data-acquisition, industrial-control and -monitoring, video-imaging, signal-conditioning, personal-instrumentation, and communications products for IBM PC, PC/XT, PC/AT, PS/2, and Apple Macintosh II microcomputers. Featured in the 304-pg publication is the family of high-speed, industrial-control and -monitoring products, the WorkHorse. The book also describes the PCIP-Scope, a single-board, digital-sampling oscilloscope; the DAS-HRES, a 16-bit data-acquisition board; the MV2 frame-grabber board; the VOS/DVOS software, an icon-based user interface for the company's image-processing hardware; and the MBIC family of 19-in., rack-mount IBM PC, PC/XT, PC/AT, and compatible industrial computers.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. **Circle No. 417**



Compilation of test equipment

The 96-pg *Catalog No. 21* contains more than 200 4-color photographs of an expanded line of test equipment. The section, "A Guide to Basic Needs," discusses the different stages of electronic testing and the necessary instruments. Also included are applications for instruments such as digital and analog oscilloscopes, audio and video products, signal generators, frequency counters, and power supplies. The publication spotlights two new products: the Model 2100R 100-MHz CRT read-out oscilloscope and the Model 408 NTSC video sync/test generator. Further, the catalog features specifications for more than 100 products including 13 new instruments.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. **Circle No. 418**

Publication covers network communications

This 216-pg catalog depicts the company's line of network-communications products. The document focuses on baluns, cable, cable assemblies, connectors and couplings, crossconnection and interconnection hardware, fiber optics, jumper/patch cords, switch boxes, cabinets and panels, telecommunications and data communications products, and tools for networking.

Electrospec Inc, 24 E Clinton St, Dover, NJ 07801. **Circle No. 419**

Brochure summarizes plotting network

Diagramming several networked CADD (computer-aided detailed drawing) configurations, this brochure explains how to use the Plot Station with each configuration. The configurations described in the publication include Intergraph workstations, MicroStation, AutoCAD, and other CADD systems that use HP Graphics Language lines.

Byers Engineering Co, 6285 Barfield Rd, Atlanta, GA 30328. **Circle No. 420**

Listing directs you to CAD vendors

The *P-CAD Third-Party Partners Directory* (4th ed) lists service bureaus, authorized training centers,

BOARD LEVEL TIMING PRODUCTS

- Synchronize Multiple Processors
- Time Tag Data

Bancomm's line of board level timing products generate and/or decode standard time code formats (IRIG, XR3, 2137, NASA36, etc.).

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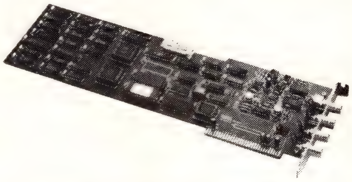
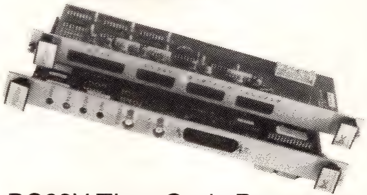


PC03XT Time Code Reader
PC05XT Time Code Generator
PC09XT SLOCODE/DC Level Shift
PC11XT Parallel Output
PC16XT Transport Control

VMEbus:
- Microsecond Resolution



PC03V Time Code Processor
PC05V Time Code Generator
PC26V Time Code Display

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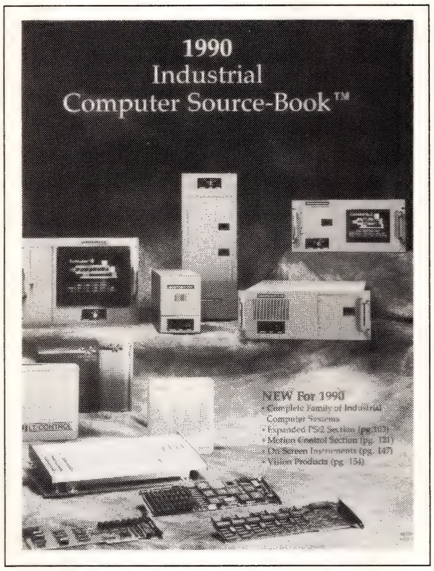
CIRCLE NO 252

and P-CAD-compatible products, including interface software, libraries, special report-generator software, graphics drivers, printers/plotters, and other output drivers from more than 110 vendors in the US and worldwide. The directory is open to any firm offering P-CAD-compatible products or services.

P-CAD, 1290 Parkmoor Ave, San Jose, CA 95126. **Circle No. 421**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• Complete Family of Industrial Computer Systems
• Expanded PS/2 Section (pg. 103)
• Motion Control Section (pg. 121)
• On-Screen Instruments (pg. 147)
• Vision Products (pg. 154)

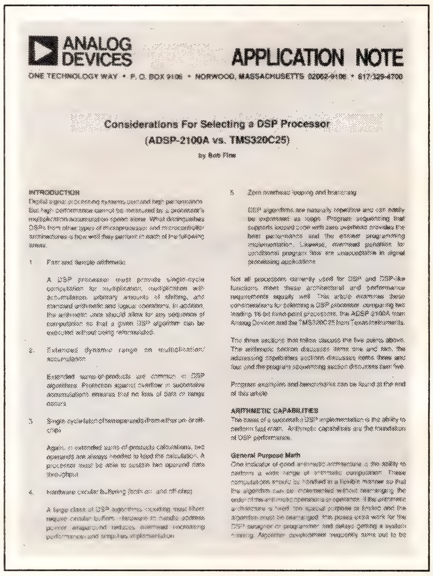
Source book for users of industrial IBM PCs

Aimed at users of IBM PC and compatible products in industrial and educational labs, factory automation, and process-measurement and -control industries, the *1990 Industrial Computer Source Book* covers more than 850 IBM PC-related products. The book presents the 7500 Series of shock-mounted industrial chassis, the 8500 Series of rack-mount industrial computers, the 7500-XC diskless computer/expansion chassis, and the 7410 10-slot chassis. Also included are the 6200-MC50 PS/2 rack-mount chassis, the 8600-RE industrial workstation, and the PC-node diskless computers. The publication features a software section that encompasses the latest operating systems, languages, utility programs, logic and circuit analysis, CAE and CAD, data analysis, and communications packages.

Industrial Computer Source, 4837 Mercury St, San Diego, CA 92111. **Circle No. 422**

Note briefs you on choosing a DSP processor

The application note, *Considerations for Selecting a DSP Processor*, explains five key elements for choosing among the high-performance DSP-process and microcontroller architectures. Delving into the five elements, the 16-pg note discusses fast and flexible arithmetic, extended dynamic range on multiply/accumulates, single-cycle fetch of two operands (both on and off chip), hardware circular buffers, and zero-overhead looping. Using these criteria, the publication compares two fixed-point processors, the company's ADSP-2100A and TI's TMS320C25. Diagrams, comparison tables, and examples illustrate the foundation of DSP performance: fast math, addressing (data fetching), and program sequencing. The note also provides benchmarks for evaluating both the ADSP-2100A and TMS320C25.



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Considerations For Selecting a DSP Processor
(ADSP-2100A vs. TMS320C25)
by Bob Fine

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. **Circle No. 423**

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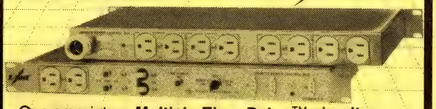

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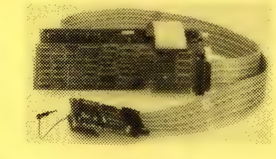
CIRCLE NO 325

68HC11

PC-based emulator for 68HC11



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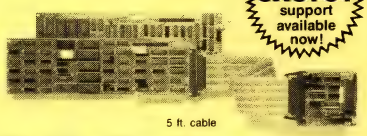

5 ft. cable

8051

See EEM 88/89 Page D-1304

PC based emulators for the 8051 family

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PRICES: 32K Emulator for 8031 $1790,* 4K Trace $1495*

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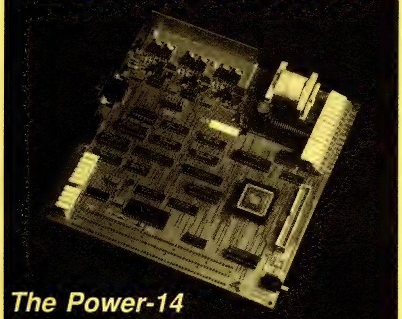
CIRCLE NO 327

DSP In Control



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- ☐ libraries for all memory models
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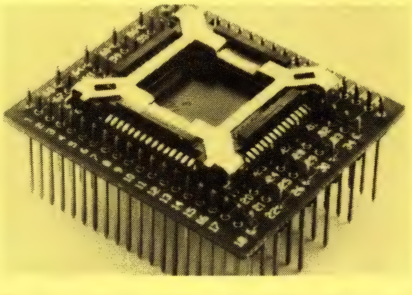

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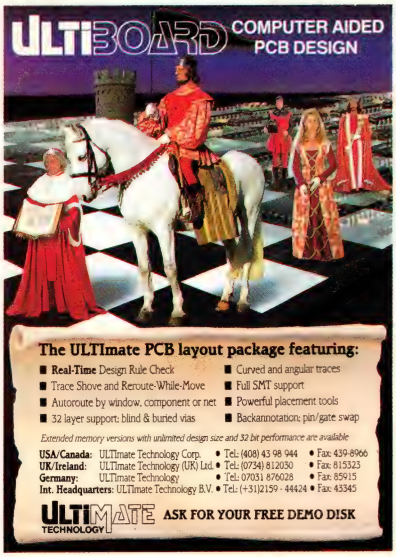

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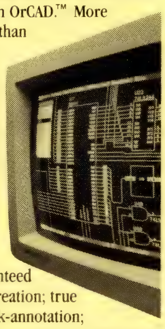

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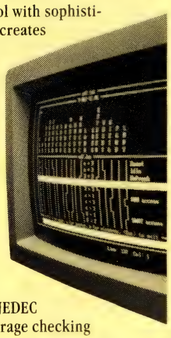

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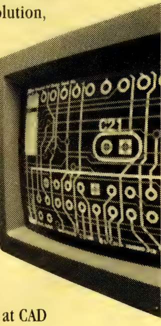

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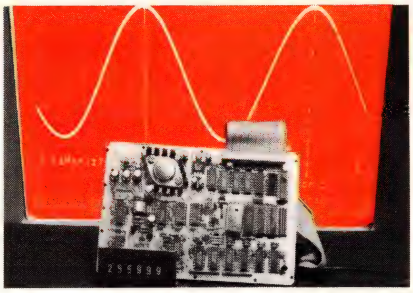

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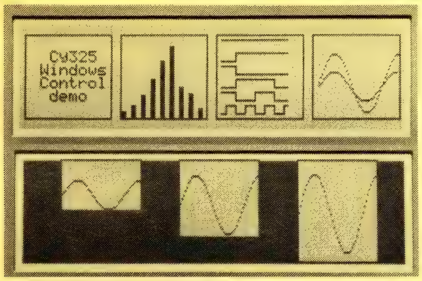

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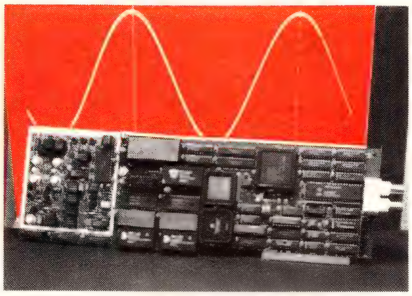

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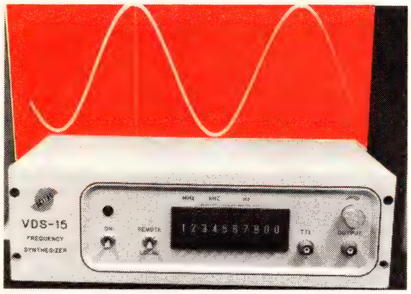

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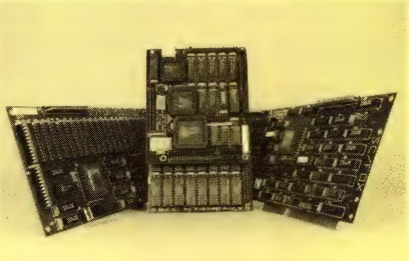

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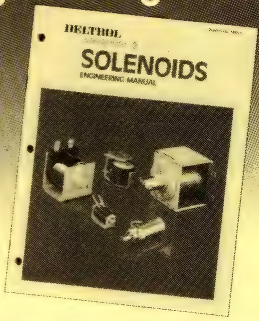

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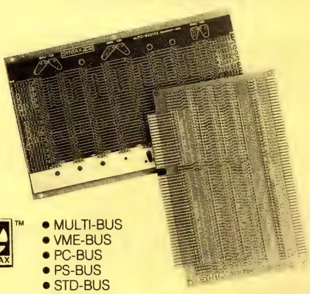

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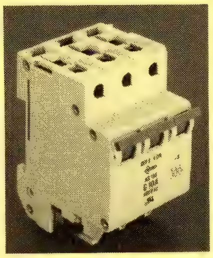

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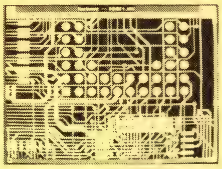

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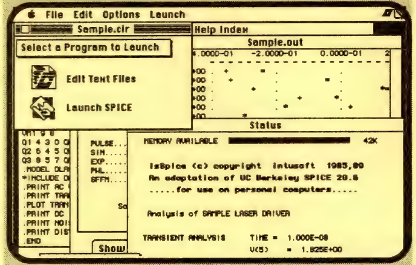

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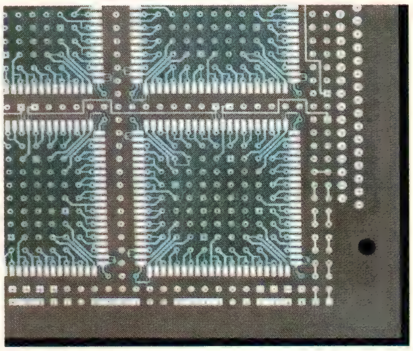

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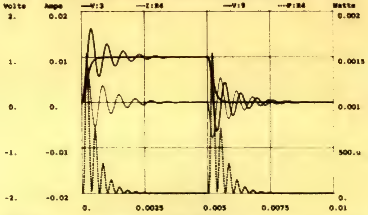

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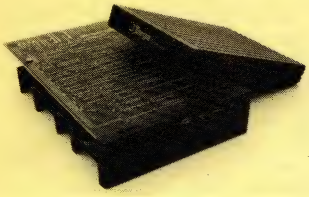

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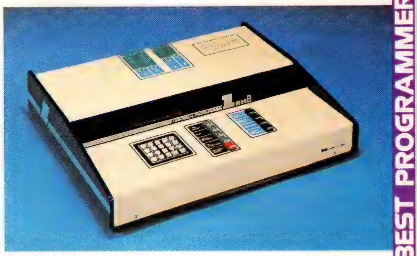

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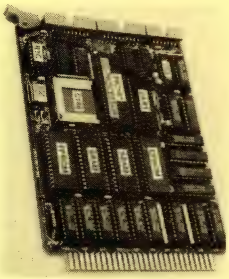

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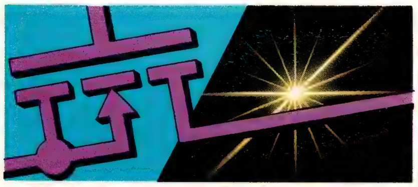

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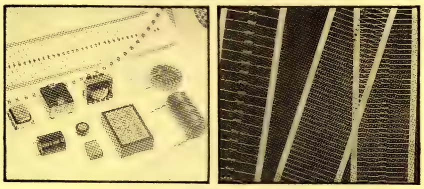

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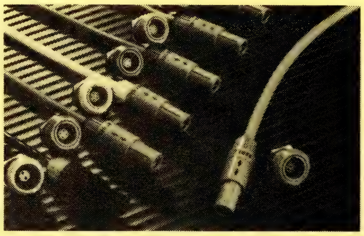

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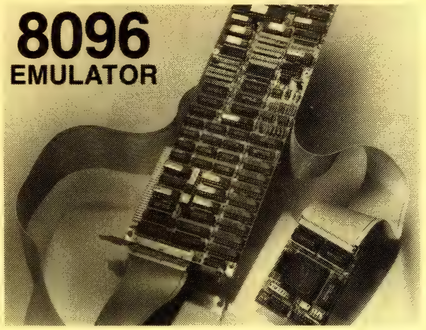

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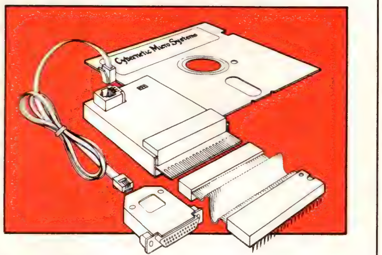

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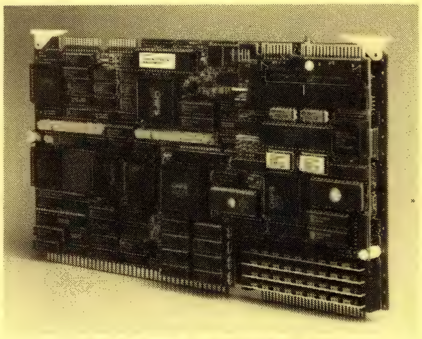

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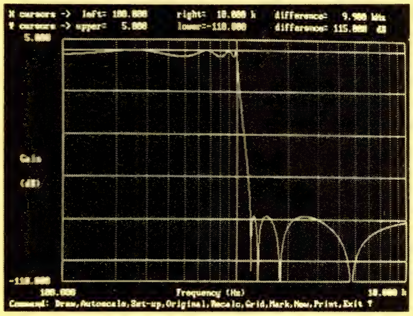

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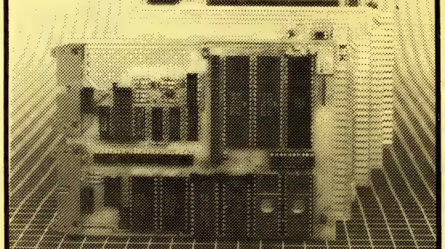

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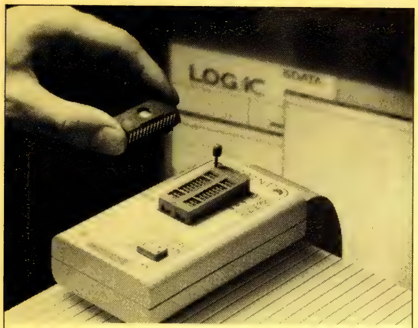

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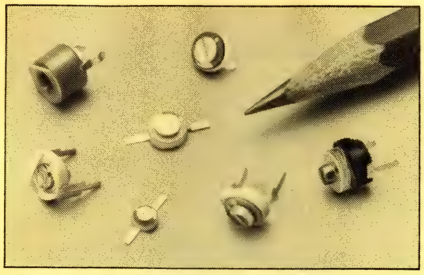

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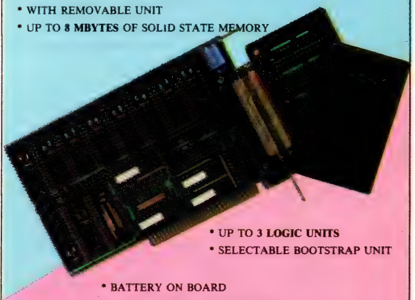

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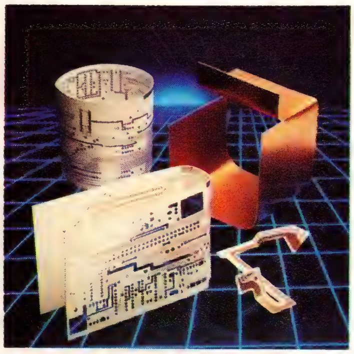

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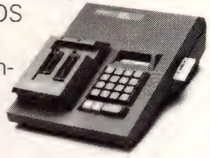

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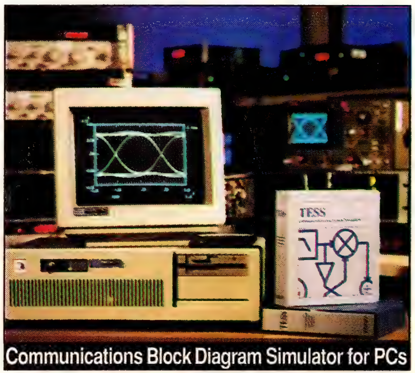

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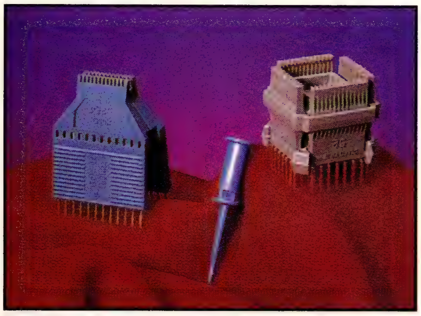

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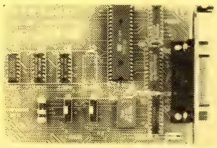

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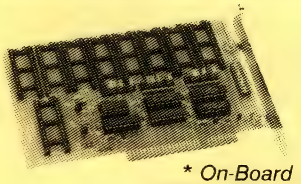

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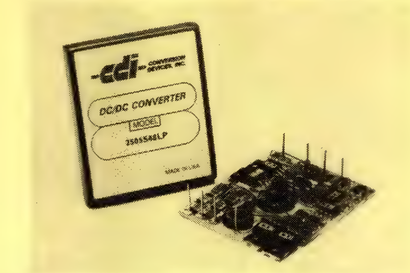

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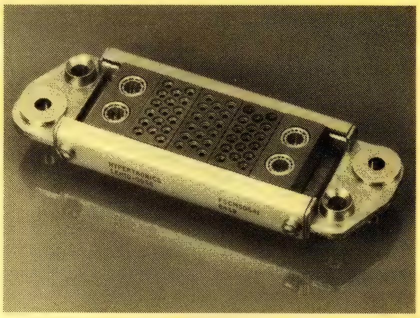

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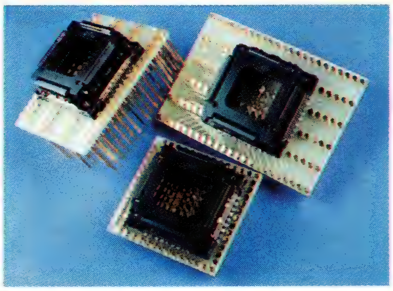

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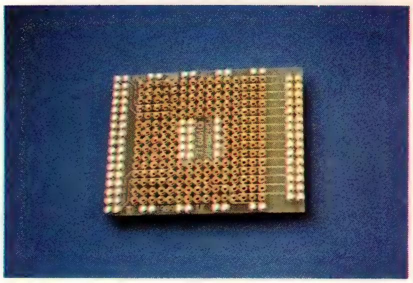

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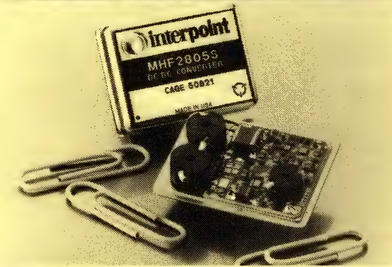

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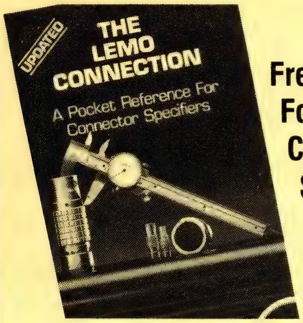

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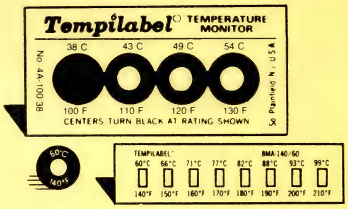

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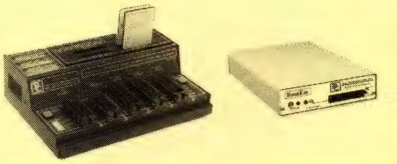

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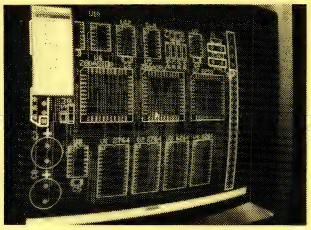

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EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News Edition
Nov. 23	Nov. 2	16th Annual μP/μC Directory, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
Dec. 7	Nov. 16	Product Showcase — Volume I, Power Supplies	Closing: Nov. 22 Mailing: Dec. 14
Dec. 21	Nov. 30	Product Showcase — Volume II, Components	

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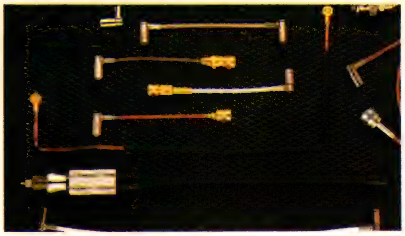
COAXIAL RF CABLE ASSEMBLIES



E. F. Johnson JCM commercial-grade equivalents to SMA, SMB and SMC subminiature connectors are now available as RF cable assemblies with any combination of A, B or C type connectors. Virtually any flexible, rigid or semi-rigid coaxial cable can be ordered with the appropriate JCM connectors. The JCM line includes screw and snap-fit connectors in a variety of mounting configurations. These include jacks and plugs in straight and right-angle configurations for bulkhead and PC board mounting, as well as standard mounts with mounting hardware included. In addition, Johnson can create custom modifications of standard items, as well as design and manufacture special connectors to customer specifications. Contact E. F. Johnson, 299 Johnson Ave., Waseca, MN 56093. Telephone: (800) 247-8256. In MN: (507) 835-6303. FAX (507) 835-6485.

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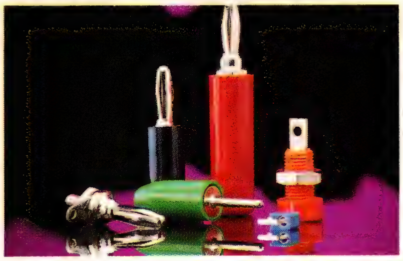
ELECTRONIC CIRCUIT HARDWARE



E. F. Johnson has long been a leader in the design and manufacture of Electronic Circuit Hardware. The same design expertise that created stripline plugs and jacks, a semi automatic termination system for volume production applications, can be yours for just about any special hardware application you may have. In addition to the standard plugs and jacks, many specials are made for particular customer applications. Plugs are supplied for crimp applications, with just about any plating, many shank lengths, diameters and thread sizes with many banana plug spring lengths and widths. Contact E. F. Johnson, 299 Johnson Avenue, Waseca, MN 56093. Telephone: (800) 247-8256. In MN: (507) 835-6303. FAX: (507) 835-6485.

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Raymond Kurzweil and the second Industrial Revolution

Jay Fraser,
Associate Editor

Whiz kid. Boy wonder. Genius. All these terms have been applied to Raymond Kurzweil. In person he's courteous and soft-spoken and appears uneasy when his accomplishments are mentioned. Nevertheless, he's been quoted as saying that when he was five years old he already knew that he'd grow up to be a successful and important scientist. He was right.

Kurzweil, now 41, has invented a machine that can read any printed text aloud in a choice of four artificial voices. It has been heralded as the greatest aid to the blind since Braille. He also invented the Kurzweil 250, the state-of-the-art music synthesizer that can accurately recreate the sound of every known musical instrument, singularly or in combinations. His latest invention is a voice-activated computer. You simply speak to the machine, and it types out whatever you say.

These three devices have made Kurzweil very successful. Today he is the chairman and chief executive officer of two corporations he founded and chairman of a division of Xerox. He became a millionaire years ago.

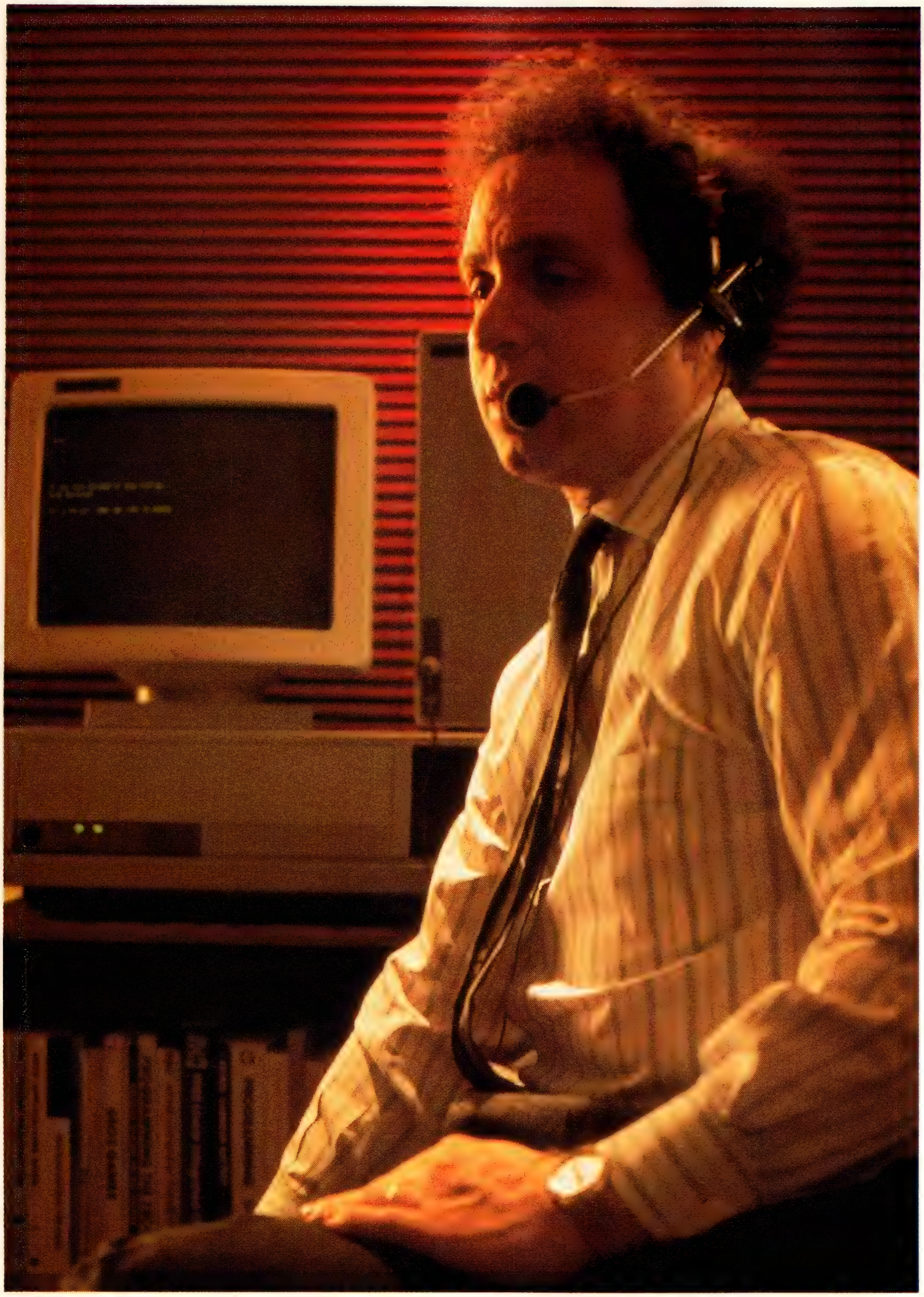
Kurzweil was born into an artistic family in Queens, New York. His mother was an illustrator and his father was a concert pianist, composer, and conductor. His father founded the music department at Queensborough College and for many years was its chairman. When he was six years old, Kurzweil was given his first piano lesson by his father.

A love of music and computers

Kurzweil quickly developed a lifelong love of music, but he also became fascinated with computers at an early age. When he was 13 years old, he wrote a software program for statistical analysis that was distributed by IBM. When he was 17, he combined these interests and won a Westinghouse Science Talent Search award with a program that enabled a computer to write music in the styles of composers such as Beethoven and Mozart. (Five other winners of the Westinghouse award have gone on to win the Nobel Prize.)

Kurzweil entered the Massachusetts Institute of Technology the following year. When he was a sophomore, he wrote a program to match high school students with appropriate colleges and sold it to Harcourt Brace Jovanovich for $100,000. He also took Marvin Minsky's course in artificial intelligence. It proved to be a turning point.

"I became interested in pattern recognition," he says. "There had been pattern-recognition machines almost since computers were invented, but they only recognized one or two type fonts that were very well printed. I thought I



Raymond Kurzweil demonstrates *his latest invention—a voice-activated computer.*

could come up with an approach to reading print as it really exists in the world."

After graduating from MIT with a bachelor's degree in computer science and literature and doing consulting work for a while, Kurzweil founded his own firm in Waltham, Massachusetts. He wanted to build a machine that could read whatever text was shown to it and speak whatever it read.

Two lean years followed. It was extremely difficult for Kurzweil to find investors. Many people thought the machine could never work. He sold his car and most of his personal electronic equipment to keep his company afloat.

At one point the telephone company threatened to disconnect him because of an unpaid bill, so he went to a pawn shop to hock his tape recorder to raise some money. While he was there, a dog tried to bite him and tore the leg of his trousers. It was a stroke of luck. The dog's owner gave him $50 to cover the damages. It was just enough to pay the phone bill.

Kurzweil introduced his Reading Machine in 1976. It was a genuine breakthrough. To operate it, you simply run an optical scanner across a printed or typed line, and the Reading Machine reads it aloud. It can read virtually any

Stevie Wonder plays *a Kurzweil 250 at a party Raymond Kurzweil threw for him.*

type face in any publication, bound or flat. The Reading Machine was the first consumer product to successfully incorporate artificial-intelligence technology.

Enter Stevie Wonder

Stevie Wonder, a blind musician, was one of the first purchasers of a Reading Machine. "He just called us up and dropped in," says Kurzweil. "We didn't have any working models on hand, so we quickly put one together for him. He came by, learned how to use it, wrote out a check, and left with it that day."

That meeting began a friendship between the two men. Stevie Wonder is an avid student of technology, and he and Kurzweil talked many times about the applications of technology to the making of music.

"One day he was lamenting the fact that there were two different worlds of music and no viable bridge between them," recalls Kurzweil. "There's the acoustic world—the instruments that create the rich, complex, musically deep sounds on which we've based our musical tradition. Then there's the electronic world, which provides powerful artistic methods of control, but the sounds that are controlled are very thin. He said wouldn't it be great if we could apply this powerful control to the acoustic sounds."

That's exactly what Kurzweil set out to do next.

In 1984 he unveiled the Kurzweil 250, a music synthesizer that can sound uncannily like a grand piano, guitar, saxophone, or any other musical instrument. It can layer sounds over one another, add tremolo or vibrato, and remember everything it plays. One person can make a Kurzweil 250 sound like a jazz drummer or a full symphony orchestra.

The effects of the Kurzweil 250 on the world of music have been far-reaching. Pop stars immediately realized its huge potential. Prince, Herbie Hancock, Madonna, and—of course—Stevie Wonder, as well as many others have added one or more to their bands. The Kurzweil 250 is also widely used in recording studios to accompany singers and provide the background music for commercials, television shows, and films. It has even begun to replace classical musicians.

On June 7, 1989, the California Digital Philharmonic Orchestra gave its debut performance at the Museum of Science and Industry in Los Angeles. They played the music of Bach, Mozart, Bizet, Grieg, and John Philip Sousa on 13 Kurzweil 250s. Kurzweil himself was the guest of honor. "You get a feeling of cognitive dissonance when you're hearing orchestral music and you're seeing 13 people in tails and performance gowns playing it on synthesizers," he says with a smile. "But it was great."

The inroads that synthesizers are making worry the musicians' union. In the negotiations two years ago between the producers of Broadway shows and Local 802 of the American Federation of Musicians, one of the most hotly debated issues was the use of synthesizers. The producers won the right to include them in their orchestras. Someday Broadway shows may be sung and danced to music provided by a single synthesizer. Not surprisingly, many musicians fear that these machines will make them obsolete.

"Nonsense," says Kurzweil. He acknowledges that his synthesizer has removed certain opportunities. "But for every opportunity it removes, it creates more that didn't exist before."

He gives as an example industrial and training films. Many companies couldn't afford to hire a group of musicians to provide the background music for a film, so they relied on prerecorded sound tracks. Now they can hire a person with a synthesizer to compose and play original music for these films.

"A strong understanding of the fundamentals of music continues to be the best possible preparation for creating music, regardless of the instrument," says Kurzweil.

"Music has always used the most advanced technologies available—from the cabinet-making crafts of the 18th century, the metalworking industries of the 19th century, and the analog electronics of the 1960s to the digital electronics and artificial intelligence of the 1980s and 1990s."

Kurzweil compares the people who are resisting the new electronic musical instruments to the Luddites of two centuries ago, who made a misguided and futile attempt to hold back the Industrial Revolution. He sees us now on the edge of a second Industrial Revolution. The first one gave us machines that extended our physical capabilities. The second one is giving us machines that extend our mental abilities.

Two years after the successful introduction of his synthesizer, Kurzweil came out with his voice-activated computer, now called the VoiceReport. When you speak to this machine, it first displays your words on a computer screen for editing, then prints them out as hard copy. It comes with a vocabulary of 5000 words, but you can add more.

The VoiceReport is another application of the technology of pattern recognition. Before you can dictate to the machine, you have to read a list of more than 200 words to it. The words contain all the sounds in the English language. Once the VoiceReport learns to recognize your individual pronunciation, you can speak freely to it. The machine can also be programmed to print out an entire sentence or paragraph when it hears a trigger word or phrase.

Although all his inventions bear his name, Kurzweil is quick to point out that they were the result of group efforts. He talks about his role in terms his father, the orchestra conductor, would readily understand.

"I attract a team, get them assembled, and provide communication across the different disciplines," he says. "What I try to do is provide leadership, a sort of galvanizing force to make it all happen."

Making sure people with different specialties can communicate with one another is essential. For example, the engineers and scientists who worked on the VoiceReport were from fields as diverse as linguistics, signal processing, speech science, and pattern recognition.

"When you bring experts from these disciplines together, you have to make sure they understand each other's methods and terminology. Because sometimes in signal processing they might have the solution to a difficult problem in linguistics and vice versa," Kurzweil explains.

Managing his two companies takes up much of Kurzweil's time and energy these days. "There was a time when I actually wrote code," he says. "I wrote a lot of the software that went into the synthesizer and the early speech recognizers. Today I probably spend half my time with technology issues and half with business issues."

When asked what he thinks the most important developments in technology will be in the near future, Kurzweil responds, "The next big frontier is continuous-speech recognition. In the next few years, you'll begin to see large-vocabulary, continuous-speech systems that can recognize anyone's voice. Continuous speech and voice-activated word processing will begin to merge."

Kurzweil lives quietly in a suburb of Boston with his wife and two children. Even though it's difficult for him to find the time, he still plays music occasionally for relaxation. When he does, he has a choice of instruments. At his home he keeps three Kurzweil 250s and his father's grand piano. EDN

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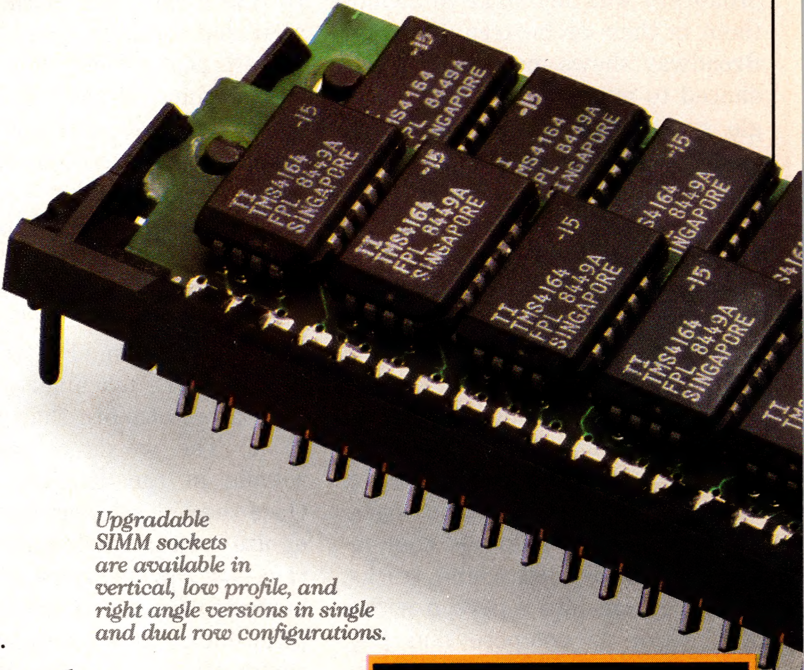

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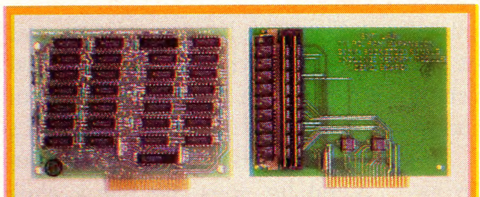
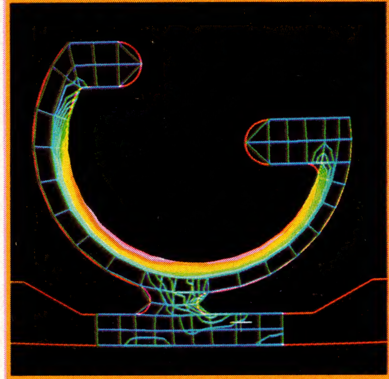


Molex SIMM socket (right) takes up dramatically less board space than DIP packaging (left).



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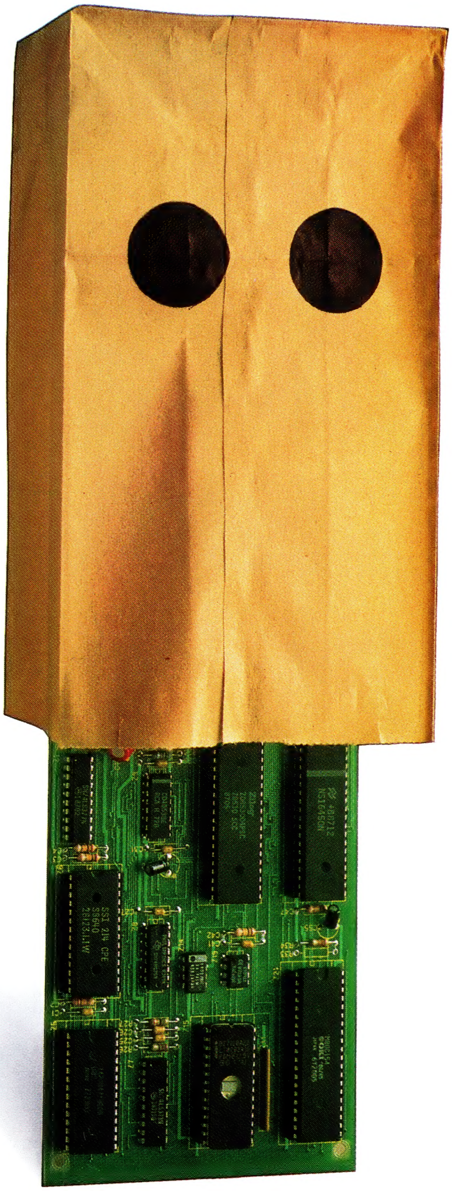

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